

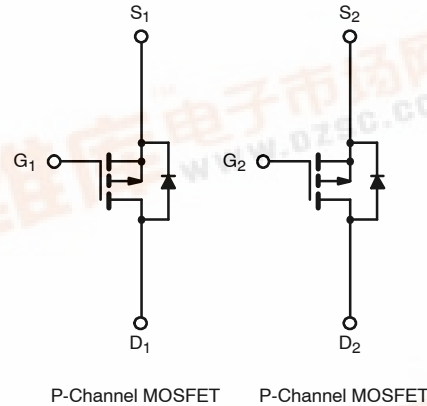
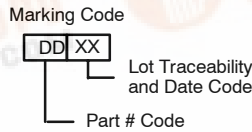
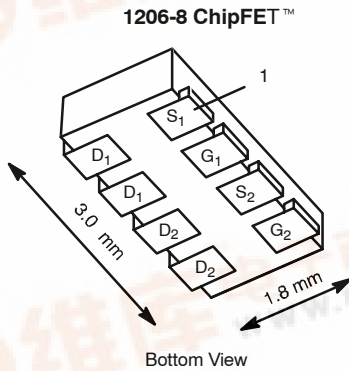


SI5975DC
Vishay Siliconix

Dual P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-12	0.086 @ V _{GS} = -4.5 V	-4.1
	0.127 @ V _{GS} = -2.5 V	-3.4
	0.164 @ V _{GS} = -1.8 V	-3.0

TrenchFET®
Power MOSFETs
1.8-V Rated



Ordering Information: SI5975DC-T1

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	-12		V	
Gate-Source Voltage	V _{GS}	±8			
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	-4.1	-3.1	A
		T _A = 85°C	-3.0	-2.2	
Pulsed Drain Current	I _{DM}	-10			
Continuous Source Current (Diode Conduction) ^a	I _S	-1.8	-0.9		
Maximum Power Dissipation ^a	P _D	T _A = 25°C	2.1	1.1	W
		T _A = 85°C	1.1	0.6	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 sec	50	60	°C/W
		Steady State	90	110	
Maximum Junction-to-Foot (Drain)	R _{thJF}	30	40		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

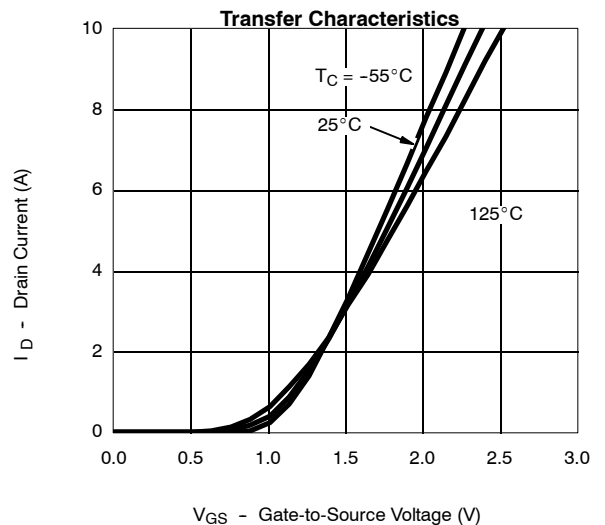
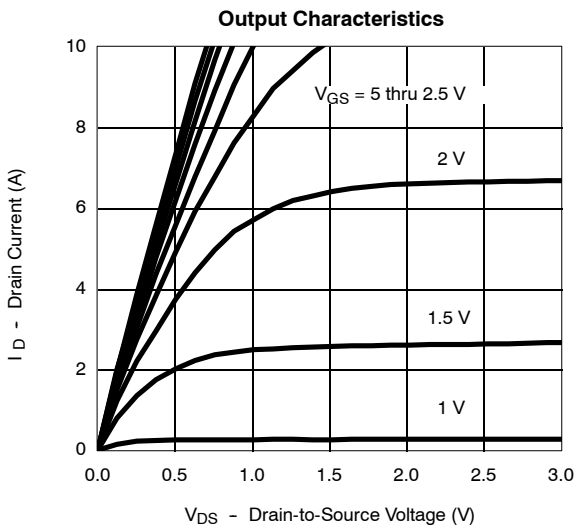


SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -1 mA	-0.45			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -9.6 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -9.6 V, V _{GS} = 0 V, T _J = 85 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-10			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -3.1 A		0.070	0.086	Ω
		V _{GS} = -2.5 V, I _D = -2.5 A		0.100	0.127	
		V _{GS} = -1.8 V, I _D = -1.0 A		0.131	0.164	
Forward Transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -3.1 A		8		S
Diode Forward Voltage ^a	V _{SD}	I _S = -0.9 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -3.1 A		5.7	9	nC
Gate-Source Charge	Q _{gs}			1.2		
Gate-Drain Charge	Q _{gd}			1.2		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		10	15	ns
Rise Time	t _r			20	30	
Turn-Off Delay Time	t _{d(off)}			31	45	
Fall Time	t _f			26	40	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -0.9 A, di/dt = 100 A/μs		40	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

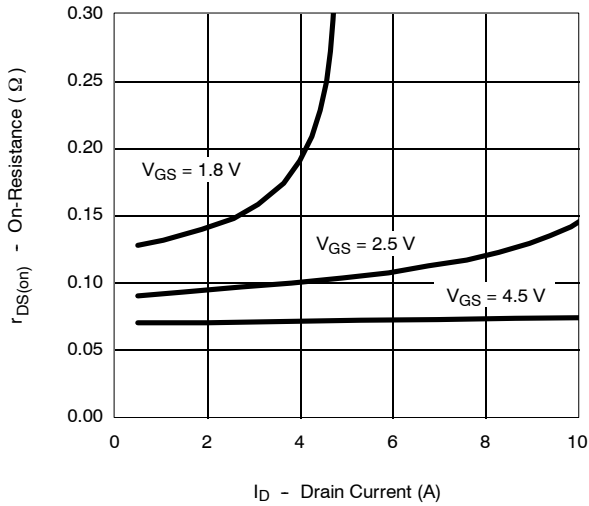
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



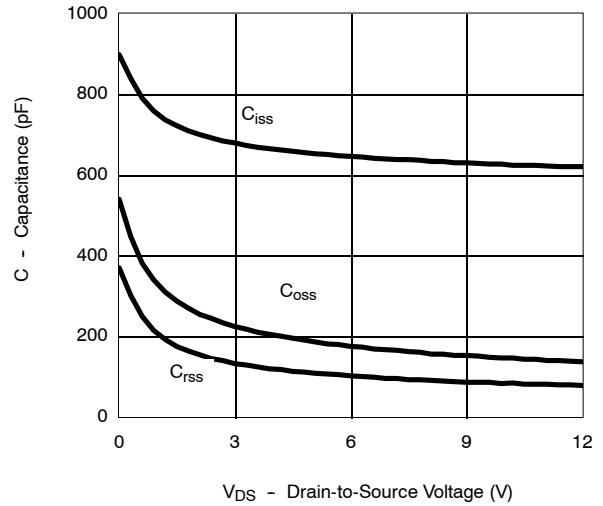


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

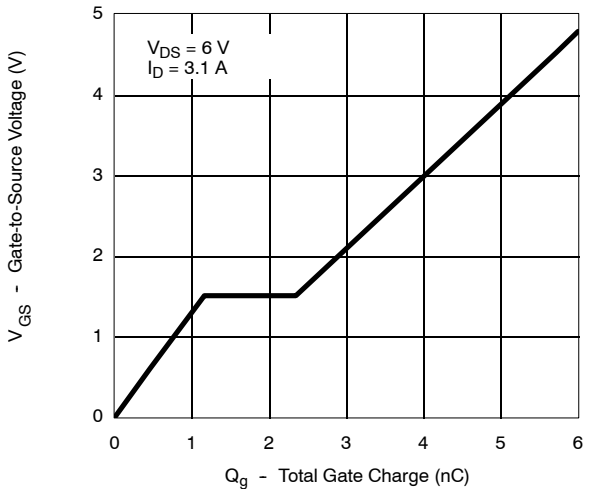
On-Resistance vs. Drain Current



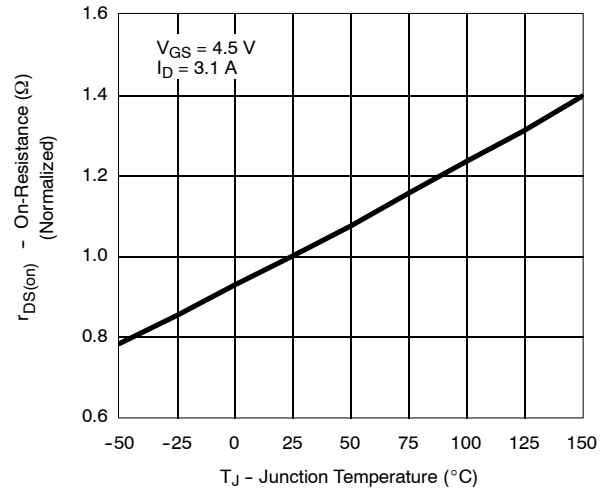
Capacitance



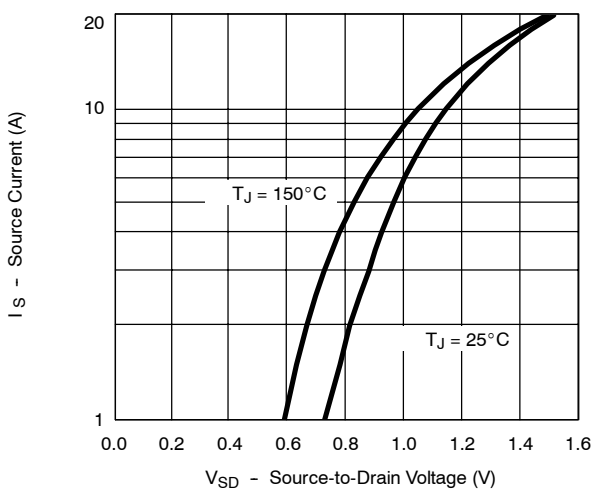
Gate Charge



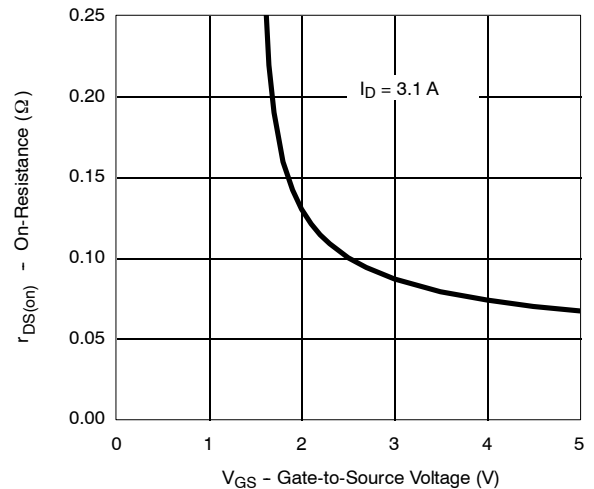
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

