

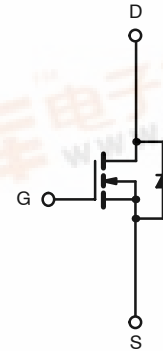
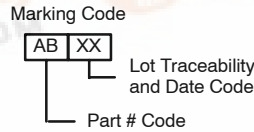
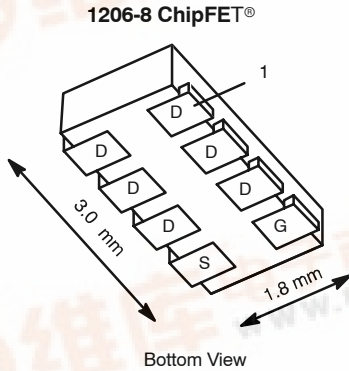


Si5404DC
Vishay Siliconix

N-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
20	0.030 @ V _{GS} = 4.5 V	7.2
	0.045 @ V _{GS} = 2.5 V	5.9

TrenchFET[®]
Power MOSFETs
2.5-V Rated



Ordering Information: Si5404DC-T1

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	20		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	7.2	5.2	A
		T _A = 85 °C	5.2	3.8	
Pulsed Drain Current	I _{DM}	20			
Continuous Source Current (Diode Conduction) ^a	I _S	2.1	1.1	W	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.5		1.3
		T _A = 85 °C	1.3		0.7
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 5 sec	40	50	°C/W
		Steady State	80	95	
Maximum Junction-to-Foot (Drain)	R _{thJF}	15	20		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

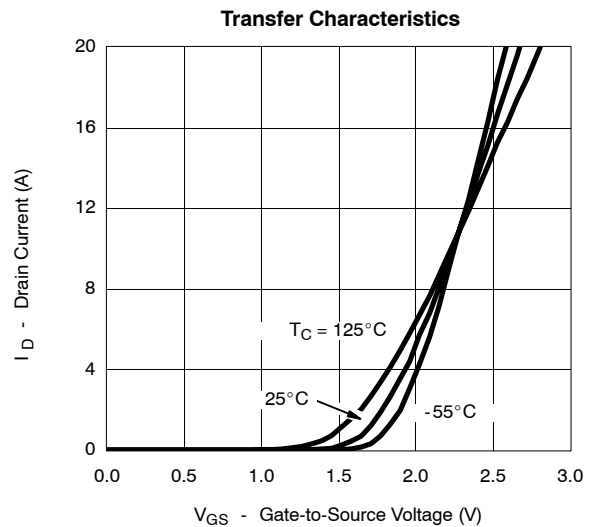
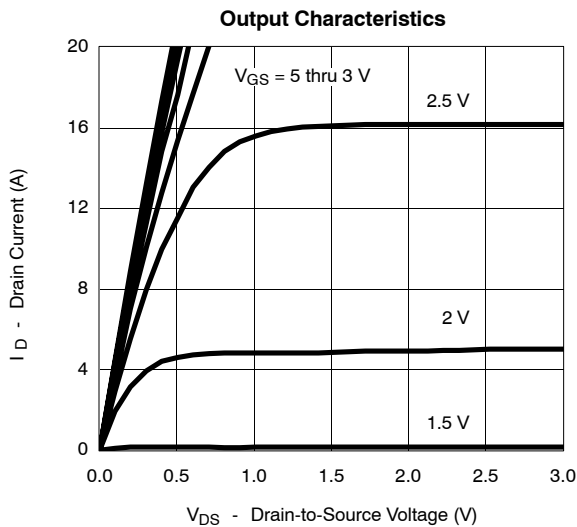


SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.6			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 85 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.2 A		0.025	0.030	Ω
		V _{GS} = 2.5 V, I _D = 4.3 A		0.038	0.045	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 5.2 A		20		S
Diode Forward Voltage ^a	V _{SD}	I _S = 1.1 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 5.2 A		12	18	nC
Gate-Source Charge	Q _{gs}			2.4		
Gate-Drain Charge	Q _{gd}			3.2		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		20	30	ns
Rise Time	t _r			40	60	
Turn-Off Delay Time	t _{d(off)}			40	60	
Fall Time	t _f			15	23	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.1 A, di/dt = 100 A/μs		30	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

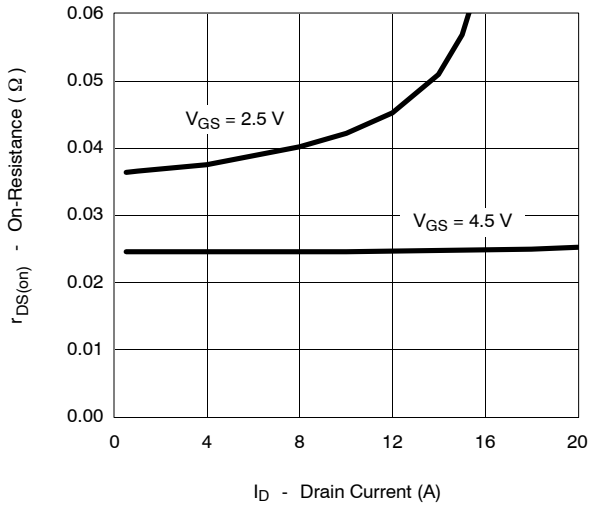
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



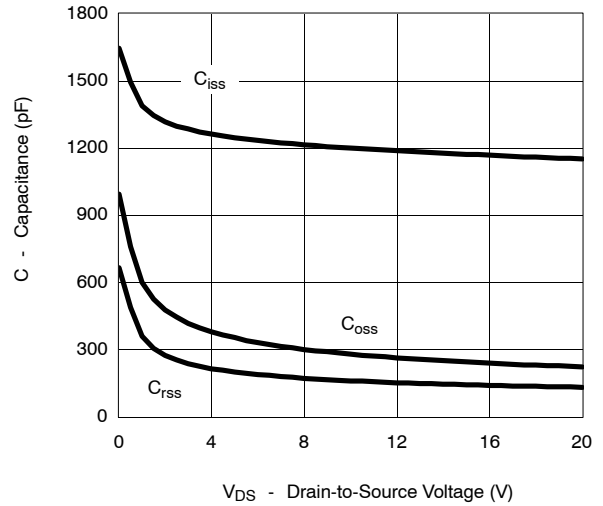


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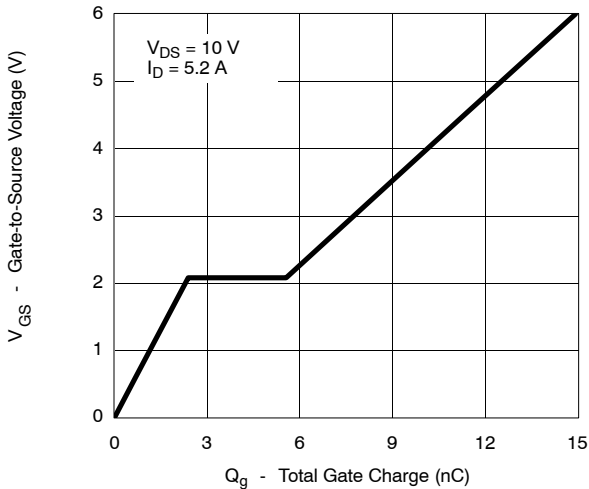
On-Resistance vs. Drain Current



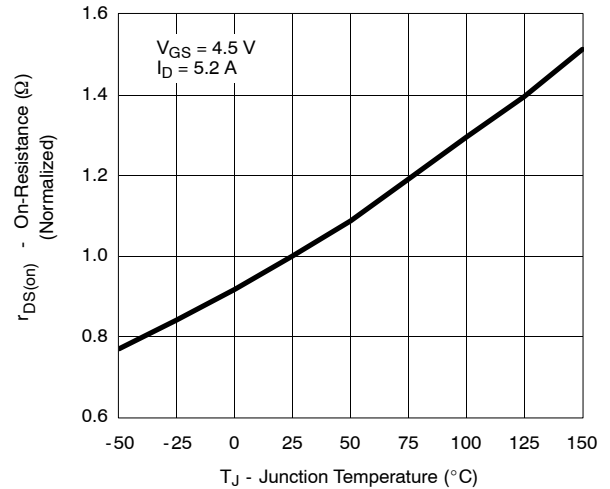
Capacitance



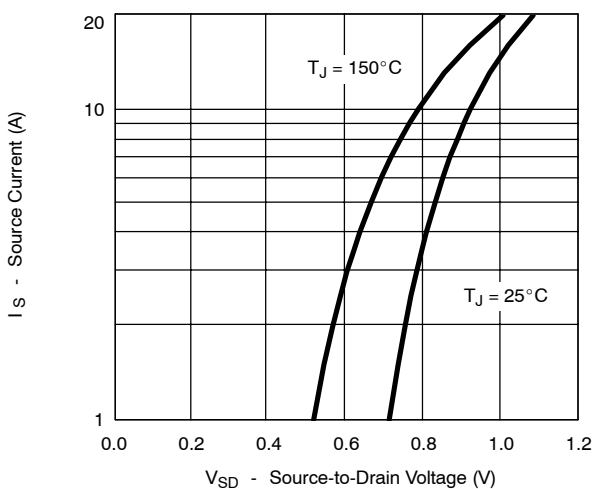
Gate Charge



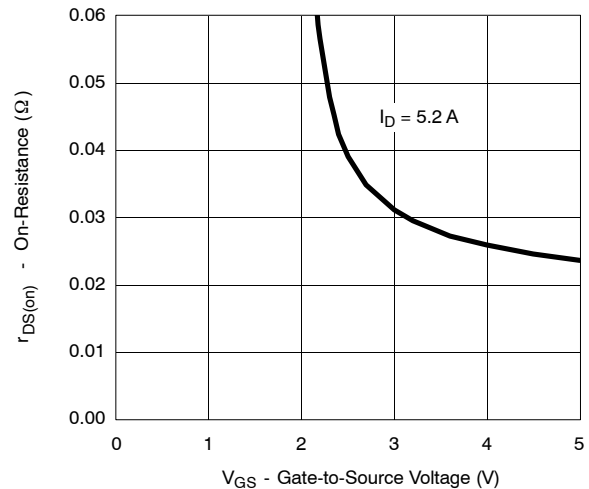
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

