



September 2001

# Si6435DQ

## 30V P-Channel PowerTrench<sup>®</sup> MOSFET

### General Description

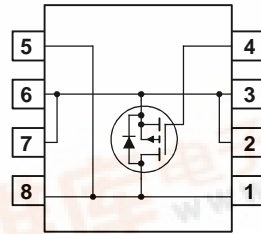
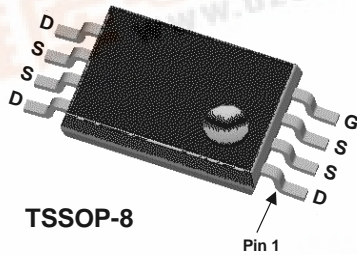
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).

### Applications

- Battery protection
- DC/DC conversion
- Power management
- Load switch

### Features

- -4.5 A, -30 V  $R_{DS(ON)} = 40\text{ m}\Omega @ V_{GS} = -10\text{ V}$   
 $R_{DS(ON)} = 70\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- Extended  $V_{GSS}$  range ( $\pm 20\text{V}$ ) for battery applications
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Low profile TSSOP-8 package



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1) – Pulsed	-4.5	A
		-30	
$P_D$	Power Dissipation (Note 1a) (Note 1b)	1.3	W
		0.6	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	87	$^\circ\text{C/W}$
		114	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6435	Si6435DQ	13"	16mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-23		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.7	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}, T_J = 125^\circ\text{C}$		27 42 38	40 70 60	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-30			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -15\text{ V}, I_D = -4.5\text{ A}$		12		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		854		pF
$C_{oss}$	Output Capacitance			215		pF
$C_{rss}$	Reverse Transfer Capacitance			112		pF
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		9	20	ns
$t_r$	Turn–On Rise Time			14	20	ns
$t_{d(off)}$	Turn–Off Delay Time			29	55	ns
$t_f$	Turn–Off Fall Time			15	25	ns
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = -1.25\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$		19	80	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -4.5\text{ A},$ $V_{GS} = -10\text{ V}$		15	35	nC
$Q_{gs}$	Gate–Source Charge			2.4		nC
$Q_{gd}$	Gate–Drain Charge			3		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-1.25	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.25\text{ A}$ (Note 2)		-0.75	-1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

- a)  $R_{\theta JA}$  is  $87\ ^\circ\text{C}/\text{W}$  (steady state) when mounted on a 1 inch<sup>2</sup> copper pad on FR-4.  
b)  $R_{\theta JA}$  is  $114\ ^\circ\text{C}/\text{W}$  (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics

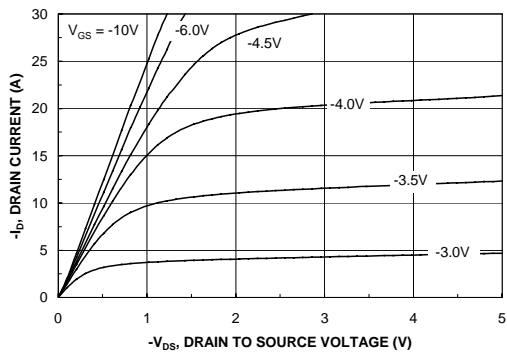


Figure 1. On-Region Characteristics.

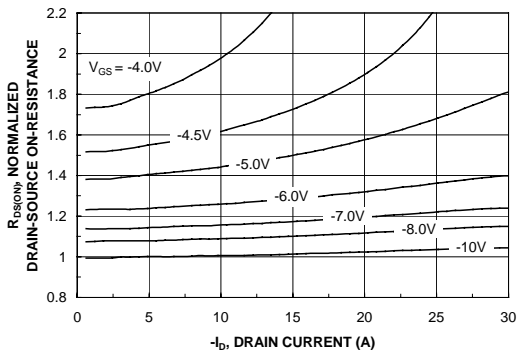


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

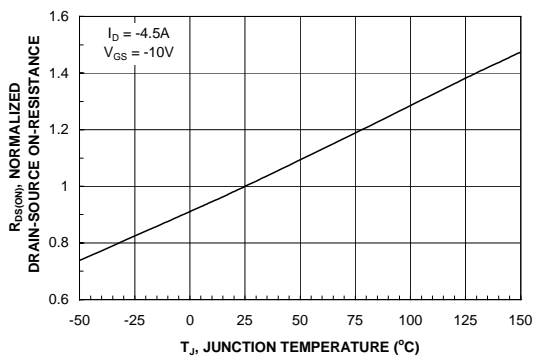


Figure 3. On-Resistance Variation with Temperature.

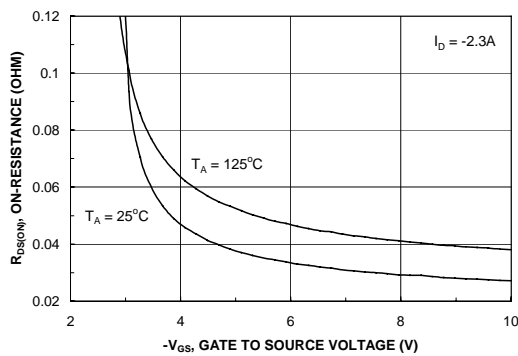


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

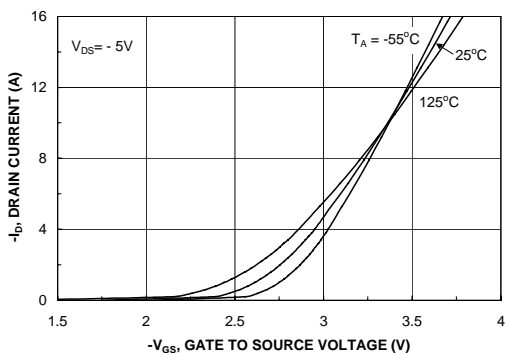


Figure 5. Transfer Characteristics.

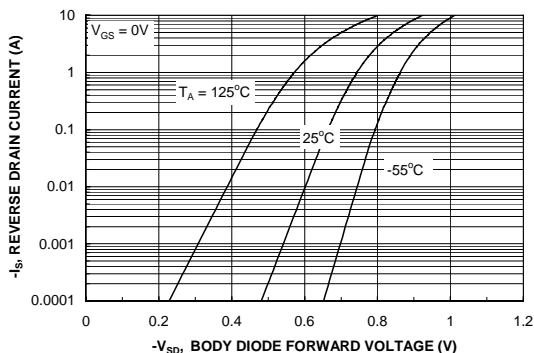


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

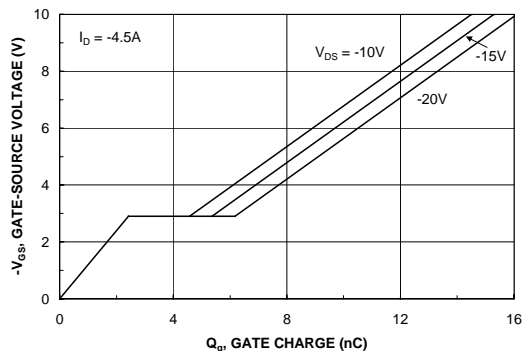


Figure 7. Gate Charge Characteristics.

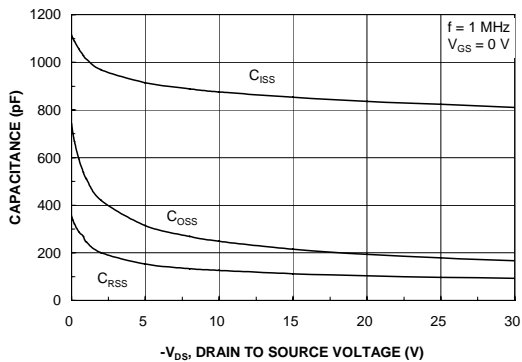


Figure 8. Capacitance Characteristics.

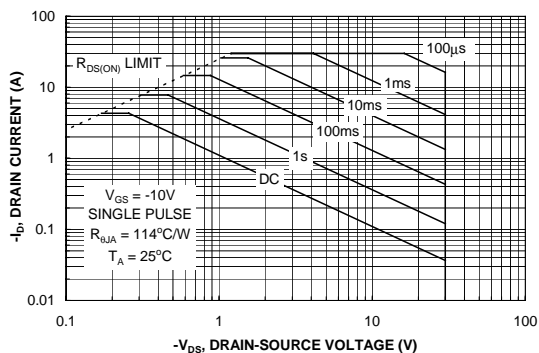


Figure 9. Maximum Safe Operating Area.

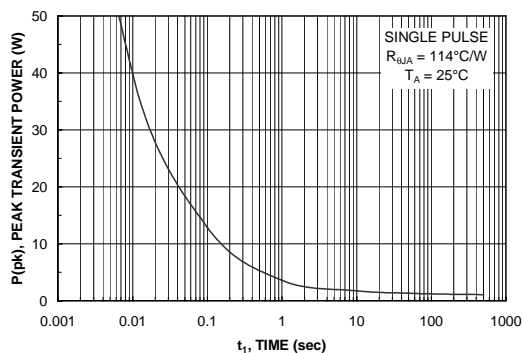


Figure 10. Single Pulse Maximum Power Dissipation.

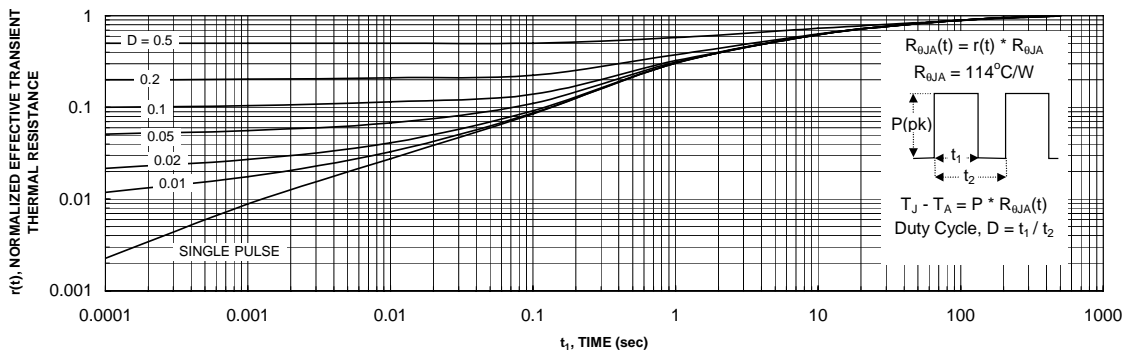


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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