

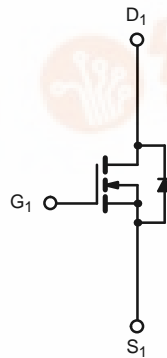
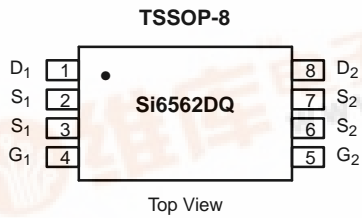


**Si6562DQ**  
Vishay Siliconix

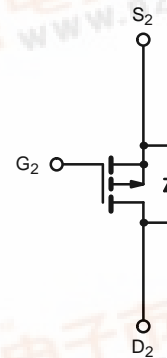
## N- and P-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY			
	$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	20	0.030 @ $V_{GS} = 4.5$ V	$\pm 4.5$
		0.040 @ $V_{GS} = 2.5$ V	$\pm 3.9$
P-Channel	-20	0.050 @ $V_{GS} = -4.5$ V	$\pm 3.5$
		0.085 @ $V_{GS} = -2.5$ V	$\pm 2.7$

**TrenchFET<sup>®</sup>**  
Power MOSFETs  
2.5-V Rated



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	$V_{DS}$	20	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 4.5$	A
		$T_A = 70^\circ\text{C}$	$\pm 3.6$	
Pulsed Drain Current	$I_{DM}$	$\pm 30$	$\pm 30$	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.25	-1.25	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	1.0	W
		$T_A = 70^\circ\text{C}$	0.64	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	125	$^\circ\text{C/W}$

Notes:  
a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

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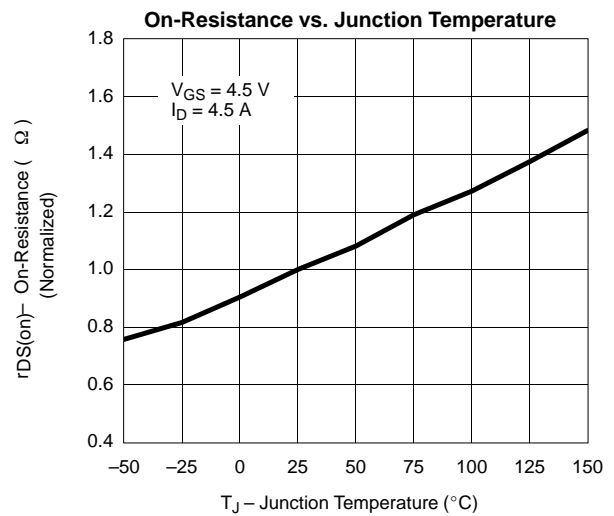
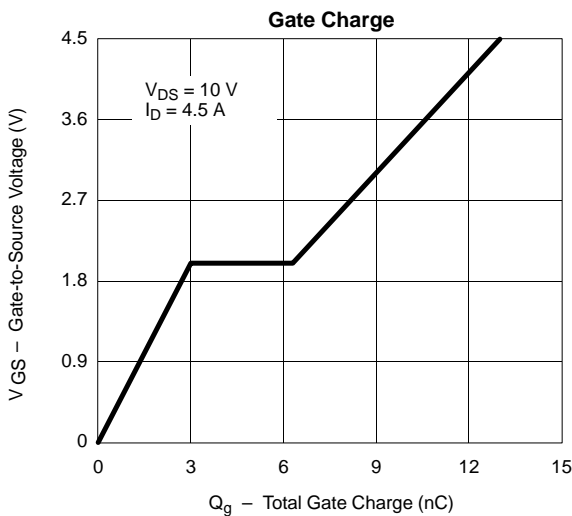
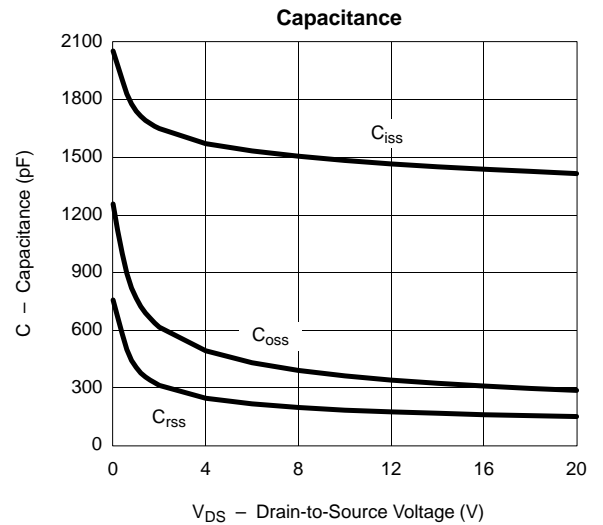
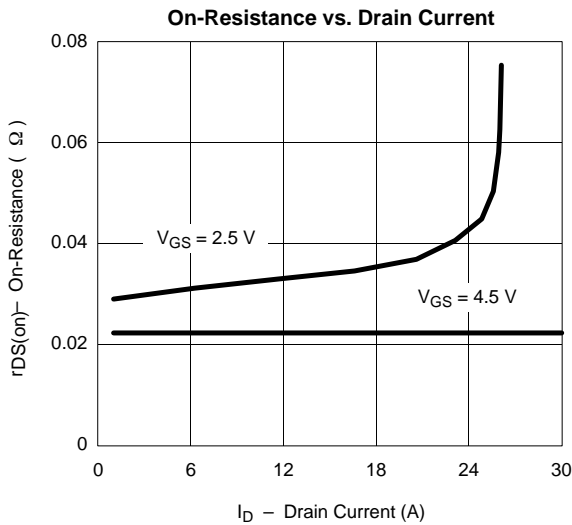
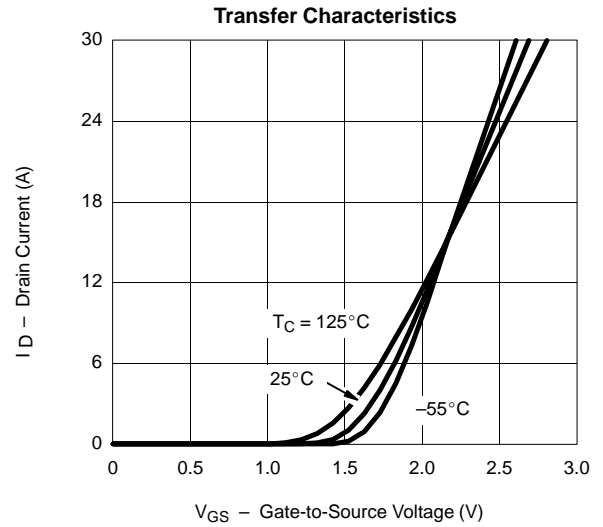
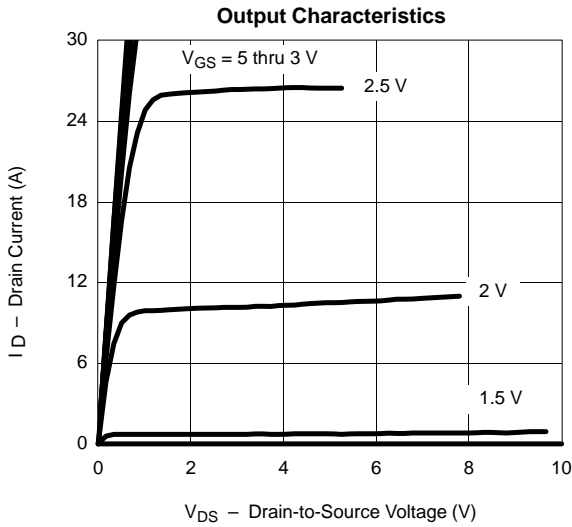
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.6			V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V	N-Ch P-Ch			±100 ±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V	P-Ch			-1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			25	
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			-25	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	30			A
		V <sub>DS</sub> ≥ -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-30			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.5 A	N-Ch		0.023	0.030	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.5 A	P-Ch		0.040	0.050	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.9 A	N-Ch		0.030	0.040	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.7 A	P-Ch		0.060	0.085	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.5 A	N-Ch		20		S
		V <sub>DS</sub> = -10 V, I <sub>D</sub> = -3.5 A	P-Ch		10		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.25 A, V <sub>GS</sub> = 0 V	N-Ch		0.65	1.2	V
		I <sub>S</sub> = -1.25 A, V <sub>GS</sub> = 0 V	P-Ch		0.72	-1.2	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.5 A  P-Channel V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.5 A	N-Ch		13	25	nC
Gate-Source Charge	Q <sub>gs</sub>		N-Ch		3.0		
Gate-Drain Charge	Q <sub>gd</sub>		P-Ch		3.5		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω  P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	N-Ch		22	50	ns
			P-Ch		27	50	
Rise Time	t <sub>r</sub>		N-Ch		40	80	
			P-Ch		30	60	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		50	100	
			P-Ch		57	100	
Fall Time	t <sub>f</sub>		N-Ch		20	40	
			P-Ch		21	40	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.25 A, di/dt = 100 A/μs	N-Ch		30	60	
		I <sub>F</sub> = -1.25 A, di/dt = 100 A/μs	P-Ch		60	100	

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



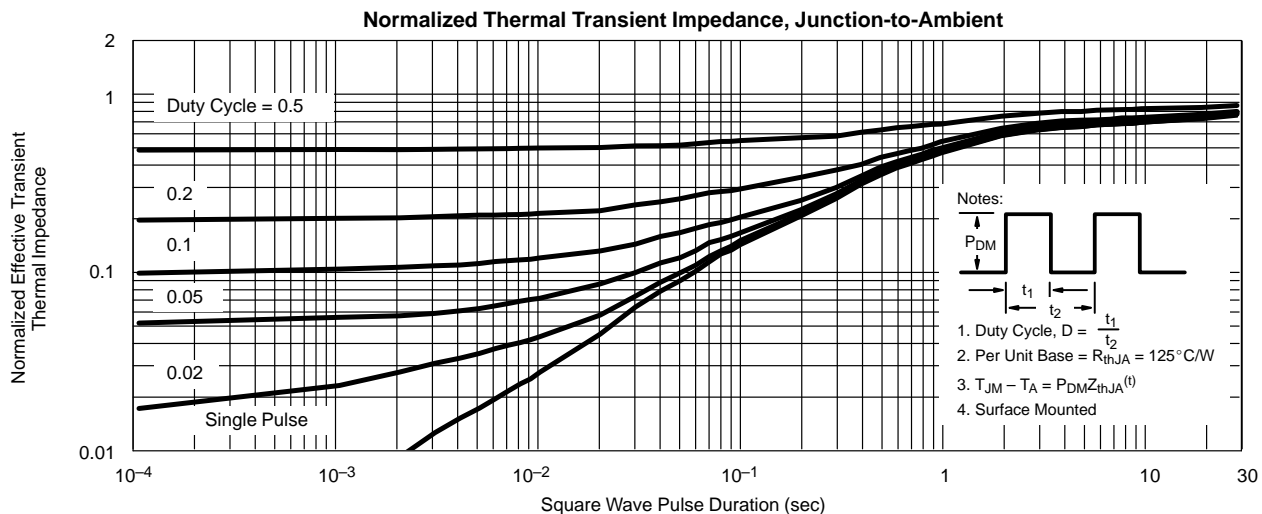
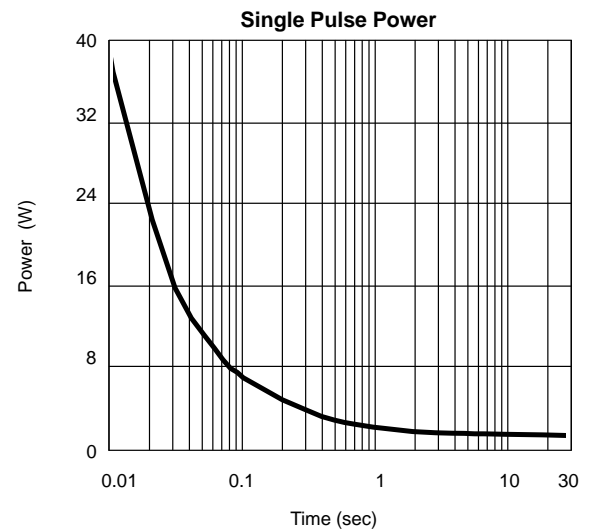
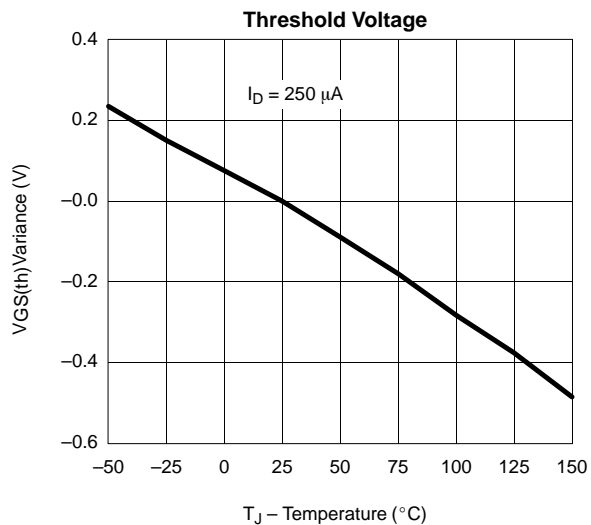
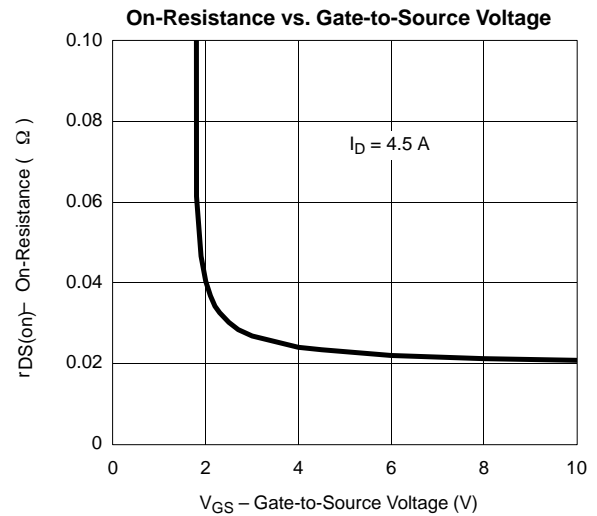
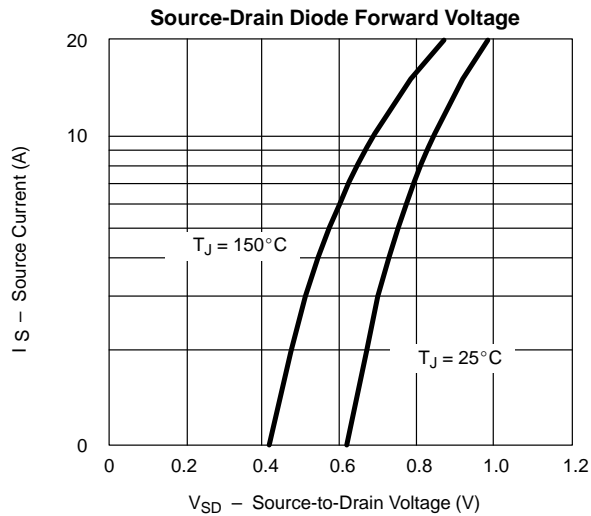
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL**





**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

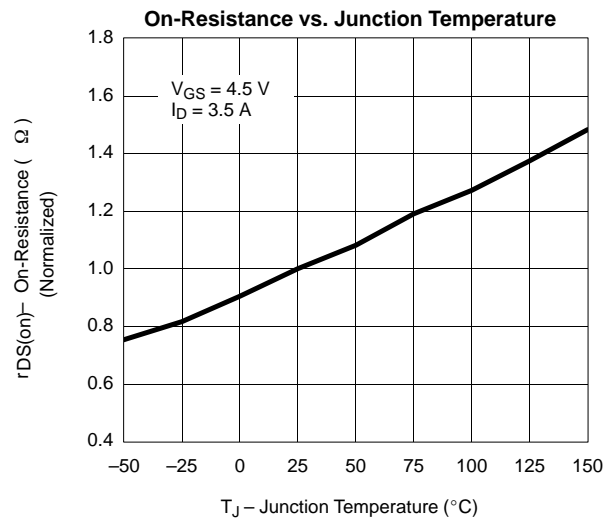
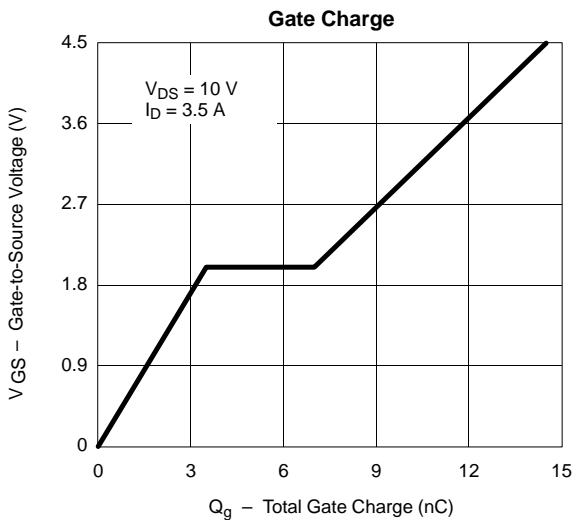
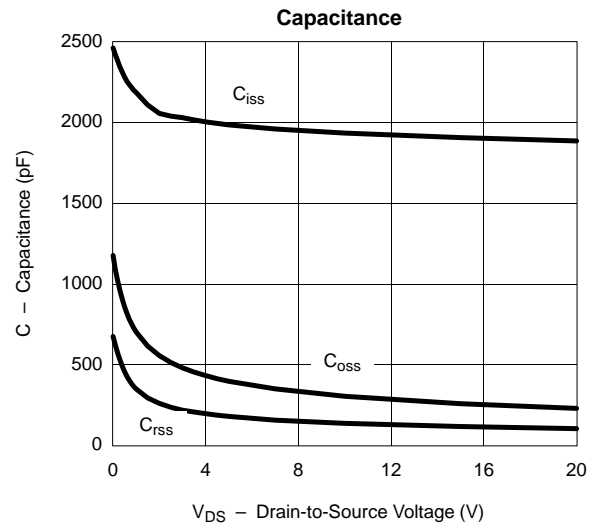
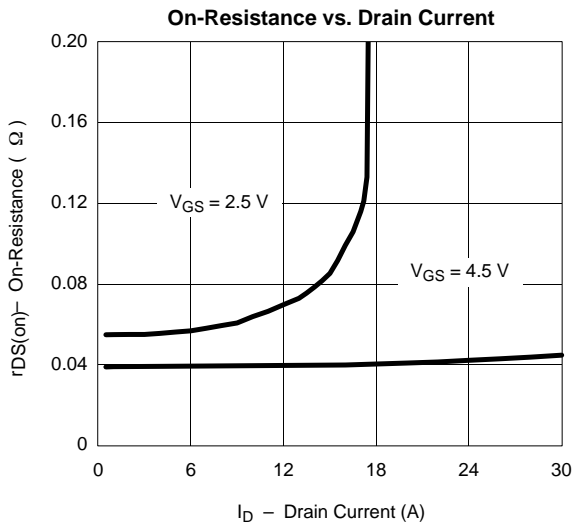
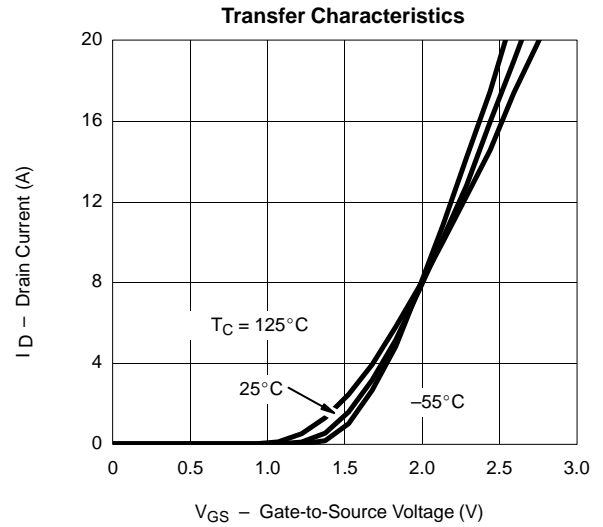
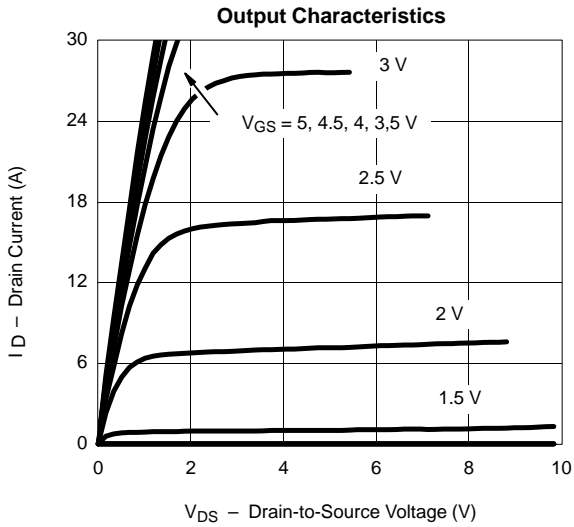
**N-CHANNEL**





**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**





### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

### P-CHANNEL

