N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
28	0.033 @ V_{GS} = 4.5 V	±4.6
	0.038 @ V_{GS} = 3.0 V	±4.3
	0.042 @ V_{GS} = 2.5 V	±4.1

ESD Protected
2000 V

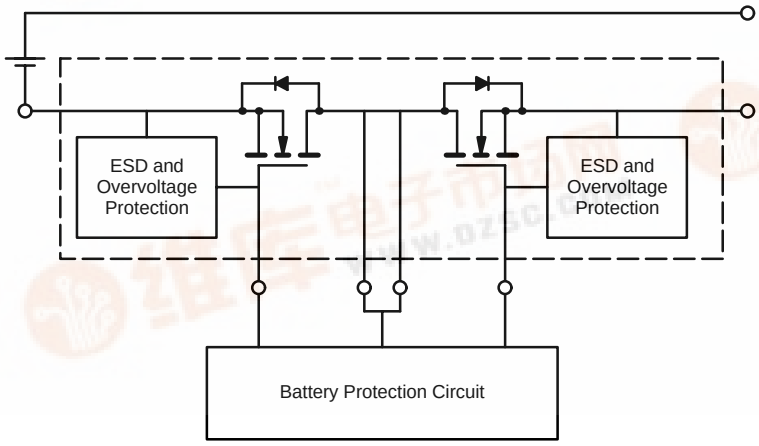
FEATURES

- Low $r_{DS(on)}$
- V_{GS} Max Rating: 14 V
- Exceeds 2-kV ESD Protection
- Low Profile TSSOP-8 Package
- $r_{DS(on)}$ Rating at 2.5-V V_{GS}
- 28-V V_{DS} Rated
- Symetrical Voltage Blocking (Off Voltage)

DESCRIPTION

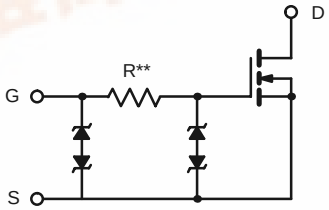
The Si6924EDQ is a dual n-channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain contsruction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second stage diode is designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA @ 14 V and the maximum t_{off} to 12 µs. The Si6924EDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5-V $r_{DS(on)}$ rating and a safe 14-V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance.

FIGURE 1. Typical Use In a Lithium Ion Battery Pack



**R typical value is 1.8 kΩ by design.

See Typical Characteristics, Gate-Current vs. Gate-Source Voltage, Page 3.

FIGURE 2. Input ESD and Overvoltage Protection Circuit.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

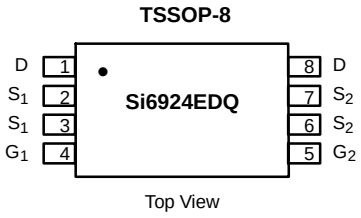
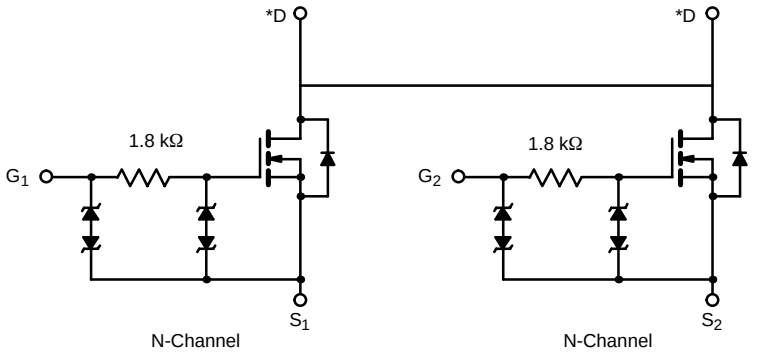


FIGURE 3.



*Thermal connection to drain pins is required to achieve specific performance.

FIGURE 4.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage, Source-Drain Voltage		V_{DS}	- to +	V
Gate-Source Voltage		V_{GS}	± 14	
Continuous Drain-to-Source Current (T_J = 150°C)[a, b]	T_A = 25°C	I_D	± 4.6	A
	T_A = 70°C		± 3.7	
Pulsed Drain-to-Source Current		I_{DM}	± 20	
Pulsed Source Current (Diode Conduction)[a, b]		I_S	1.25	
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	1.1	W
	T_A = 70°C		0.72	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}		125	°C/W
	Steady-State		115		

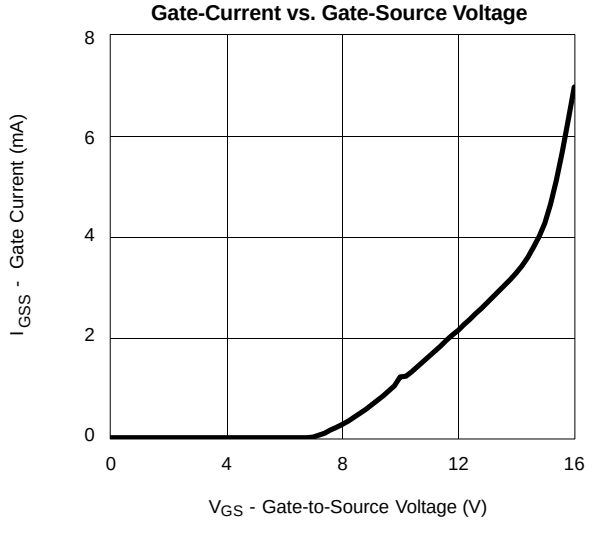
Notes
a. Surface Mounted on FR4 Board.
b. t ≤ 10 sec.

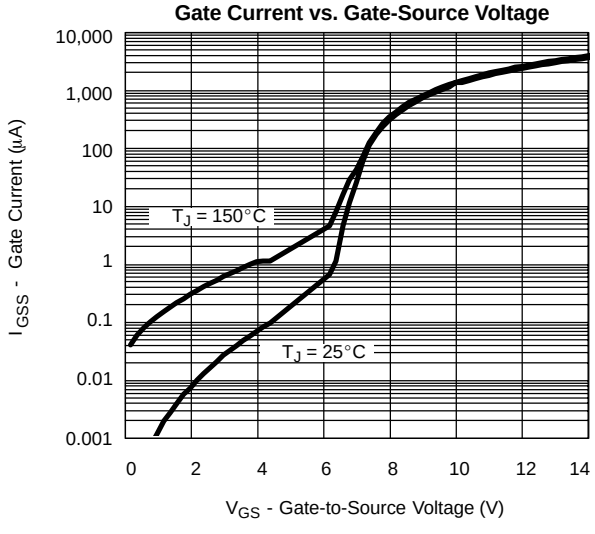
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	0.5			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±1	μA
		V_{DS} = 0 V, V_{GS} = ±14 V			±10	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 22.4 V, V_{GS} = 0 V			1	μA
		V_{DS} = 22.4 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 5 V	10			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.6 A		0.026	0.033	Ω
		V_{GS} = 3.0 V, I_D = 4.3 A		0.029	0.038	
		V_{GS} = 2.5 V, I_D = 4.1 A		0.031	0.042	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 4.6 A		18		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.7	1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.6 A		14	20	nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			4.2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		0.55	1.0	μs
Rise Time	t_r			2.0	4.0	
Turn-Off Delay Time	$t_{d(off)}$			7.0	12	
Fall Time	t_f			4.5	8	

Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

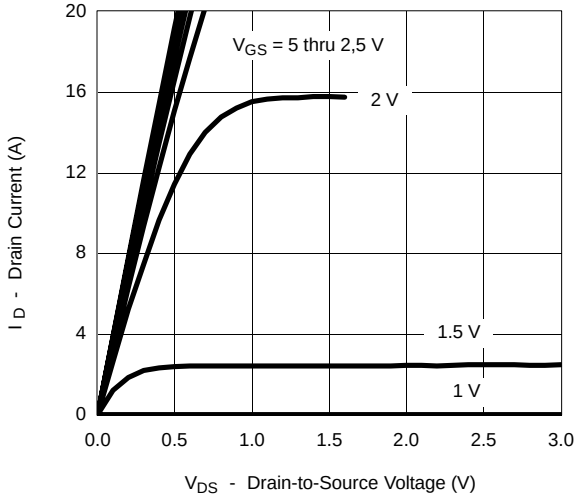
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



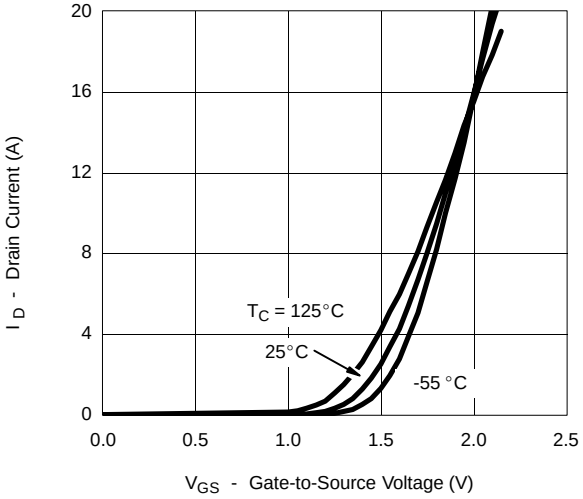


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

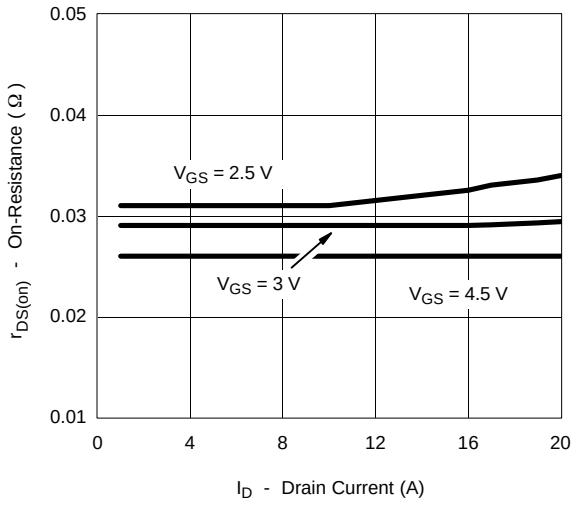
Output Characteristics



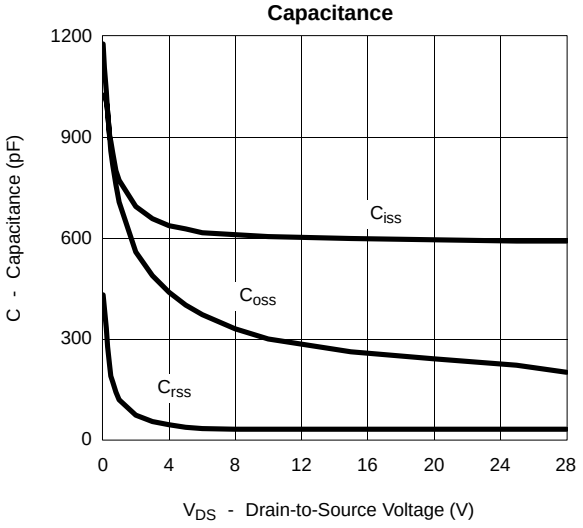
Transfer Characteristics



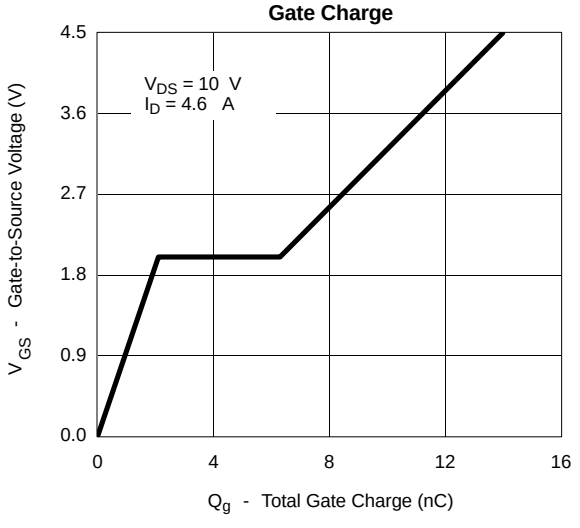
On-Resistance vs. Drain Current



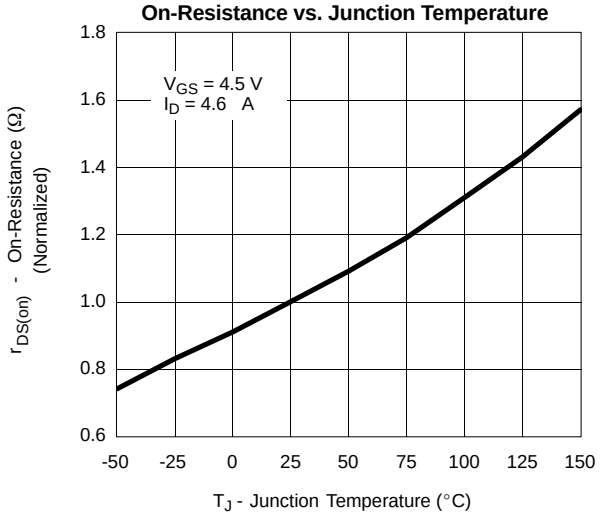
Capacitance



Gate Charge

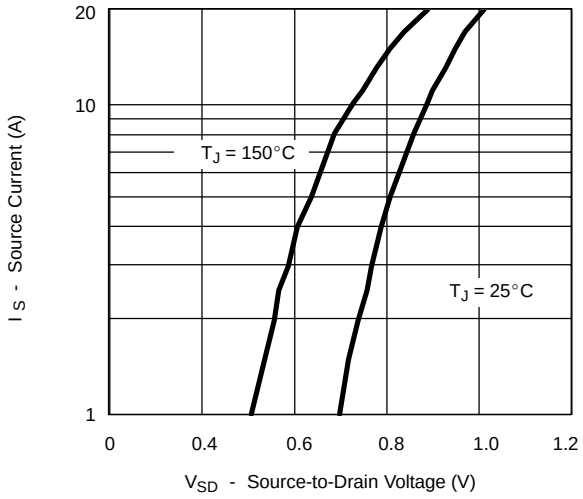


On-Resistance vs. Junction Temperature

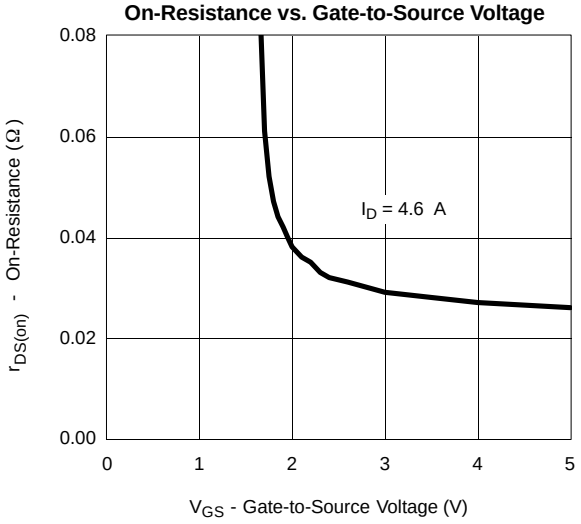


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

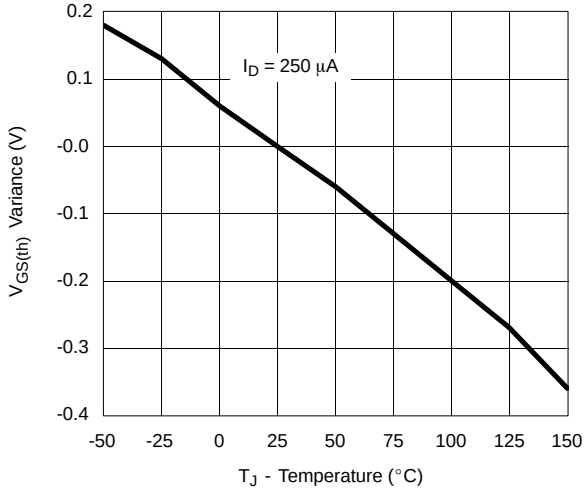
Source-Drain Diode Forward Voltage



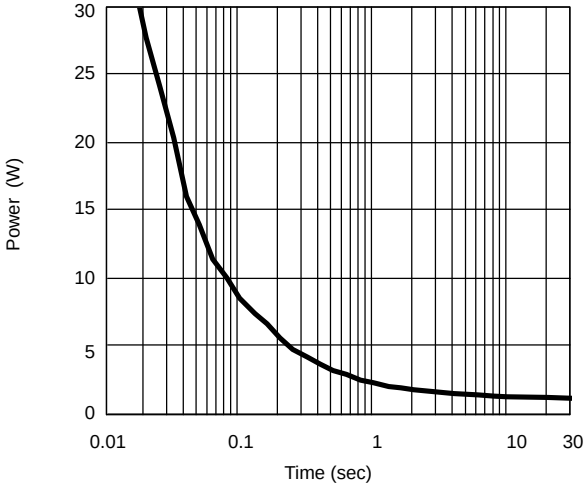
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient