# Dual N-Channel 2.5-V (G-S) MOSFET

## CHARACTERISTICS

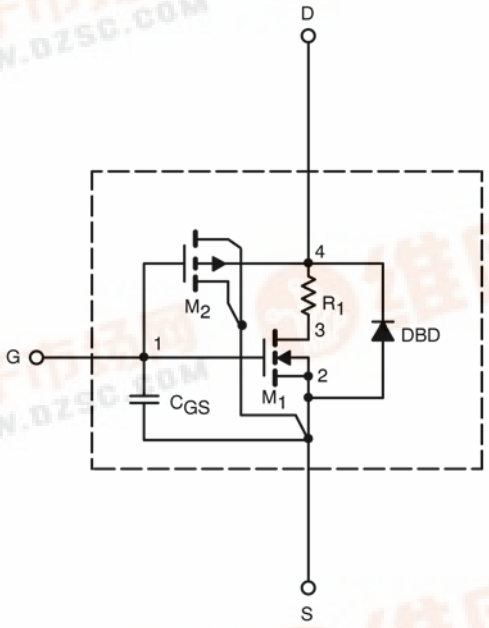
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the –55 to 125°C temperature ranges under the pulsed 0 to 5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

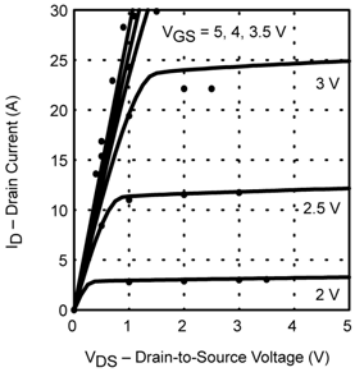
## SUBCIRCUIT MODEL SCHEMATIC

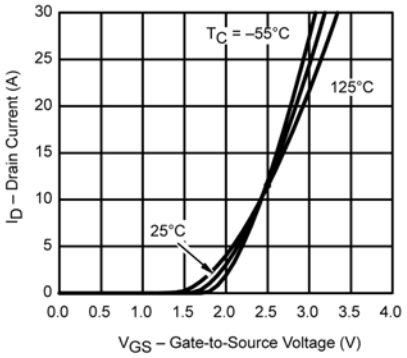


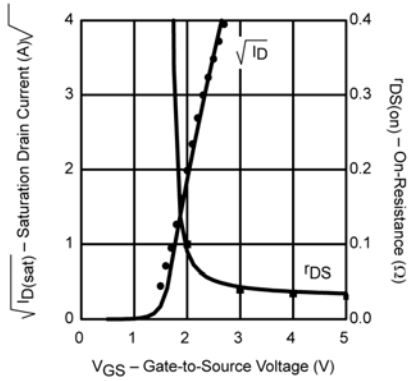
| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.1 | | V |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 4.5 V | 80 | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 3.9 A | 0.036 | 0.035 | Ω |
| | | $V_{GS}$ = 3 V, $I_D$ = 3.5 A | 0.043 | 0.042 | |
| | | $V_{GS}$ = 2.5 V, $I_D$ = 3 A | 0.052 | 0.050 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 3.9 A | 15 | 14 | S |
| Forward Voltage[a] | $V_{SD}$ | $I_S$ = 1 A, $V_{GS}$ = 0 V | 0.78 | 0.75 | V |
| **Dynamic[b]** | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 6 V, $V_{GS}$ = 4.5 V, $I_D$ = 3.9 A | 4 | 4 | nC |
| Gate-Source Charge | $Q_{gs}$ | | 0.90 | 0.90 | |
| Gate-Drain Charge | $Q_{gd}$ | | 1 | 1 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 6 V, $R_L$ = 6 Ω<br>$I_D \cong$ 1 A, $V_{GEN}$ = 4.5 V, $R_G$ = 6 Ω | 52 | 40 | ns |
| Rise Time | $t_r$ | | 28 | 50 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 25 | 20 | |
| Fall Time | $t_f$ | | 8 | 10 | |

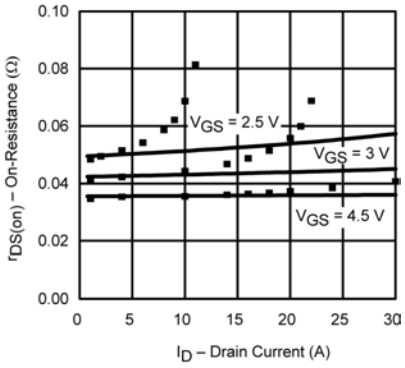
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

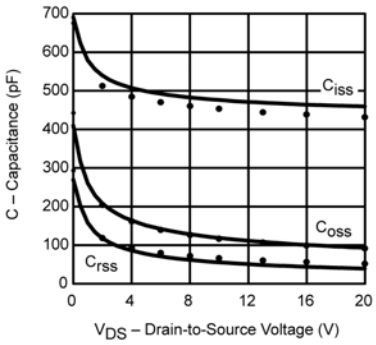
COMPARISON OF MODEL WITH MEASURED DATA ($T_J$=25°C UNLESS OTHERWISE NOTED)

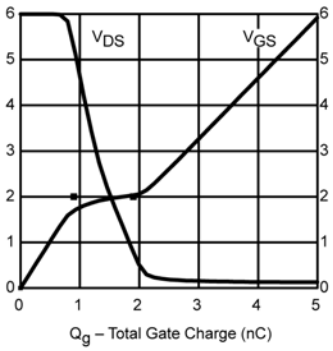



Note: Dots and squares represent measured data.