



# **Dual N-Channel 30-V (D-S) MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$r_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)		
30	0.036 @ V <sub>GS</sub> = 10 V	6.8	7		
	0.039 @ V <sub>GS</sub> = 4.5 V	6.6	,		

#### **FEATURES**

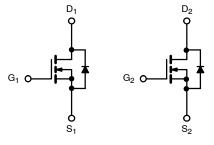
- TrenchFET® Gen II Power MOSFET
- 100% R<sub>q</sub> Tested
- Space Savings Optimized for Fast Switching



RoHS

#### **APPLICATIONS**

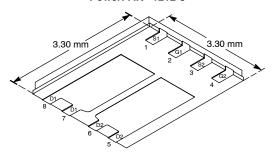
- Synchronous Rectification
- Intermediate Driver



N-Channel MOSFET

N-Channel MOSFET

#### PowerPAK® 1212-8



Ordering Information: Si7212DN-T1—E3 (Lead (Pb)-Free)

**Bottom View** 

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30		٧	
Gate-Source Voltage		$V_{GS}$	±12			
O II D : O I T 150000	T <sub>A</sub> = 25°C	I <sub>D</sub>	6.8	4.9	А	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	T <sub>A</sub> = 85°C		4.9	3.5		
Pulsed Drain Current		I <sub>DM</sub>	20			
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	2.2	1.1	А	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25°C		2.6	1.3		
	T <sub>A</sub> = 85°C	P <sub>D</sub>	1.4	0.69	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	–55 to 150			
Soldering Recommendations (Peak Temperature) <sup>b,c</sup>				260	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 10 sec	R <sub>thJA</sub>	38	48	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		77	94		
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	4.3	5.4		

#### Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

# **Vishay Siliconix**



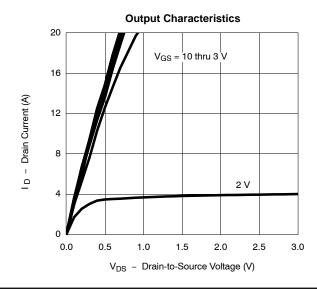
Parameter	Symbol	Test Condition	Min	Тур	Max	Unit	
Static	<b>.</b>		•				
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.6		1.6	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = $\pm 20$ V			±100	nA	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	_	
	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			5	<b>μA</b>	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-State Resistancea		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.8 A		0.030	0.036	Ω	
Dialif-Source Oil-State nesistance	r <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 6.6 \text{ A}$		0.032	0.039	1 32	
Forward Transconductancea	9fs	$V_{DS} = 10 \text{ V}, I_D = 6.8 \text{ A}$		20		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.2 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_g$			7	11		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 6.8 A		2		пC	
Gate-Drain Charge	$Q_{gd}$			1.7			
Gate Resistance	$R_g$	f = 1 MHz	1.5	3.0	4.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		12	20	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		30	45		
Fall Time	t <sub>f</sub>			10	15		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.2 A, di/dt = 100 A/μs		15	30		

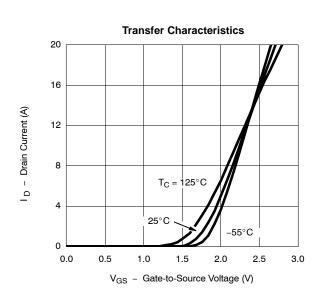
#### Notes

- Pulse test; pulse width  $\leq 300 \,\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



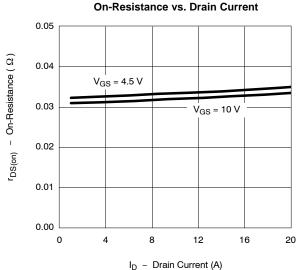




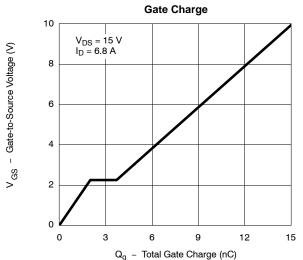


# Vishay Siliconix

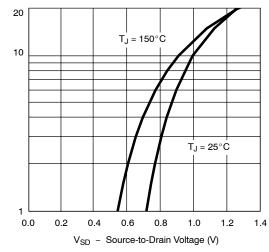
## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



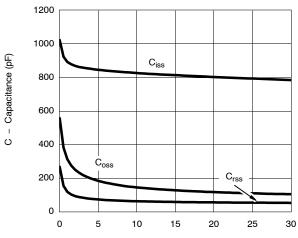




Source-Drain Diode Forward Voltage

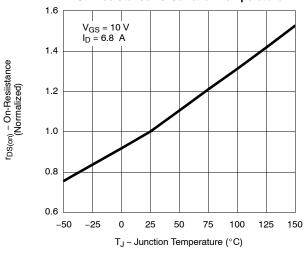


Capacitance

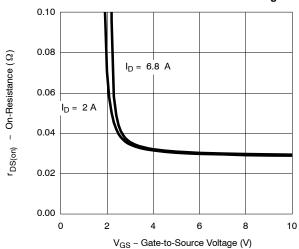


V<sub>DS</sub> - Drain-to-Source Voltage (V)

#### On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

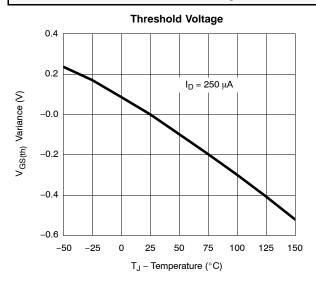


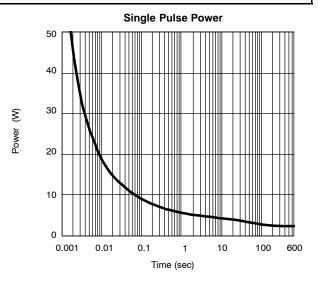
Source Current (A)

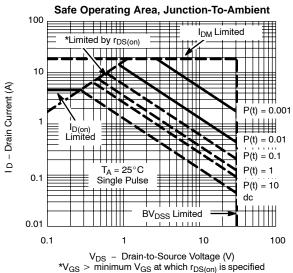
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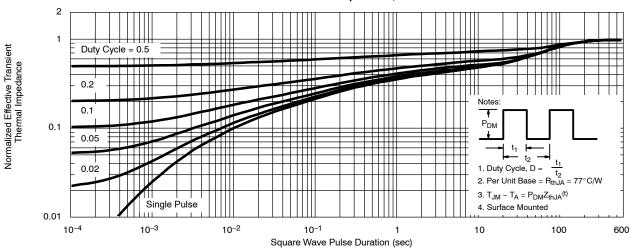
## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)







#### Normalized Thermal Transient Impedance, Junction-to-Ambient





## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

## Normalized Thermal Transient Impedance, Junction-to-Case 2 1 Normalized Effective Transient Thermal Impedance Duty Cycle = 0.5 0.2 0.1 0.1 0.02 Single Pulse 0.01 10-4 10-2 10<sup>-3</sup> 10<sup>-1</sup> Square Wave Pulse Duration (sec)

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