



New Product

Si7388DP
Vishay Siliconix

N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY

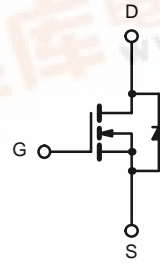
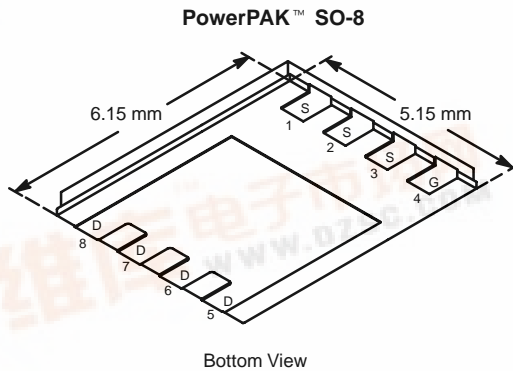
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.007 @ $V_{GS} = 10$ V	19
	0.010 @ $V_{GS} = 4.5$ V	15

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile

APPLICATIONS

- DC/DC Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	19	12	A
	$T_A = 70^\circ\text{C}$		15	9	
Pulsed Drain Current		I_{DM}	± 50		
Continuous Source Current (Diode Conduction) ^a		I_S	4.1	1.6	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5	1.9	W
	$T_A = 70^\circ\text{C}$		3.2	1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^a	$t \leq 10$ sec	R_{thJA}	20	25	$^\circ\text{C/W}$
	Steady State		55	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.0	2.6	

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.

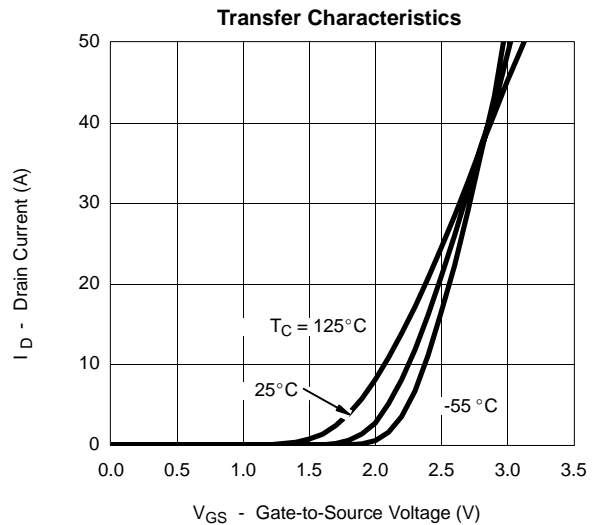
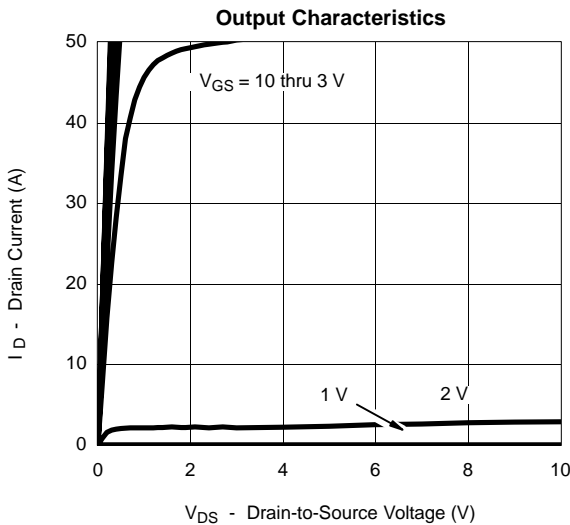


MOSFET SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.80		1.6	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 70 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 19 A		0.0058	0.007	Ω
		V _{GS} = 4.5 V, I _D = 15 A		0.008	0.010	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 19 A		40		S
Diode Forward Voltage ^a	V _{SD}	I _S = 4.1 A, V _{GS} = 0 V		0.75	1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 5.0 V, I _D = 19 A		16.3	24	nC
Gate-Source Charge	Q _{gs}			4		
Gate-Drain Charge	Q _{gd}			5.9		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D = 1 A, V _{GEN} = 10 V, R _G = 6 Ω		14	20	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			44	70	
Fall Time	t _f			20	30	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3 A, di/dt = 100 A/μs		40	70	

Notes

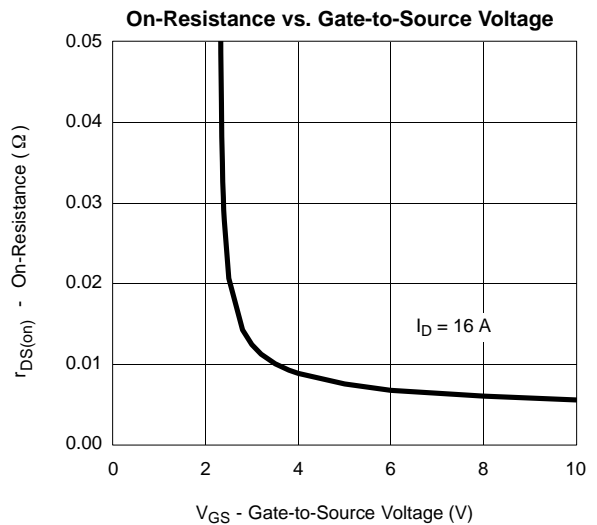
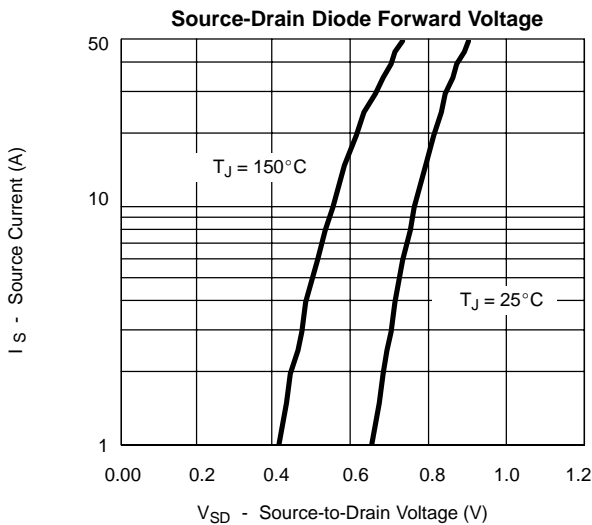
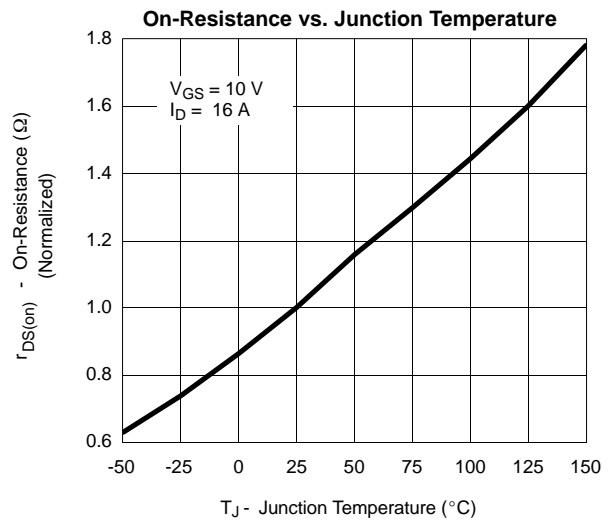
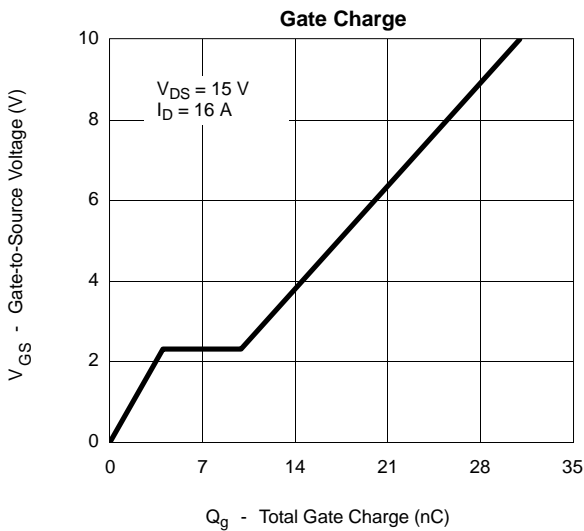
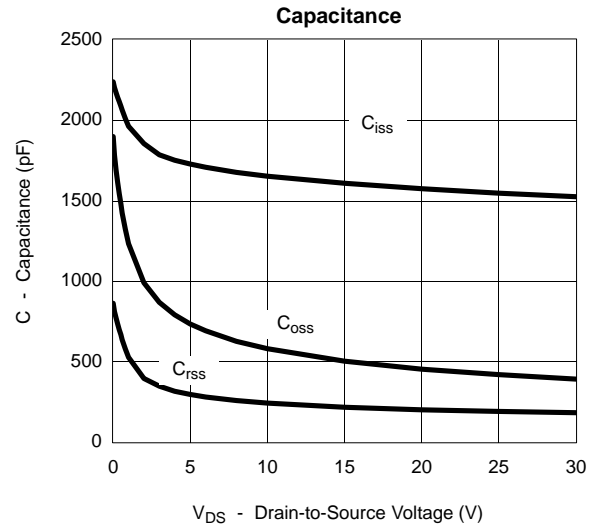
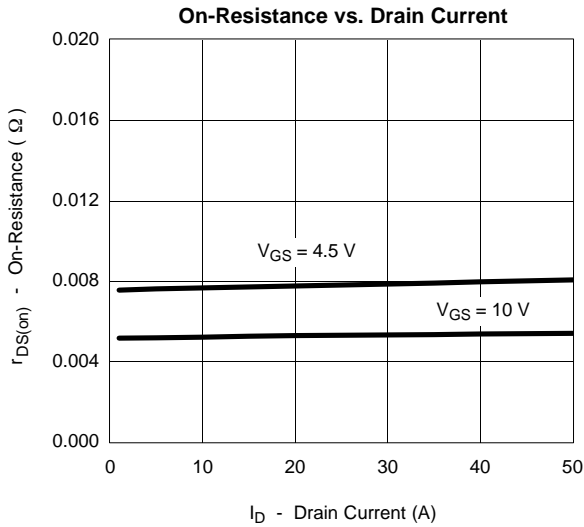
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



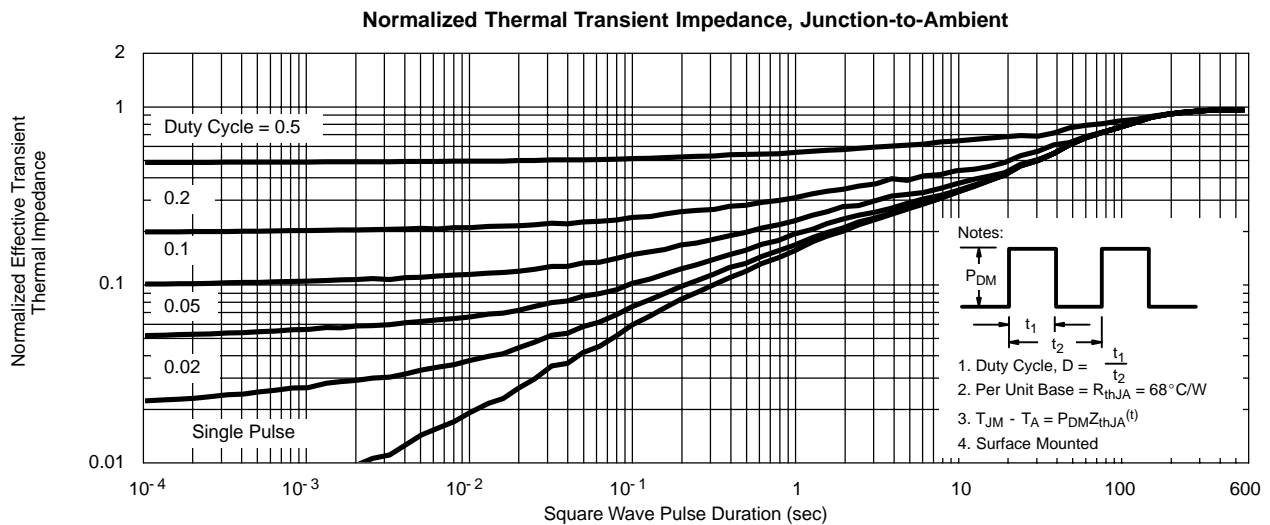
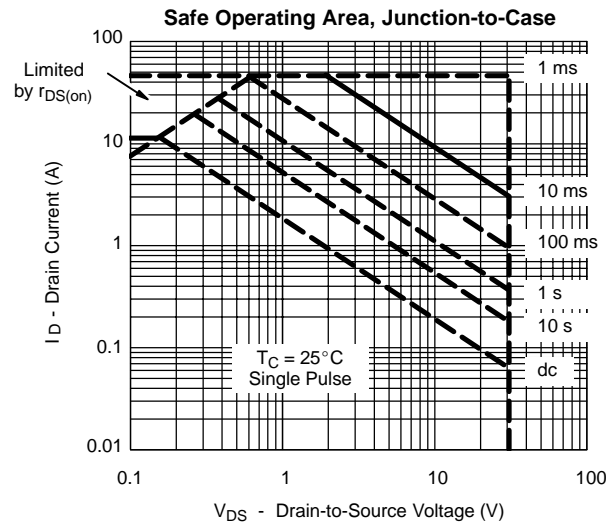
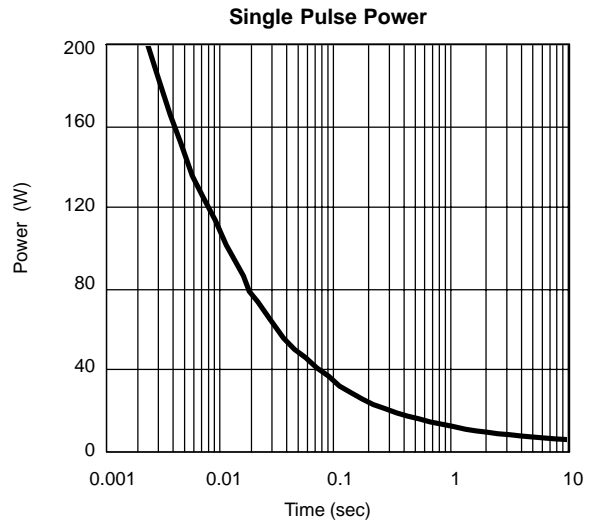
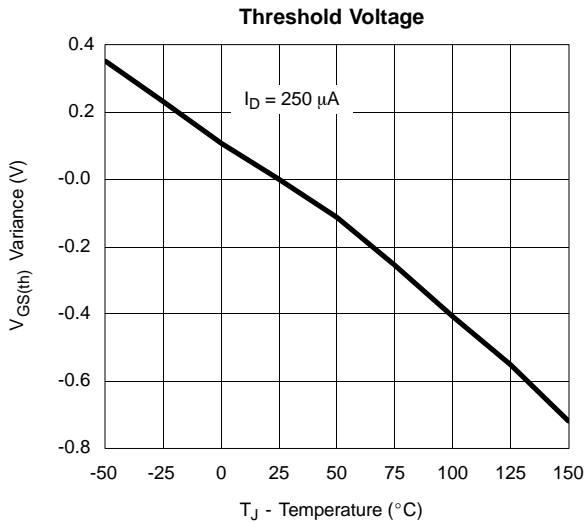


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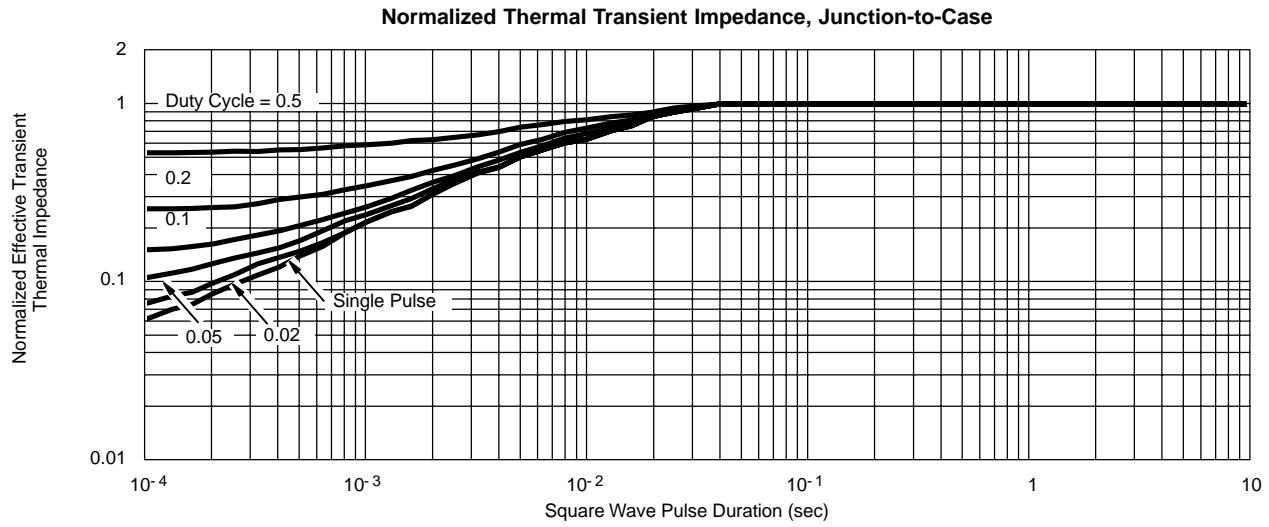




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