

SPICE Device Model Si7840BDP Vishay Siliconix

N-Channel 30-V (D-S) Fast Switching MOSFET

CHARACTERISTICS

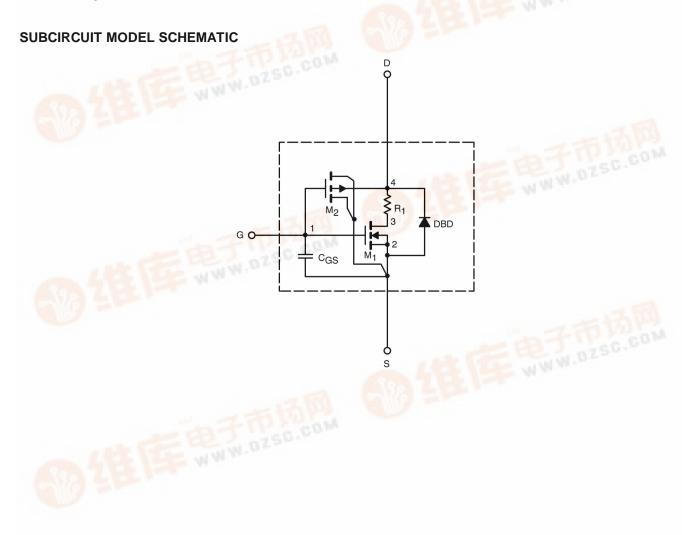
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{qd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.



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This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



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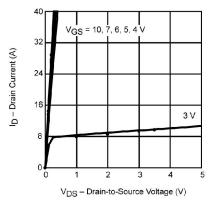
SPECIFICATIONS (T _J = 25° C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},\ I_{D}=250\ \mu A$	1.8		V
On-State Drain Current ^a	I _{D(on)}	$V_{\text{DS}} \geq 5 \text{ V}, V_{\text{GS}} = 10 \text{ V}$	684		А
Drain-Source On-State Resistance ^a	r	V_{GS} = 10 V, I_{D} = 16.5 A	0.0070	0.0070	Ω
	r _{DS(on)}	$V_{GS}=4.5~V,~I_D=13~A$	0.0084	0.0084	
Forward Transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 16.5 \text{ A}$	17	60	S
Diode Forward Voltage ^a	V _{SD}	$I_{\rm S} = 3.7$ A, $V_{\rm GS} = 0$ V	0.74	0.75	V
Dynamic ^b					
Total Gate Charge	Qg	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{D} = 16.5 A	13	14	nC
Gate-Source Charge	Q _{gs}		6	6	
Gate-Drain Charge	Q _{gd}		3.5	3.5	

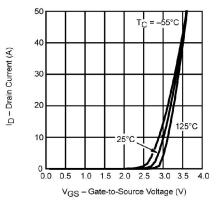
Notes a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

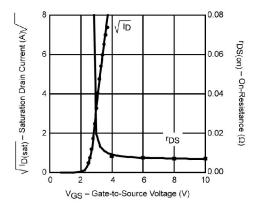


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COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

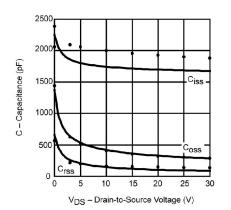


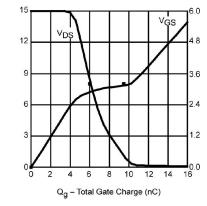




0.012 0.01 0.010 0.009 4.5 GS 0.008 V_{GS} = 10 V 0.00 0.006 0.005 0.004 L 5 10 15 20 25 30 35 40 I_D – Drain Current (A)

 $rDS(on) - On-Resistance (\Omega)$





Note: Dots and squares represent measured data