



New Product

Si7852DP  
Vishay Siliconix

## N-Channel 80-V (D-S) MOSFET

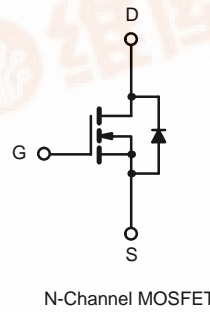
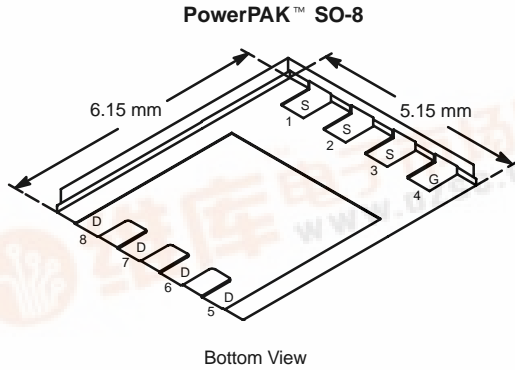
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
80	0.0165 @ $V_{GS} = 10$ V	12.5
	0.022 @ $V_{GS} = 6$ V	10.9

### FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching

### APPLICATIONS

- Primary Side Switch for DC/DC Applications



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		$V_{DS}$	80		V
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	12.5	7.6	A
	$T_A = 70^\circ\text{C}$		10.0	6.1	
Pulsed Drain Current		$I_{DM}$	50		
Avalanch Current		$I_{AS}$	40		
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	4.7	1.7	
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	5.2	1.9	W
	$T_A = 70^\circ\text{C}$		3.3	1.2	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$	19	24	$^\circ\text{C/W}$
	Steady State		52	65	
Maximum Junction-to-Case (Drain)		$R_{thJC}$	1.5	1.8	

Notes:  
a. Surface Mounted on 1" x 1" FR4 Board.



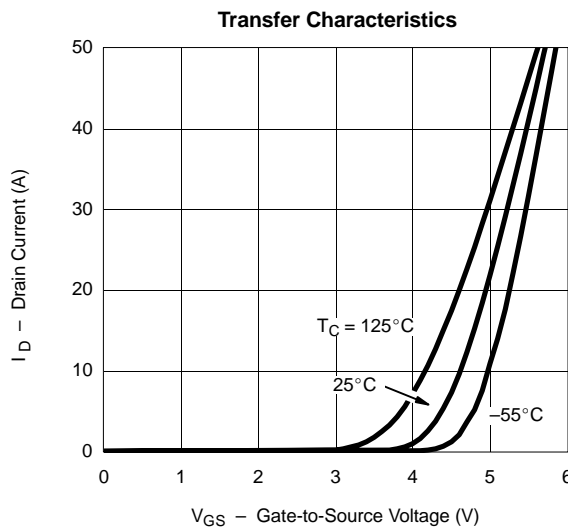
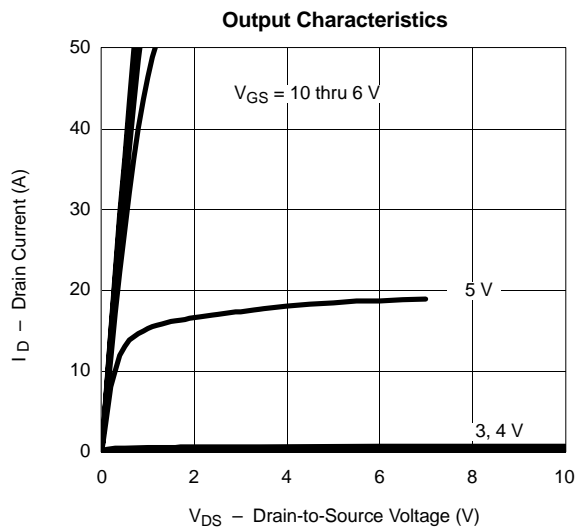
### SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.0135	0.0165	Ω
		V <sub>GS</sub> = 6.0 V, I <sub>D</sub> = 8.0 A		0.0175	0.022	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		25		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.8 A, V <sub>GS</sub> = 0 V		0.75	1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		34	41	nC
Gate-Source Charge	Q <sub>gs</sub>			7.5		
Gate-Drain Charge	Q <sub>gd</sub>			11.0		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 40 Ω I <sub>D</sub> ≅ 1.0 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		17	25	ns
Rise Time	t <sub>r</sub>			11	17	
Turn-Off Delay Time	t <sub>d(off)</sub>			40	60	
Fall Time	t <sub>f</sub>			31	45	
Gate Resistance	R <sub>g</sub>			0.85		Ω
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.8 A, di/dt = 100 A/μs		45	75	ns

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

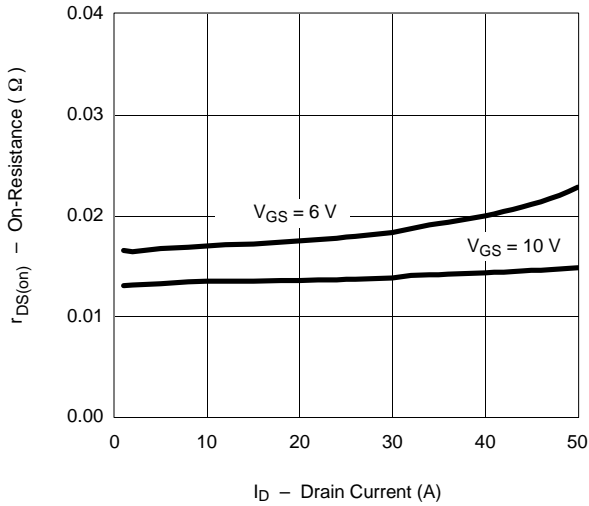
### TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



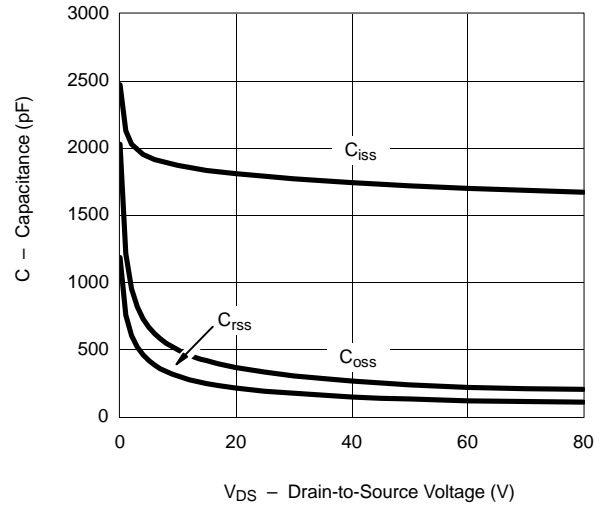


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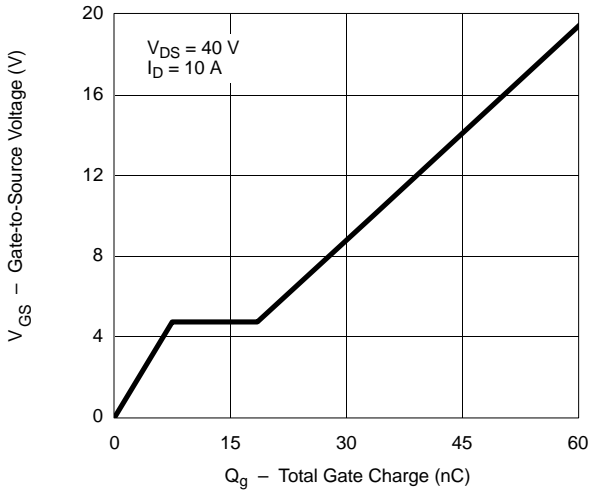
On-Resistance vs. Drain Current



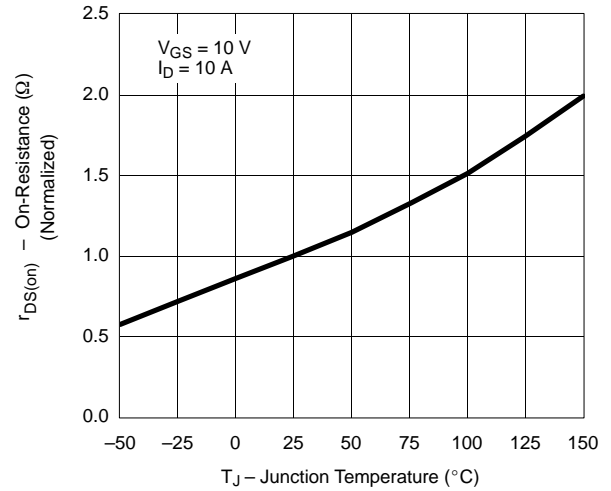
Capacitance



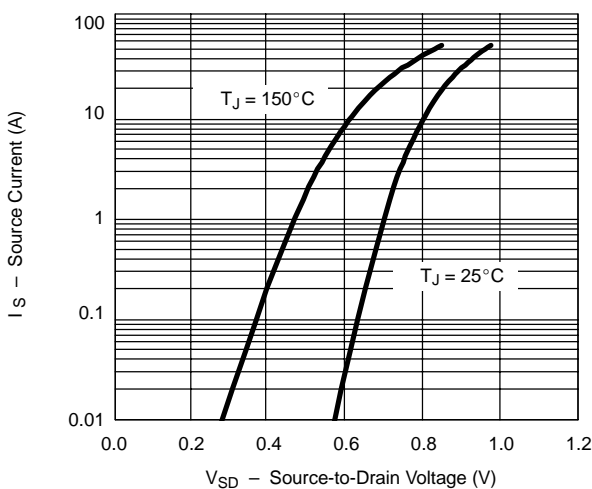
Gate Charge



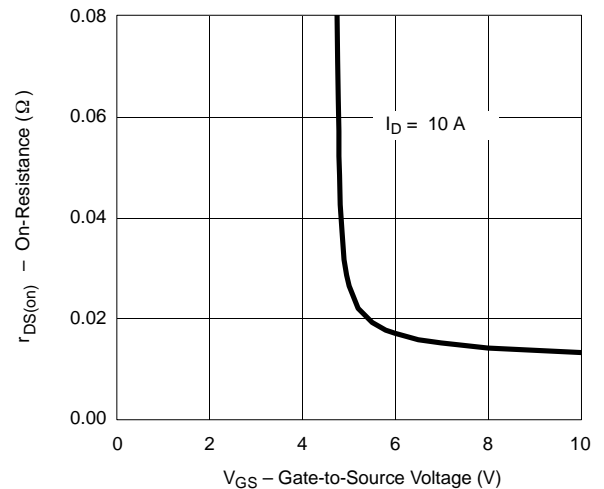
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

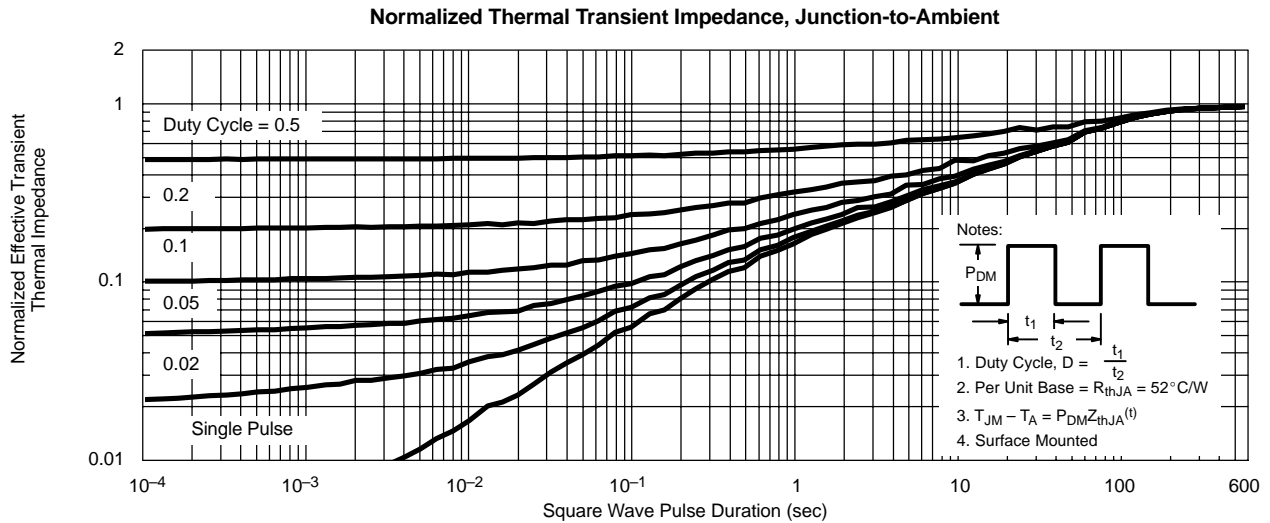
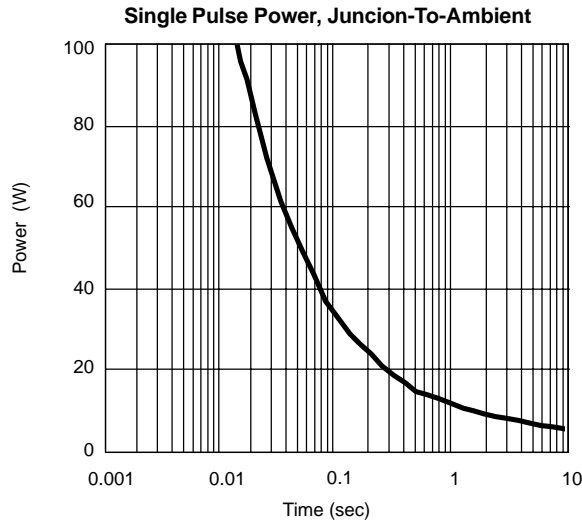
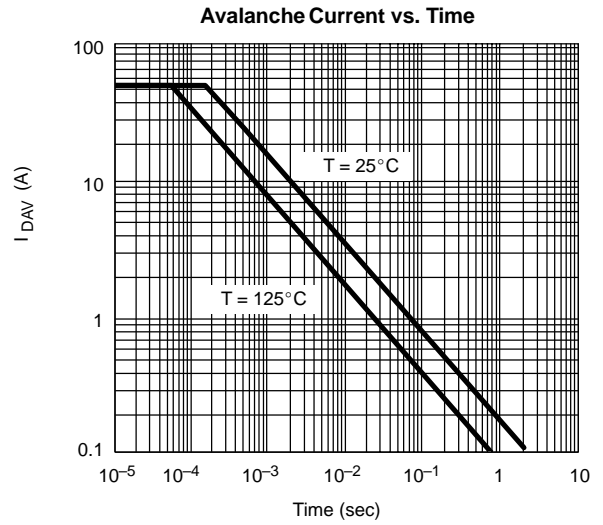
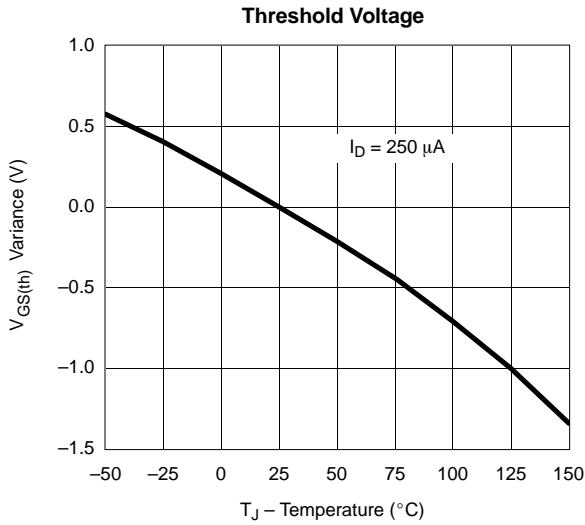


On-Resistance vs. Gate-to-Source Voltage





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