



New Product

Si7970DP
Vishay Siliconix

Dual N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
40	0.019 @ $V_{GS} = 10$ V	10.2
	0.026 @ $V_{GS} = 4.5$ V	8.7

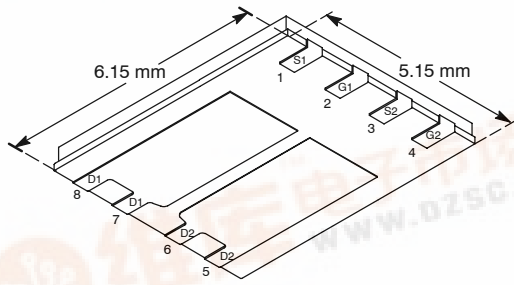
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings
- 100% R_g Tested

APPLICATIONS

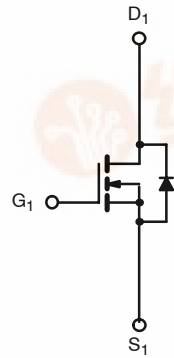
- Primary Side Switch
 - Low Power Quarter Buck
- Intermediate BUS Switch

PowerPAK SO-8

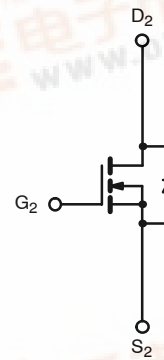


Bottom View

Ordering Information: Si7970DP-T1—E3



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	40		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	10.2	6.5	A
		$T_A = 70^\circ\text{C}$	8.2	5.2	
Pulsed Drain Current	I_{DM}	40			
Continuous Source Current (Diode Conduction) ^a	I_S	2.9	1.2		
Single Avalanche Current	I_{AS}	30			
Single Avalanche Energy		E_{AS}	45		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.5	1.4	W
		$T_A = 70^\circ\text{C}$	2.2	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	35	$^\circ\text{C/W}$
		Steady State	60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.2	2.7		

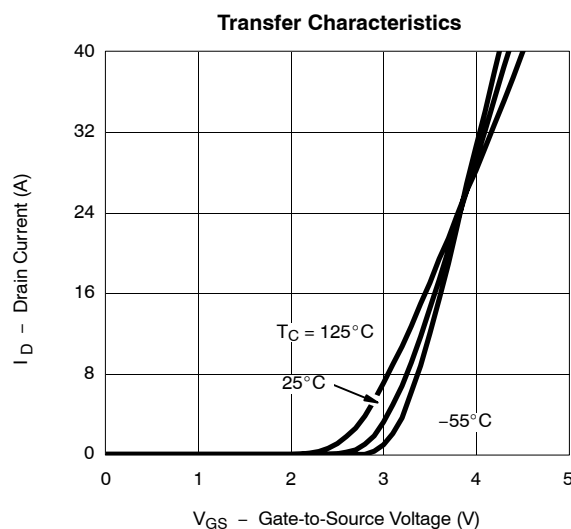
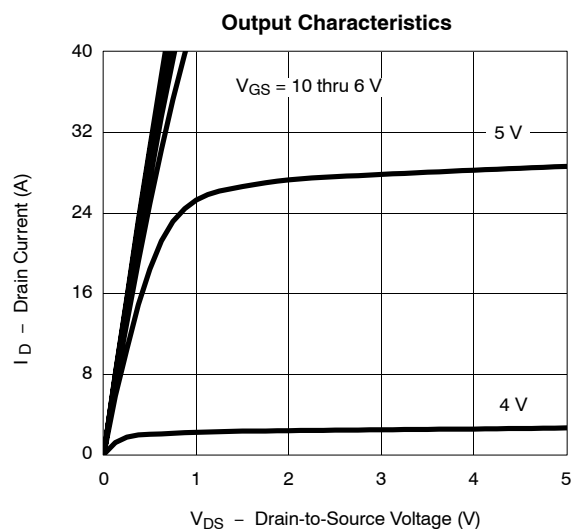
Notes:
a. Surface Mounted on 1" x 1" FR4 Board.


SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 10.2 A		0.016	0.019	Ω
		V _{GS} = 4.5 V, I _D = 8.7 A		0.021	0.026	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10.2 A		26		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 10.2 A		23	35	nC
Gate-Source Charge	Q _{gs}			4.4		
Gate-Drain Charge	Q _{gd}			5.6		
Gate Resistance	R _g	f = 1 MHz	1	2.3	3.9	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 20 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		15	25	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			50	75	
Fall Time	t _f			16	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, di/dt = 100 A/μs		30	60	

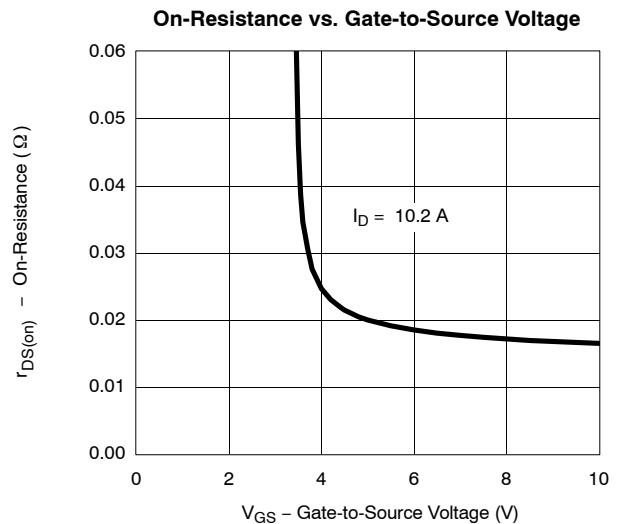
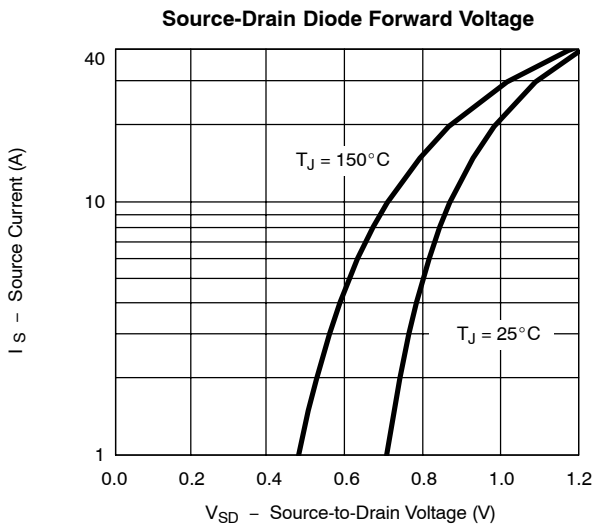
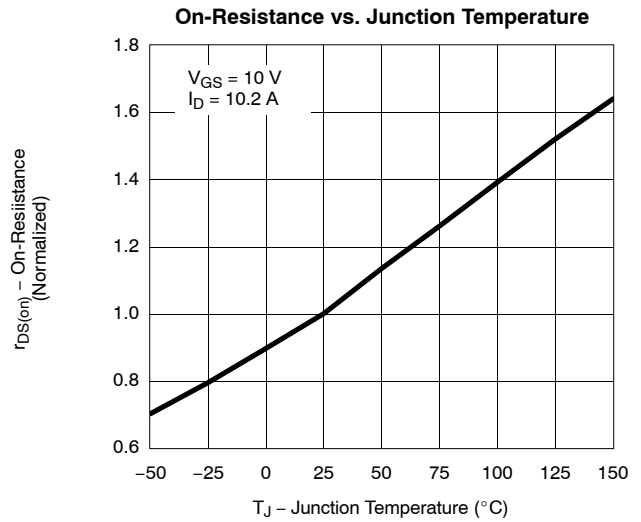
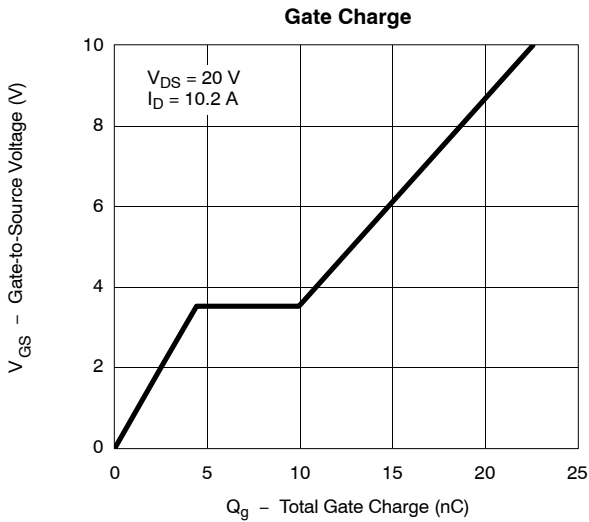
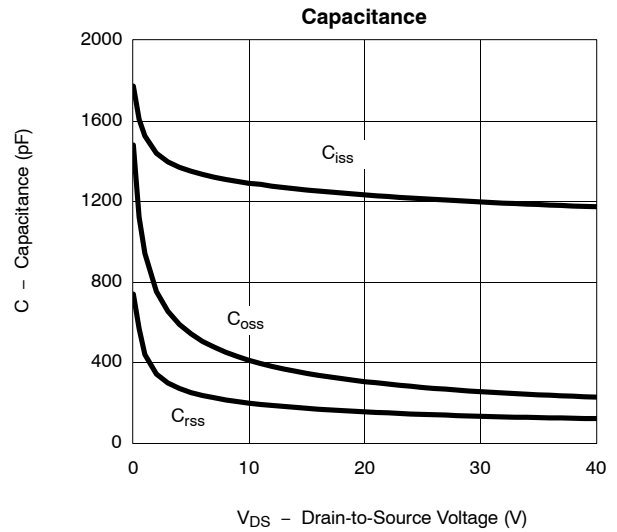
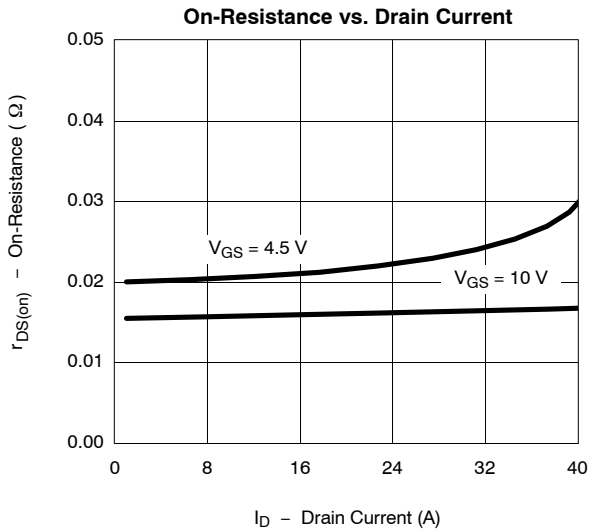
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
 b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)


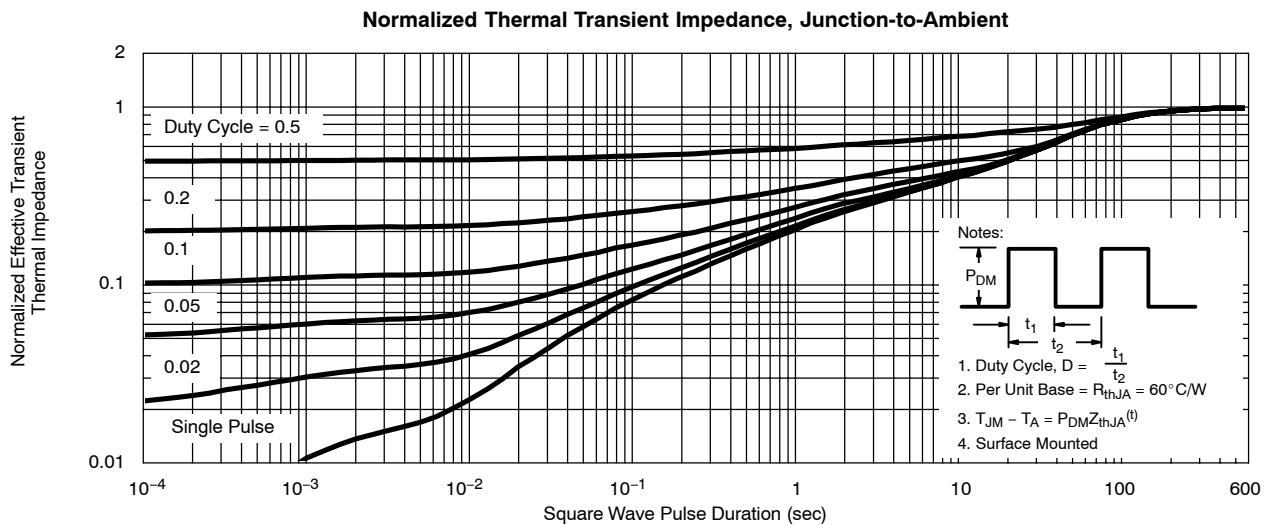
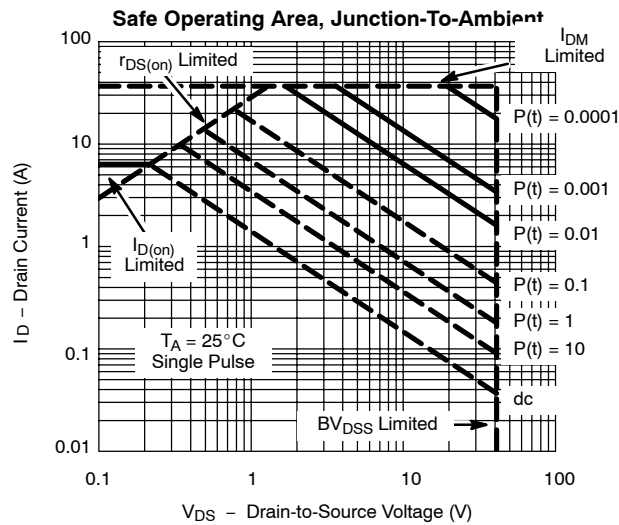
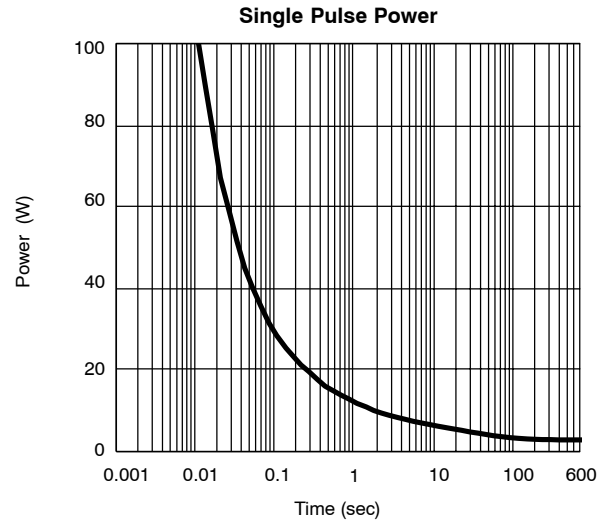
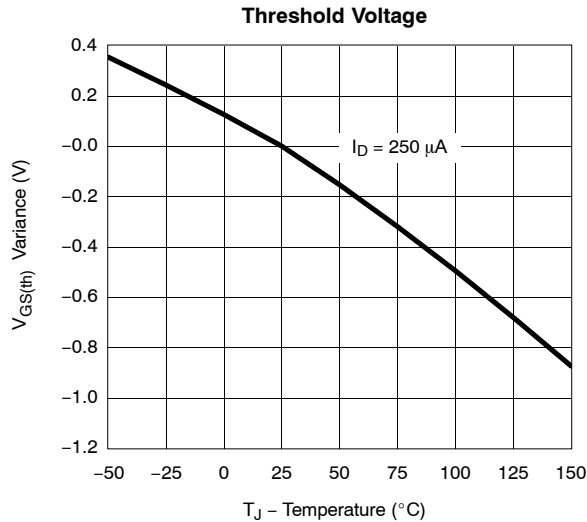


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