



SPICE Device Model Si7423DN Vishay Siliconix

P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

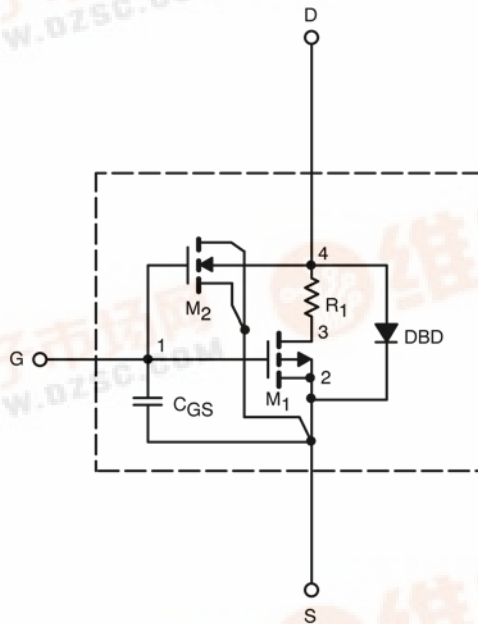
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	1.8		V
On-State Drain Current ^b	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	60		A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = -11.7 A	0.014	0.014	Ω
		V _{GS} = -4.5 V, I _D = -9 A	0.023	0.023	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -11.7 A	29	29	S
Diode Forward Voltage ^b	V _{SD}	I _S = -3.2 A, V _{GS} = 0 V	-0.83	-0.76	V
Dynamic^a					
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -10 V, I _D = -11.7 A	34	37.5	nC
Gate-Source Charge	Q _{gs}		5.8	5.8	
Gate-Drain Charge	Q _{gd}		9.6	9.6	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	15	11	ns
Rise Time	t _r		11	10	
Turn-Off Delay Time	t _{d(off)}		72	74	
Fall Time	t _f		25	50	

Notes

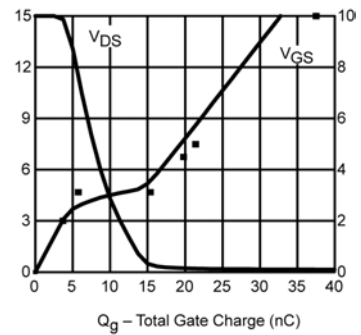
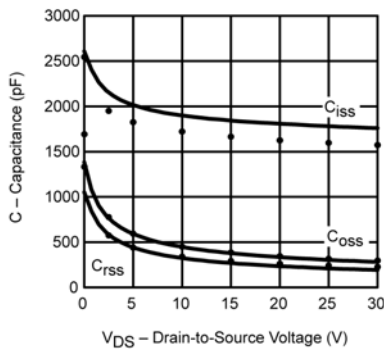
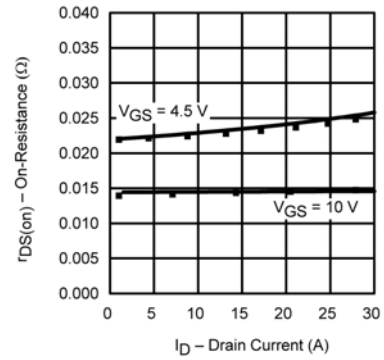
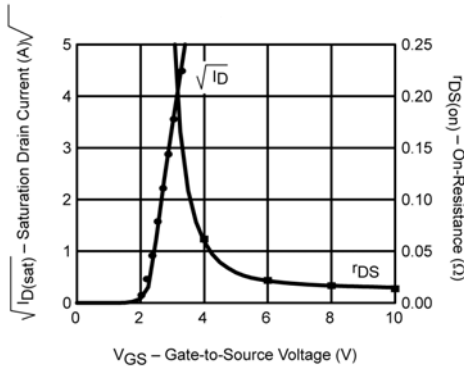
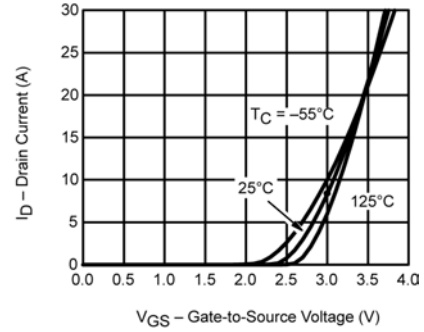
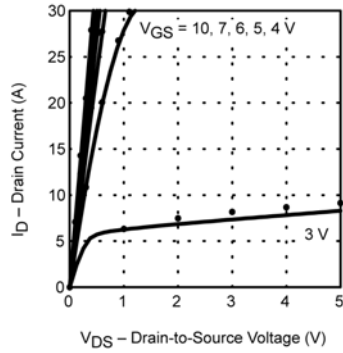
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.