



New Product

Si7810DN
Vishay Siliconix

N-Channel 100-V (D-S) MOSFET

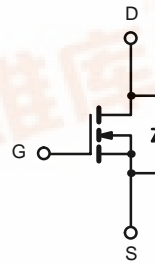
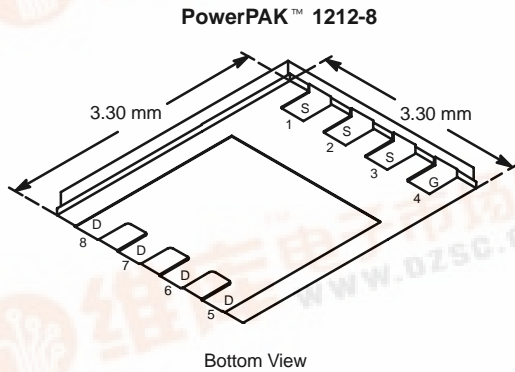
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.062 @ $V_{GS} = 10$ V	5.4
	0.084 @ $V_{GS} = 6$ V	4.6

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance
- PowerPAK™ 1212-8 Package with Low 1.07-mm-Profile
- PWM Optimized

APPLICATIONS

- Primary Side Switch
- In-Rush Current Limiter



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	100		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	5.4	3.4	A
		$T_A = 70^\circ\text{C}$	4.3	2.8	
Pulsed Drain Current	I_{DM}	20			
Continuous Source Current (Diode Conduction) ^a	I_S	3.2	1.3		
Single Avalanche Current	I_{AS}	19		mJ	
Single Avalanche Energy		E_{AS}	18		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	3.8	1.5	W
		$T_A = 70^\circ\text{C}$	2.0	0.8	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	26	33	$^\circ\text{C/W}$
		Steady State	65	81	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.9	2.4		

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.

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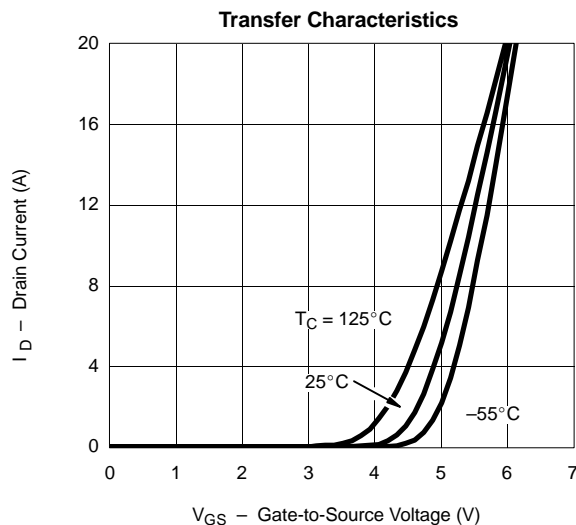
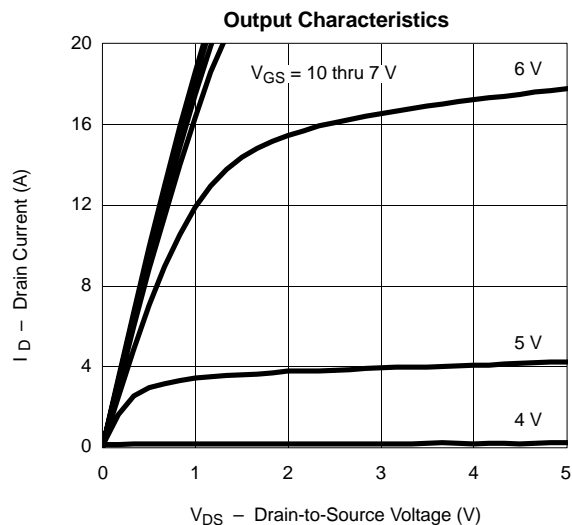
MOSFET SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55°C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5.4 A		0.052	0.062	Ω
		V _{GS} = 6 V, I _D = 4.6 A		0.070	0.084	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.4 A		12		S
Diode Forward Voltage ^a	V _{SD}	I _S = 3.2 A, V _{GS} = 0 V		0.78	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 5.4 A		13.5	17	nC
Gate-Source Charge	Q _{gs}			3		
Gate-Drain Charge	Q _{gd}			4.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		10	15	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			15	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3.2 A, di/dt = 100 A/μs		45	90	

Notes

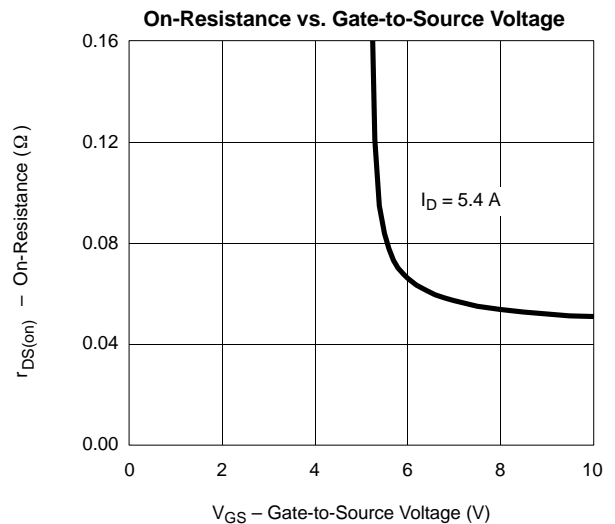
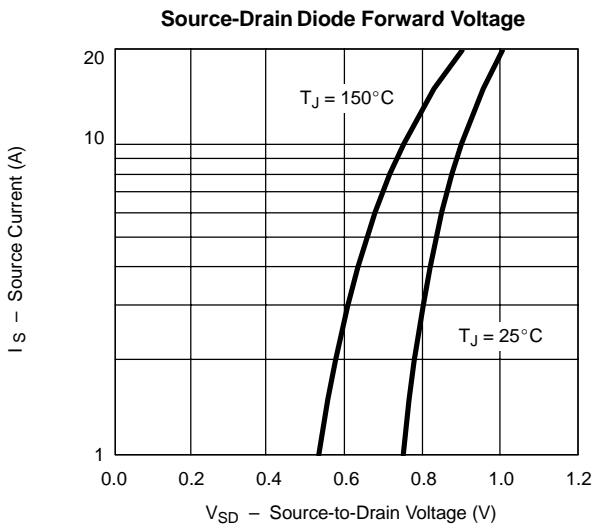
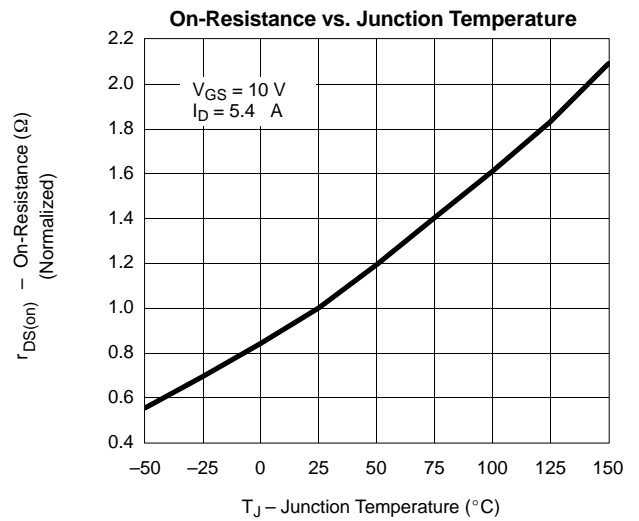
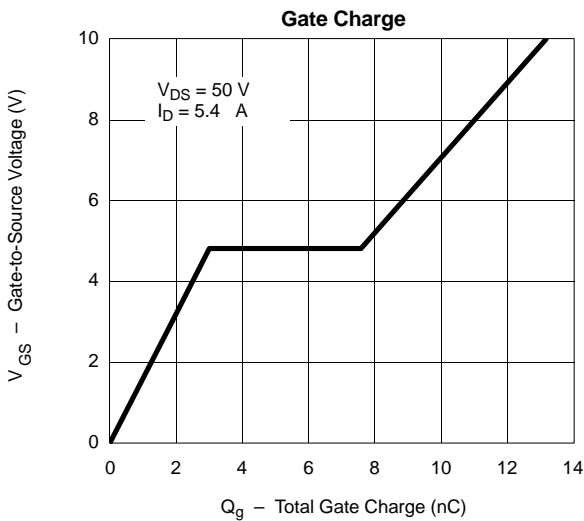
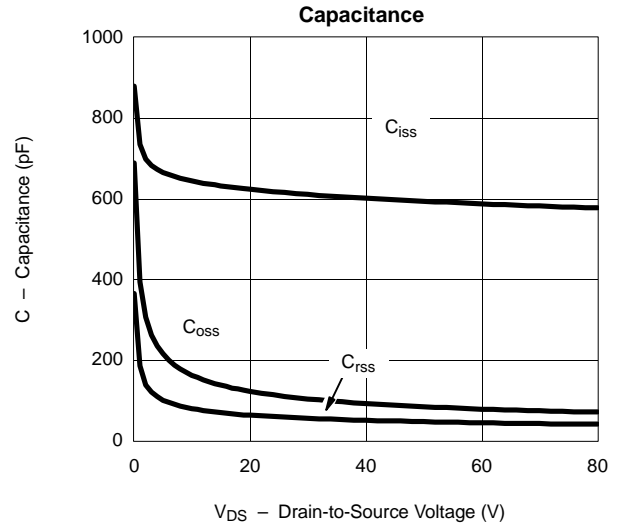
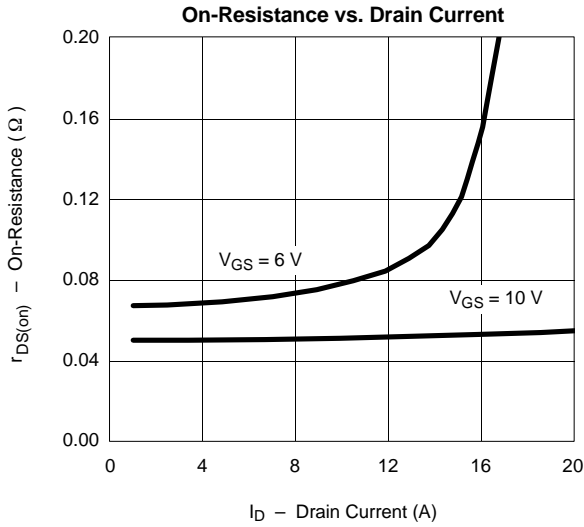
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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