# Dual-Output Power-Supply Controller

## FEATURES

- Fixed 5-V and 3.3-V Step-down Converters
- Less than 500-µA Quiescent Current per Converter
- 25-µA Shutdown Current
- 5.5-V to 30-V Operating Range

## DESCRIPTION

The Si786 Dual Controller for Portable Computer Power Conversion is pin and functionally compatible with the MAX786 dual-output power supply controller for notebook computers. The device is designed as a drop-in replacement for that circuit.

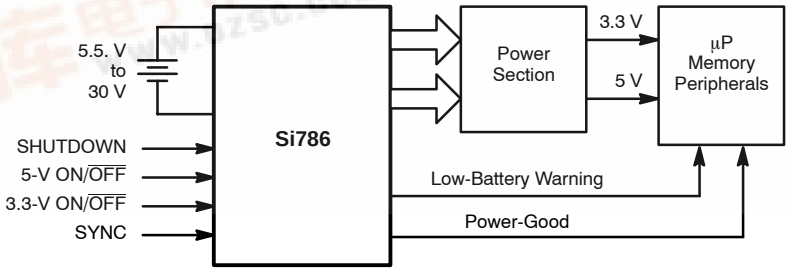
The circuit is a system level integration of two step-down controllers, micropower 5-V and 3.3-V linear regulators, and two comparators. The controllers perform high efficiency conversion of the battery pack energy (typically 12 V) or the output of an ac to dc wall converter (typically 18-V to 24-V dc) to 5-V and 3.3-V system supply voltages. The micropower linear regulator can be used to keep power management and back-up circuitry alive during the shutdown of the step-down converters. The comparators can be biased at any voltage between 2.7 V and the input voltage, simplifying battery monitoring or providing sufficient voltage to enhance the gate of a low on-resistance n-channel FET used in switching power to different zones in the system.

A complete power conversion and management system can be implemented with the Si786 Dual Controller for Portable Computer Power Conversion, an inexpensive linear regulator, the Si9140 SMP Controller for High Performance Processor Power Supplies, five Si4410 n-channel TrenchFET® Power MOSFETs, one Si4435 p-channel TrenchFET Power MOSFET, and two Si9712 PC Card (PCMCIA) Interface Switches.

The Si9130 Pin-Programmable Dual Controller for Portable PCs is another integrated system level devices for portable PC power systems.

The Si786 is available in both standard and lead (Pb)-free 28-pin SSOP packages and specified to operate over the (0°C to 70°C), (–10°C to 90°C) and (–40°C to 85°C) temperature ranges. See Ordering Information for corresponding part numbers.

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

V+ to GND . . . . . -0.3 V to 36 V
PGND to GND . . . . . ±2 V
$V_L$ to GND . . . . . -0.3V to 7 V
$BST_3$, $BST_5$ to GND . . . . . -0.3V to 36 V
$LX_3$ to $BST_3$ . . . . . -7 V to 0.3 V
$LX_5$ to $BST_5$ . . . . . -7 V to 0.3 V
Inputs/Outputs to GND
($D_1$, $D_2$, $\overline{SHDN}$, $ON_5$, REF, $SS_5$, $CS_5$. $FB_5$, SYNC, $CS_3$, $FB_3$, $SS_3$, $ON_3$)) . . . . . -0.3 V, ($V_L$ + 0.3 V)
$V_H$ to GND . . . . . -0.3 V to 20 V
$Q_1$, $Q_2$ to GND . . . . . -0.3 V, ($V_H$ + 0.3 V)
$DL_3$, $DL_5$ to PGND . . . . . -0.3 V, ($V_L$ + 0.3 V)
$DH_3$ to $LX_3$ . . . . . -0.3 V ($BST_3$ + 0.3 )
$DH_5$ to $LX_5$ . . . . . -0.3 V ($BST_5$ + 0.3 )

REF, $V_L$ Short to GND . . . . . Momentary
REF Current . . . . . 20 mA
$V_L$ Current . . . . . 50 mA
Continuous Power Dissipation ($T_A$ = 70°C)a
28-Pin SSOP[b] . . . . . 762 mW
Operating Temperature Range: ($T_{MIN}$ to $T_{MAX}$)
Si786CG/CRG/CSG (C-Grade) . . . . . 0 to 70°C
Si786LG/LRG/LSG (L-Grade) . . . . . −10° to 90°C
Si786DG/DRG/DSG (D-Grade) . . . . . −40° to 85°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 9.52 mW/°C above 70°C.

*Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time*

## SPECIFICATIONS

| Parameter | Specific Test Conditions<br>V+ = 15 V, $I_{VL}$ = $I_{REF}$ = 0 mA, $\overline{SHDN}$ = $ON_3$ = $ON_5$ = 5 V<br>Other Digital Input Levels 0 V or 5 V, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | Limits[e] Min[a] | Typ[b] | Max[a] | Unit |
|---|---|---|---|---|---|---|
| **3.3-V and 5-V Step-Down Controllers** | | | | | | |
| Input Supply Range | | | 5.5 | | 30 | V |
| $FB_5$ Output Voltage | 0 mV < ($CS_5$-$FB_5$) < 70 mV, 6 V < V + < 30 V<br>(includes load and line regulation) | | 4.80 | 5.08 | 5.20 | |
| $FB_3$ Output Voltage | 0 mV < ($CS_3$-$FB_3$) < 70 mV<br>6 V < V + < 30 V<br>(includes load and line regulation) | Si786CG/LG/DG | 3.17 | 3.35 | 3.46 | |
| | | Si786CRG/LRG/DRG | 3.32 | 3.50 | 3.60 | |
| | | Si786CSG/LSG/DSG | 3.46 | 3.65 | 3.75 | |
| Load Regulation | Either Controller ($CS_\_$ to $FB_\_$ = 0 to 70 mV) | | | 2.5 | | % |
| Line Regulation | Either Controller (V+ = 6 V to 30 V) | | | 0.03 | | %/V |
| Current-Limit Voltage | $CS_3$-$FB_3$ or $CS_5$-$FB_5$ | | 80 | 100 | 120 | mV |
| | | Si786DG/DRG/DSG | 77 | 100 | 120 | |
| $SS_3$/$SS_5$ Source Current | | | 2.5 | 4.0 | 6.5 | µA |
| | | Si786DG/DRG/DSG | 2.3 | 4.0 | 6.5 | |
| $SS_3$/$SS_5$ Fault Sink Current | | | 2 | | | mA |
| **Internal Regulator and Reference** | | | | | | |
| $V_L$ Output Voltage | $ON_5$ = $ON_3$ = 0 V, 5.5 V < V+ < 30 V<br>0 mA < $I_L$ < 25 mA | | 4.5 | | 5.5 | V |
| $V_L$ Fault Lockout Voltage | Falling Edge, Hysteresis = 1% | | 3.6 | | 4.2 | |
| $V_L$/$FB_5$ Switchover Voltage | Rising Edge of $FB_5$, Hysteresis = 1% | | 4.2 | | 4.7 | |
| REF Output Voltage | No External Load[c] | | 3.24 | | 3.36 | |
| REF Fault Lockout Voltage | Falling Edge | | 2.4 | | 3.2 | |
| REF Load Regulation | 0 mA < $I_L$ < 5 mA[d] | | | 30 | 75 | mV |
| V+ Shutdown Current | $\overline{SHDN}$ = $D_1$ = $D_2$ = $ON_3$ = $ON_5$ = 0 V<br>V+ = 30 V | | | 25 | 40 | µA |
| V+ Standby Current | $D_1$ = $D_2$ = $ON_3$ = $ON_5$ = 0 V, V+ = 30 V | | | 70 | 110 | |
| | | Si786DG/DRG/DSG | | 70 | 115 | |
| Quiescent Power Consumption (both PWM controllers on) | $D_1$ = $D_2$ = 0 V, $FB_5$ = $CS_5$ = 5.25 V<br>$FB_3$ = $CS_3$ = 3.5 V | | | 5.5 | 8.6 | mW |
| | | Si786DG/DRG/DSG | | 5.5 | 9.0 | |
| V+ Off Current | $FB_5$ = $CS_5$ = 5.25 V, $V_L$ Switched Over to $FB_5$ | | | 30 | 60 | µA |

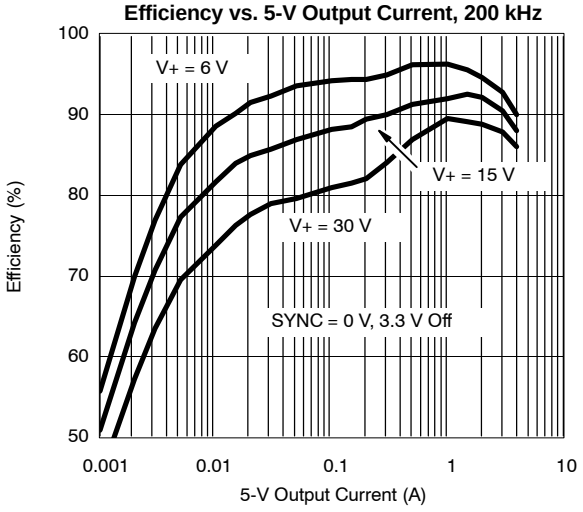
## SPECIFICATIONS

| Parameter | Specific Test Conditions<br>V+ = 15 V, $I_{VL}$ = $I_{REF}$ = 0 mA, $\overline{SHDN}$ = $ON_3$ = $ON_5$ = 5 V<br>Other Digital Input Levels 0 V or 5 V, $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | Limits[e] Min[a] | Typ[b] | Max[a] | Unit |
|---|---|---|---|---|---|---|
| **Comparators** | | | | | | |
| $D_1$, $D_2$ Trip Voltage | Falling Edge, Hysteresis = 1% | | 1.61 | | 1.69 | V |
| | | Si786DG/DRG/DSG | 1.60 | | 1.69 | |
| $D_1$, $D_2$ Input Current | $D_1$ = $D_2$ = 0 V, 5 V | | | | ±100 | nA |
| $Q_1$, $Q_2$ Source Current | $V_H$ = 15 V, $V_{OUT}$ = 2.5 V | | 12 | 20 | 30 | µA |
| $Q_1$, $Q_2$ Sink Current | | | 200 | 500 | 1000 | |
| $Q_1$, $Q_2$ Output High Voltage | $I_{SOURCE}$ = 5 µA, $V_H$ = 3 V | | $V_H$ - 0.5 | | | V |
| $Q_1$, $Q_2$ Output Low Voltage | $I_{SINK}$ = 20 µA, $V_H$ = 3 V | | | | 0.4 | |
| Quiescent $V_H$ Current | $V_H$ = 18 V, $D_1$ = $D_2$ = 5 V, No External Load | | | 4 | 10 | µA |
| **Oscillator and Inputs/Outputs** | | | | | | |
| Oscillator Frequency | SYNC = 3.3 V | | 270 | 300 | 330 | kHz |
| | | Si786DG/DRG/DSG | 260 | 300 | 330 | |
| | SYNC = 0 V, 5 V | | 170 | 200 | 230 | |
| | | Si786DG/DRG/DSG | 165 | 200 | 230 | |
| SYNC High Pulse Width | | | 200 | | | ns |
| SYNC Low Pulse Width | | | 200 | | | |
| SYNC Rise/Fall Time | Not Tested | | | | 200 | |
| Oscillator SYNC Range | | | 240 | | 350 | kHz |
| Maximum Duty Cycle | SYNC = 3.3 V | | 89 | 92 | | % |
| | SYNC = 0 V, 5 V | | 92 | 95 | | |
| Input Low Voltage | $\overline{SHDN}$, $ON_3$, $ON_5$ SYNC | | | | 0.8 | V |
| Input High Voltage | $\overline{SHDN}$, $ON_3$, $ON_5$ | | 2.4 | | | |
| | SYNC | | $V_L$ - 0.5 | | | |
| Input Current | $\overline{SHDN}$, $ON_3$, $ON_5$ $V_{IN}$ = 0 V, 5 V | | | | ±1 | µA |
| $DL_3$/$DL_5$ Sink/Source Current | $V_{OUT}$ = 2 V | | | 1 | | A |
| $DH_3$/$DH_5$ Sink/Source Current | $BST_3$ - $LX_3$ = $BST_5$ - $LX_5$ = 4.5 V, $V_{OUT}$ = 2 V | | | 1 | | |
| $DL_3$/$DL_5$ On-Resistance | High or Low | | | | 7 | Ω |
| $DH_3$/$DH_5$ On-Resistance | High or Low<br>$BST_3$ - $LX_3$ = $BST_5$ - $LX_5$ = 4.5 V | | | | 7 | |

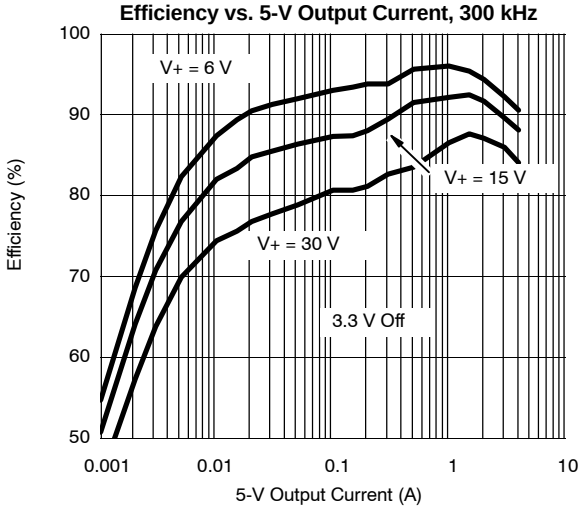
Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The main switching outputs track the reference voltage. Loading the reference reduces the main outputs slightly according to the closed-loop gain ($AV_{CL}$) and the reference voltage load-regulation error. $AV_{CL}$ for the 3.3-V supply is unity gain. $AV_{CL}$ for the 5-V supply is 1.54.
d. Since the reference uses $V_L$ as its supply, its V+ line regulation error is insignificant.
e. Limits are for all temperature grades unless otherwise noted.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

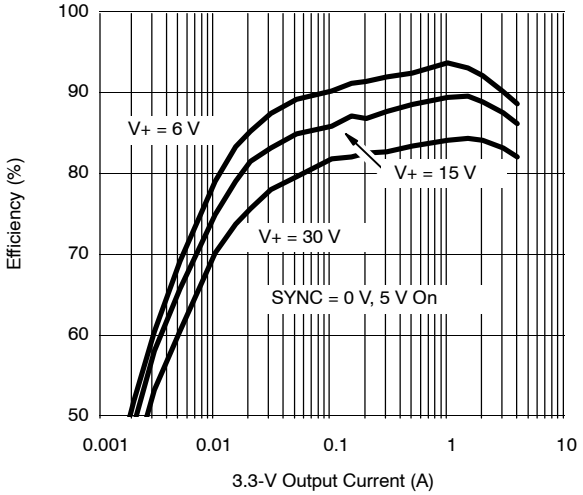
**Efficiency vs. 5-V Output Current, 200 kHz**



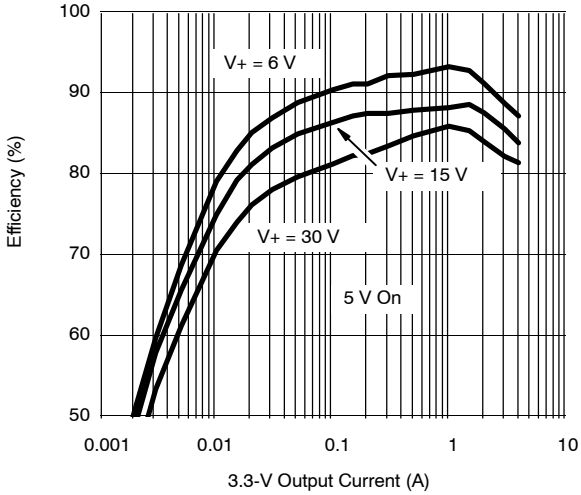

**Efficiency vs. 5-V Output Current, 300 kHz**



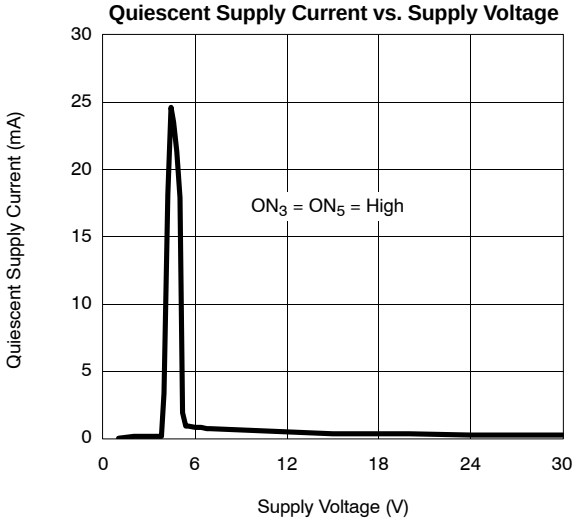

**Efficiency vs. 3.3-V Output Current, 200 kHz**



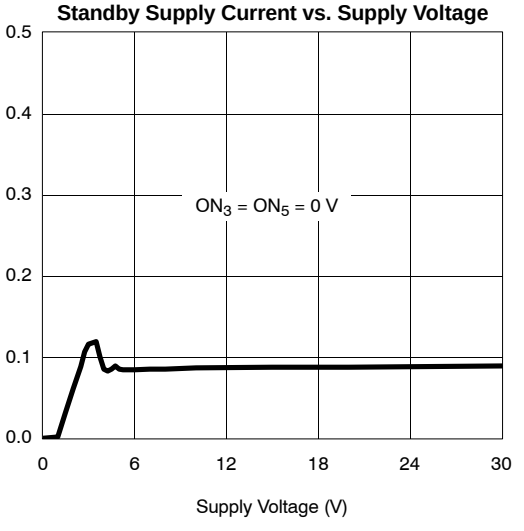

**Efficiency vs. 3.3-V Output Current, 300 kHz**




**Quiescent Supply Current vs. Supply Voltage**

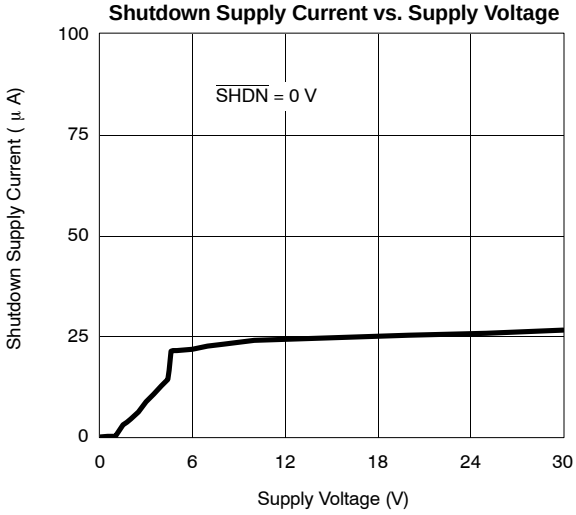



**Standby Supply Current vs. Supply Voltage**

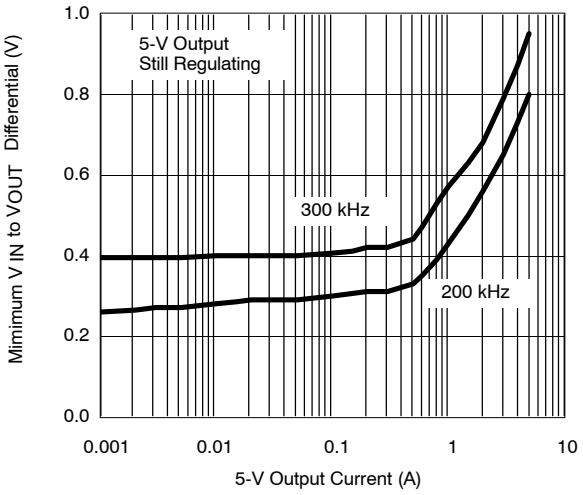


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

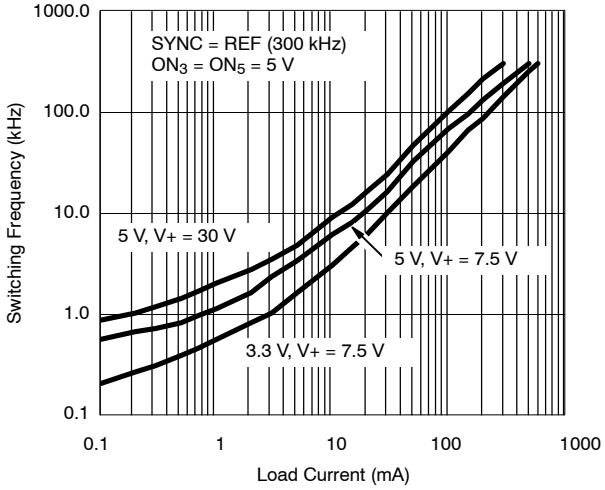
**Shutdown Supply Current vs. Supply Voltage**



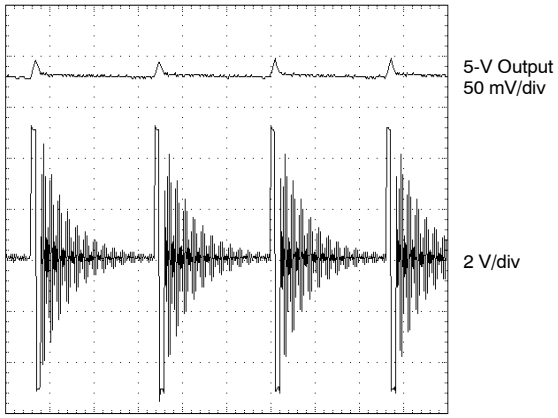

**Minimum $V_{IN}$ to $V_{OUT}$ Differential vs. 5-V Output Current**




**Switching Frequency vs. Load Current**

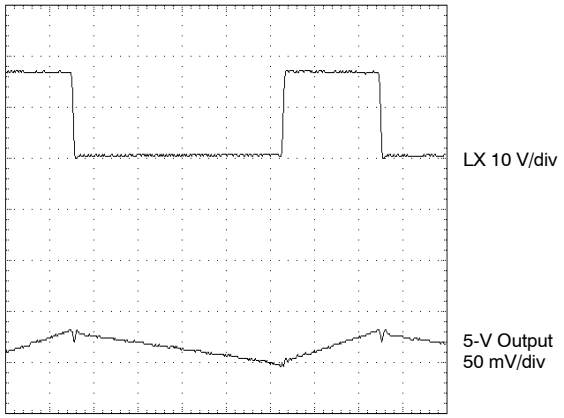



**Pulse-Skipping Waveforms**




200 μS/div
$I_{Load}$ = 100 mA
$V_{IN}$ = 10 V

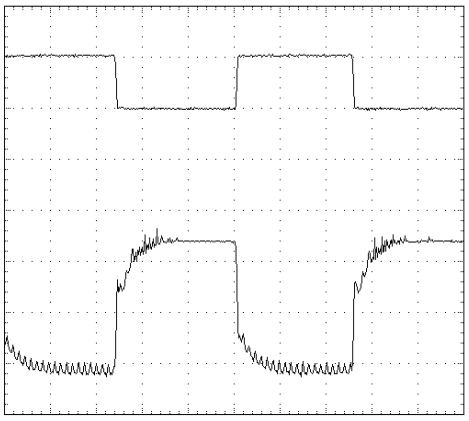
**Pulse-Width Modulation Mode Waveforms**




500 ns/div
5-V Output Current = 1 A
$V_{IN}$ = 16 V

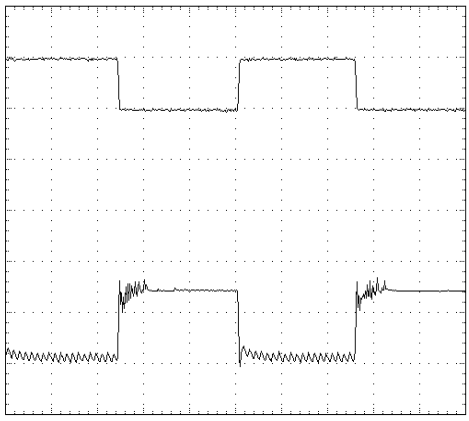
## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

**5-V Load-Transient Response**



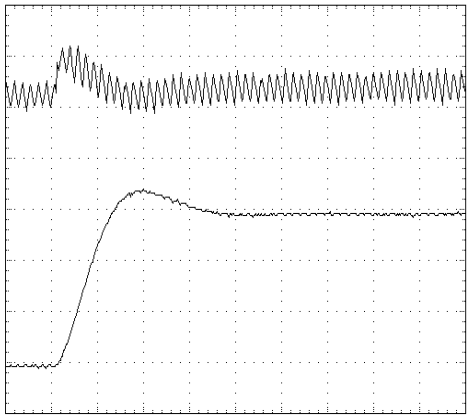

200 μS/div
$V_{IN}$ = 15 V

**3.3-V Load-Transient Response**



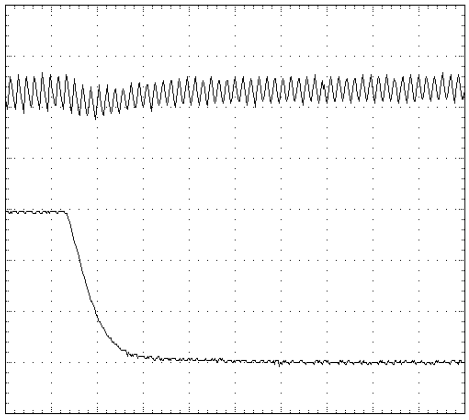

200 μS/div
$V_{IN}$ = 15 V

**5-V Line-Transient Response, Rising**



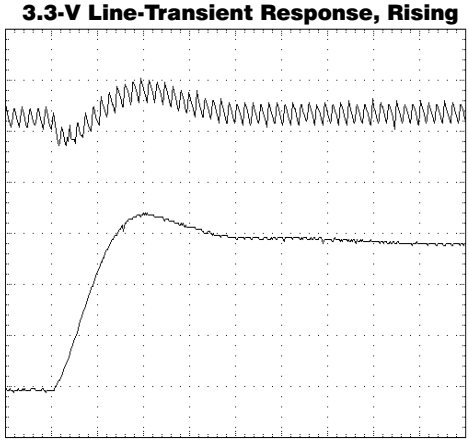

20 μS/div
$I_{LOAD}$ = 2 A

**5-V Line-Transient Response, Falling**



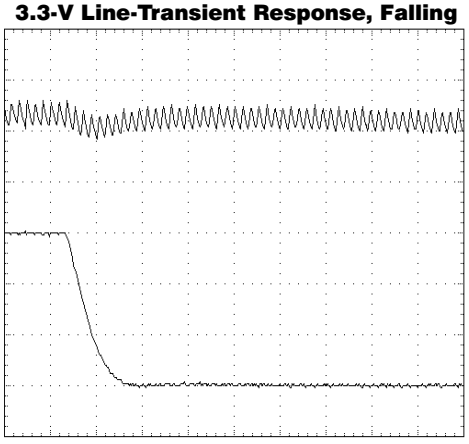

20 μS/div
$I_{LOAD}$ = 2 A

**3.3-V Line-Transient Response, Rising**



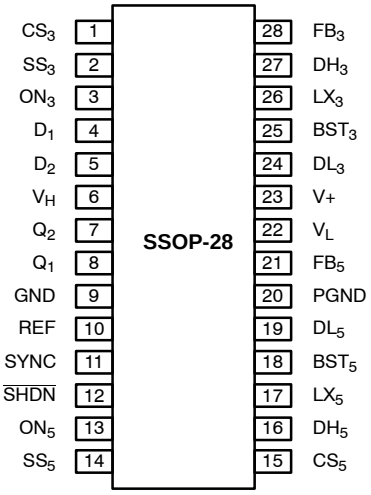

20 μS/div
$I_{LOAD}$ = 2 A

**3.3-V Line-Transient Response, Falling**




20 μS/div
$I_{LOAD}$ = 2 A

## PIN DESCRIPTION AND ORDERING INFORMATION




Top View

### PIN DESCRIPTION

| Pin | Symbol | Description |
|---|---|---|
| 1 | $CS_3$ | Current-sense input for 3.3-V Buck controller—this pins over current threshold is 100 mV with respect to $FB_3$. |
| 2 | $SS_3$ | Soft-start input for 3.3 V. Connect capacitor from $SS_3$ to GND. |
| 3 | $ON_3$ | ON/$\overline{OFF}$ logic input disables the 3.3-V Buck controller. Connect directly to $V_L$ for automatic turn-on. |
| 4 | $D_1$ | Comparator #1 noninverting input, threshold = 1.650 V. Comparator #1 output = Q1. Connect to GND if unused. |
| 5 | $D_2$ | Comparator #2 noninverting input (see $D_1$). |
| 6 | $V_H$ | External bias supply-voltage input for comparators #1 and #2. |
| 7 | $Q_2$ | Comparator #2 output. Sources 20 μA from $V_H$ when $D_2$ is high. Sinks 500 μA to GND when $D_2$ is low regardless of $V_H$ input voltage. |
| 8 | $Q_1$ | Comparator #1 output (see $Q_2$). |
| 9 | GND | Analog ground. |
| 10 | REF | 3.3-V reference output. Supplies external loads up to 5 mA. |
| 11 | SYNC | Oscillator control/synchronization input. Connect capacitor to GND, 1-μF/mA output or 0.22 μF minimum. For external clock synchronization, a rising edge starts a new cycle to start. To use internal 200-kHz oscillator, connect to VL or GND. For 300-kHz oscillator, connect to REF. |
| 12 | $\overline{SHDN}$ | Shutdown logic input, active low. Connect to $V_L$ for automatic turn-on. The 5-V $V_L$ supply will not be disabled in shutdown allowing connection to $\overline{SHDN}$. |
| 13 | $ON_5$ | ON/$\overline{OFF}$ logic input disables the 5-V Buck Controller. Connect to $V_L$ for automatic turn-on. |
| 14 | $SS_5$ | Soft-start control input for 5 V Buck controller. Connect capacitor from $SS_5$ to GND. |
| 15 | $CS_5$ | Current-sense input for 5 V Buck controller—this pins over current threshold is 100 mV referenced to $FB_3$. |
| 16 | $DH_5$ | Gate-drive output for the 5-V supply high-side n-channel MOSFET. |
| 17 | $LX_5$ | Inductor connection for the 5-V supply. |
| 18 | $BST_5$ | Boost capacitor connection for the 5-V supply. |
| 19 | $DL_5$ | Gate-drive output for the 5-V supply rectifying n-channel MOSFET. |
| 20 | PGND | Power Ground. |
| 21 | $FB_5$ | Feedback input for the 5-V Buck controller. |
| 22 | $V_L$ | 5-V logic supply voltage for internal circuitry—able to source 5-mA external loads. $V_L$ remains on with valid voltage at V+. |
| 23 | V+ | Supply voltage input. |
| 24 | $DL_3$ | Gate-drive output for the 3.3-V supply rectifying n-channel MOSFET. |
| 25 | $BST_3$ | Boost capacitor connection for the 3.3-V supply. |
| 26 | $LX_3$ | Inductor connection for the 3.3-V supply. |
| 27 | $DH_3$ | Gate-drive output for the 3.3-V supply high-side n-channel MOSFET. |
| 28 | $FB_3$ | Feedback input for the 3.3-V Buck controller. |

| ORDERING INFORMATION | | | |
|---|---|---|---|
| Part Number | Lead (Pb)-Free Part Number | Temp Range | $V_{OUT}$ |
| Si786CG | | C-Grade 0 to 70°C | 3.3 V |
| Si786CG-T1 | Si786CG-T1—E3 | | |
| Si786CRG | | | 3.45 V |
| Si786CRG-T1 | Si786CRG-T1—E3 | | |
| Si786CSG | | | 3.6 V |
| Si786CSG-T1 | Si786CSG-T1—E3 | | |
| Si786LG | | L-Grade −10° to 90°C | 3.3 V |
| Si786LG-T1 | Si786LG-T1—E3 | | |
| Si786LRG | | | 3.45 V |
| Si786LRG-T1 | Si786LRG-T1—E3 | | |
| Si786LSG | | | 3.6 V |
| Si786LSG-T1 | Si786LSG-T1—E3 | | |
| Si786DG | | D-Grade −40° to 85°C | 3.3 V |
| Si786DG-T1 | Si786DG-T1—E3 | | |
| Si786DRG | | | 3.45 V |
| Si786DRG-T1 | Si786DRG-T1—E3 | | |
| Si786DSG | | | 3.6 V |
| Si786DSG-T1 | Si786DSG-T1—E3 | | |

| Demo Board | Temp Range | Board Type |
|---|---|---|
| Si786DB | 0 to 70°C | Surface Mount |

## DESCRIPTION OF OPERATION

The Si786 is a dual step-down converter, which takes a 5.5-V to 30-V input and supplies power via two PWM controllers (see Figure 1). These 5-V and 3.3-V supplies run on an optional 300-kHz or 200-kHz internal oscillator, or an external sync signal. Amount of output current is limited by external components, but can deliver greater than 6 A on either supply. As well as these two main Buck controllers, additional loads can be driven from two micropower linear regulators, one 5 V ($V_L$) and the other 3.3 V (REF)—see Figure 2. These supplies are each rated to deliver 5 mA. If the linear regulator circuits fall out of regulation, both Buck controllers are shut down.

Two voltage comparators with adjustable output voltages are included in the Si786. They can be used for gate drive in load switching applications, where n-channel MOSFETs are used. Logic level voltages can be generated as well, for instance to serve as µP interfacing (e.g. a Power-good signal).

### 3.3-V Switching Supply

The 3.3-V supply is regulated by a current-mode PWM controller in conjunction with several externals: two n-channel MOSFETs, a rectifier, an inductor and output capacitors (see Figure 1). The gate drive supplied by $DH_3$ needs to be greater than $V_L$ , so it is provided by the bootstrap circuit consisting of a 100-nF capacitor and diode connected to $BST_3$ .

A low-side switching MOSFET connected to $DL_3$ increases efficiency by reducing the voltage across the rectifier diode. A low value sense resistor in series with the inductor sets the maximum current limit, to disallow current overloads at power-on or in short-circuit situations.

The soft-start feature on the Si786 is capacitor programmable; pin $SS_3$ functions as a constant current source to the external capacitor connected to GND. Excess currents at power-on are avoided, and power-supplies can be sequenced with different turn-on delay times by selecting the correct capacitor value.

### 5-V Switching Supply

The 5-V supply is regulated by a current-mode PWM controller which is nearly the same as the 3.3-V output. The dropout voltage across the 5-V supply, as shown in the schematic in Figure 1, is 400 mV (typ) at 2 A. If the voltage at V+ falls, nearing 5 V, the 5-V supply will lower as well, until the $V_L$ linear regulator output falls below the 4-V undervoltage lockout threshold. Below this threshold, the 5-V controller is shut off.

The frequency of both PWM controllers is set at 300 kHz when the SYNC pin is tied to REF. Connecting SYNC to either GND or $V_L$ sets the frequency at 200 kHz.

### 3.3-V and 5-V Switching Controllers

Each PWM controller on the Si786 is identical with the exception of the preset output voltages. The controllers only share three functional blocks (see Figure 2): the oscillator, the voltage reference (REF) and the 5-V logic supply ($V_L$). The 3.3-V and 5-V controllers are independently enabled with pins $ON_3$ and $ON_5$ , respectively. The PWMs are a direct-summing type, without the typical integrating error amplifier along with the phase shift which is a side effect of this type of topology. Feedback compensation is not needed, as long as the output capacitance and its ESR requirements are met, according to the *Design Considerations* section of this data sheet.

The main PWM comparator is an open loop device which is comprised of three comparators summing four signals: the feedback voltage error signal, current sense signal, slope-compensation ramp and voltage reference as shown in Figure 3. This method of control comes closer to the ideal of maintaining the output voltage on a cycle-by-cycle basis. When the load demands high current levels, the controller is in full PWM mode. Every cycle from the oscillator asserts the output latch and drives the gate of the high-side MOSFET for a period determined by the duty cycle (approximately $V_{OUT}/V_{IN} \times 100\%$) and the frequency. The high-side switch turns off, setting the synchronous rectifier latch and 60ns later, the rectifier MOSFET turns on. The low-side switch stays on until the start of the next clock cycle in continuous mode, or until the inductor current becomes positive again in discontinuous mode. In over-current situations, where the inductor current is greater than the 100-mV current-limit threshold, the high-side latch is reset and the high-side gate drive is shut off.

During low-current load requirements, the inductor current will not deliver the 25-mV minimum current threshold. The Minimum Current comparator signals the PWM to enter pulse-skipping mode when the threshold has not been reached. Pulse-skipping mode skips pulses to reduce switching losses, the losses which decrease efficiency the most at light load. Entering this mode causes the minimum current comparator to reset the high-side latch at the beginning of each oscillator cycle.

### Soft-Start

To slowly bring up the 3.3-V and 5-V supplies, connect capacitors from $SS_3$ and $SS_5$ to GND. Asserting $ON_3$ or $ON_5$ starts a 4-μA constant current source to charge these capacitors to 4 V. As the voltage on these pins ramps up, so does the current limit comparator threshold, to increase the duty cycle of the MOSFETs to their maximum level. If $ON_3$ or $ON_5$ are left low, the respective capacitor is discharged to GND. Leaving the $SS_3$ or $SS_5$ pins open will cause either controller to reach the terminal over-current level within 10 μs.

Soft start helps prevent current spikes at turn-on and allows separate supplies to be delayed using external programmability.

### Synchronous Rectifiers

Synchronous rectification replaces the Schottky rectifier with a MOSFET, which can be controlled to increase the efficiency of the circuit.

When the high-side MOSFET is switched off, the inductor will try to maintain its current flow, inverting the inductor's polarity. The path of current then becomes the circuit made of the Schottky diode, inductor and load, which will charge the output capacitor. The diode has a 0.5-V forward voltage drop, which contributes a significant amount of power loss, decreasing efficiency. A low-side switch is placed in parallel with the Schottky diode and is turned on just after the diode begins to conduct. Because the $r_{DS(ON)}$ of the MOSFET is low, the I*R voltage drop will not be as large as the diode, which increases efficiency. The low-side rectifier is shut off when the inductor current drops to zero.

Shoot-through current is the result when both the high-side and rectifying MOSFETs are turned on at the same time. Break-before-make timing internal to the Si786 manages this potential problem. During the time when neither MOSFET is on, the Schottky is conducting, so that the body diode in the low-side MOSFET is not forced to conduct.

Synchronous rectification is always active when the Si786 is powered-up, regardless of the operational mode.

### Gate-Driver Boost

The high-side n-channel drive is supplied by a flying-capacitor boost circuit (see Figure 4). The capacitor takes a charge from $V_L$ and then is connected from gate to source of the high-side MOSFET to provide gate enhancement. At power-up, the low-side MOSFET pulls LX_ down to GND and charges the BST_ capacitor connected to 5 V. During the second half of the oscillator cycle, the controller drives the gate of the high-side MOSFET by internally connecting node BST_ to DH_. This supplies a voltage 5 V higher than the battery voltage to the gate of the high-side MOSFET.

Oscillations on the gates of the high-side MOSFET in discontinuous mode are a natural occurrence caused by the LC network formed by the inductor and stray capacitance at the LX_ pins. The negative side of the BST_ capacitor is connected to the LX_ node, so ringing at the inductor is translated through to the gate drive.

## SCHEMATIC DRAWINGS

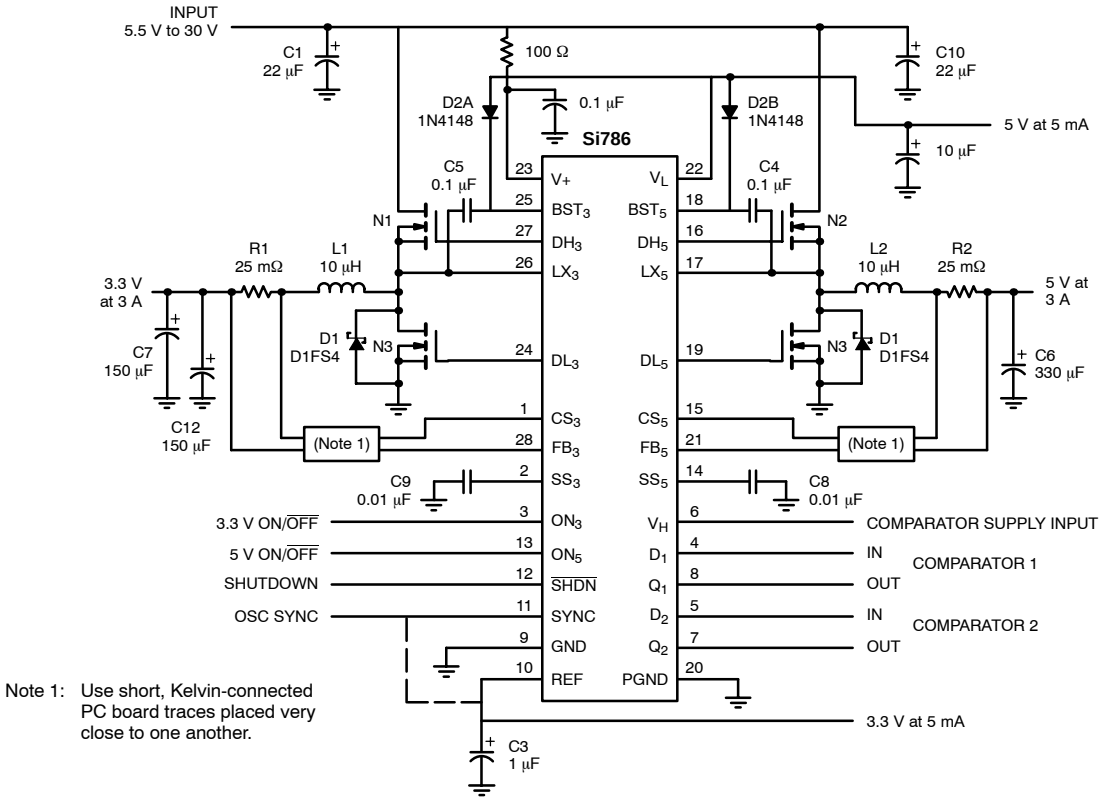



**FIGURE 1.** Si786 Application Circuit

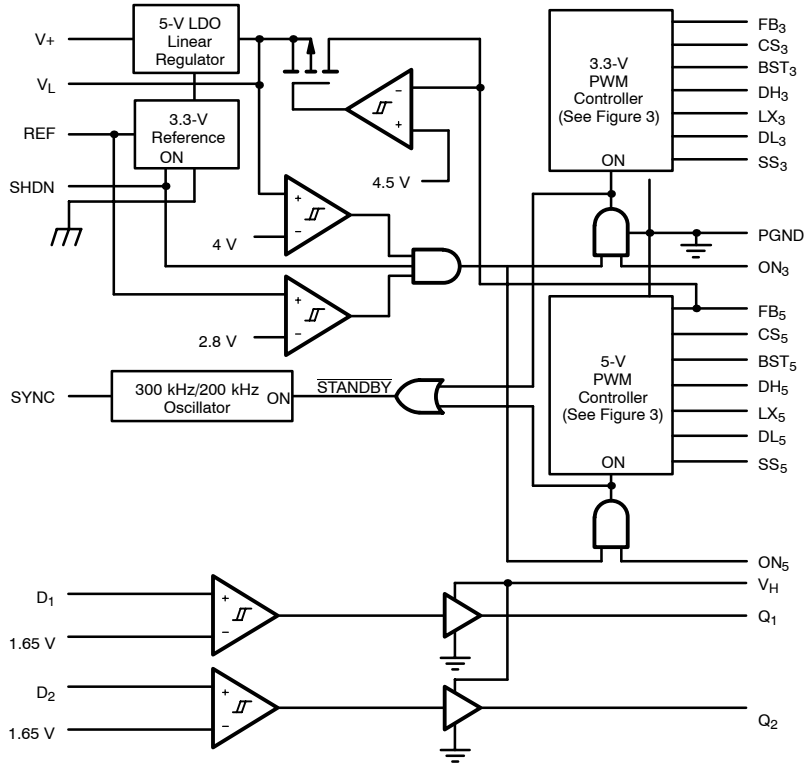



**FIGURE 2.** Si786 Block Diagram

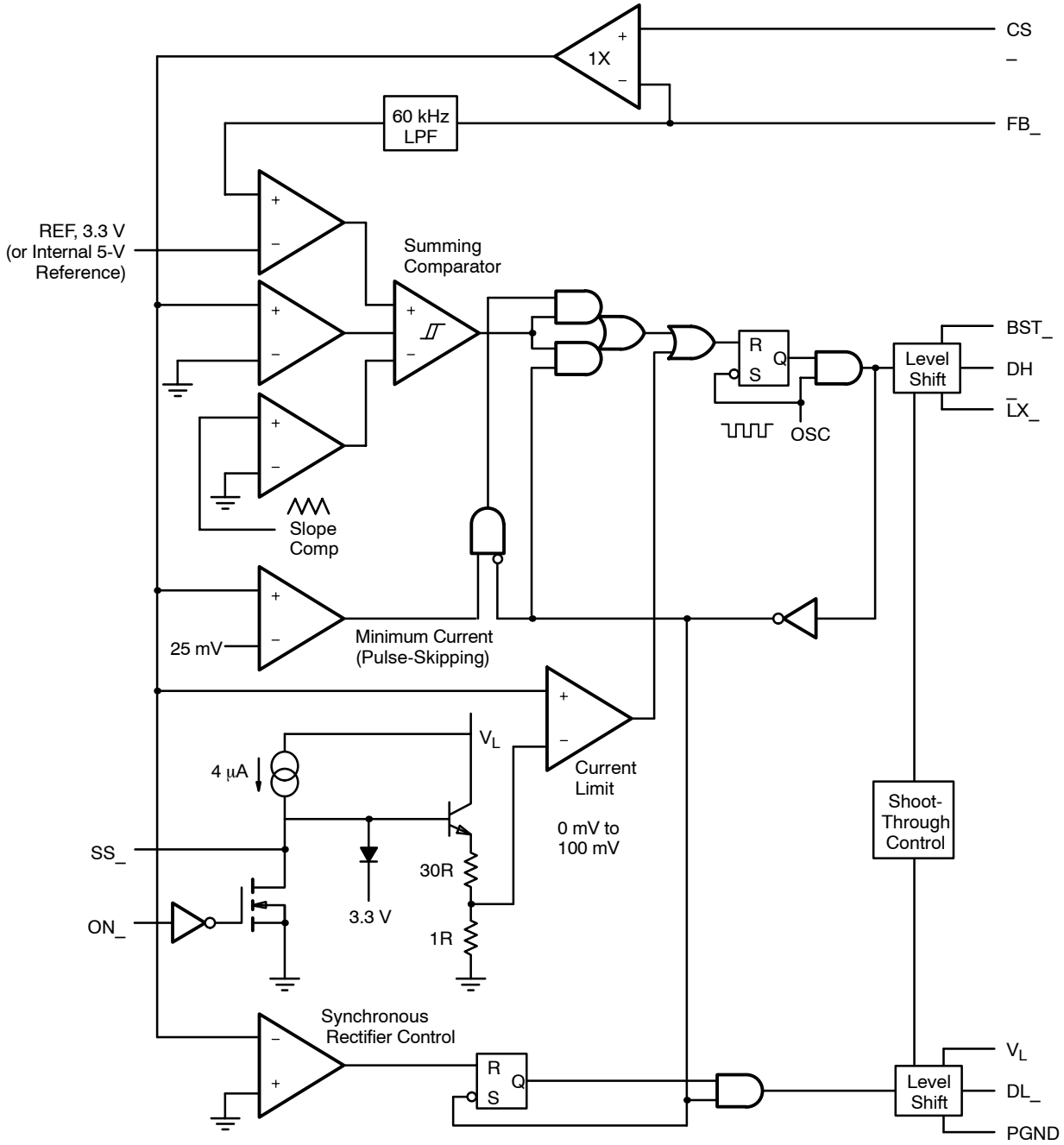



**FIGURE 3.** Si786 Controller Block Diagram

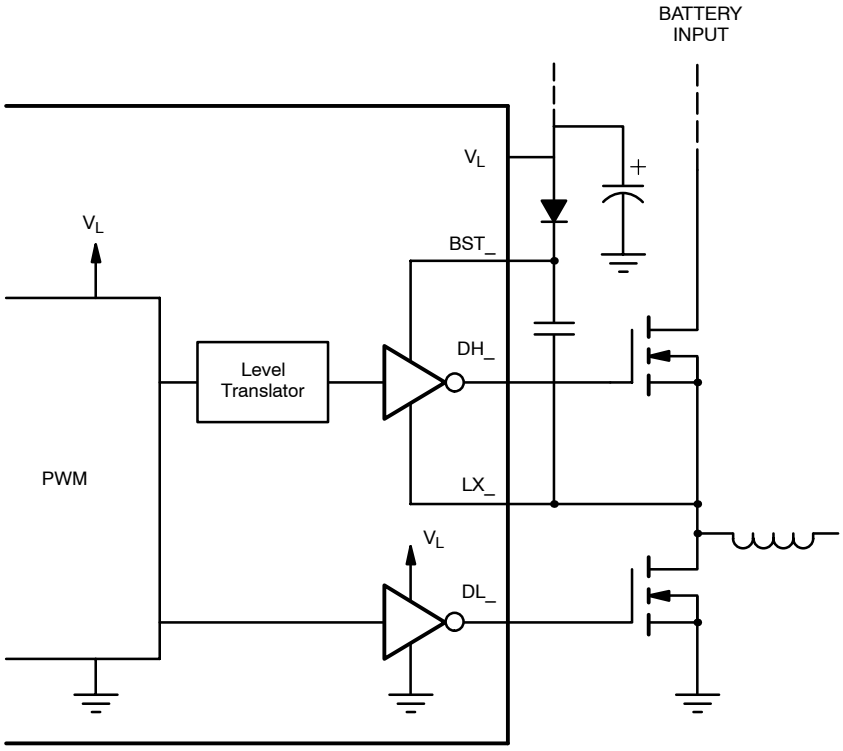



**FIGURE 4.** Boost Supply for Gate Drivers

## OPERATIONAL MODES

### PWM Mode

The 3.3-V and 5-V Buck controllers operate in continuous-current PWM mode when the load demands more than approximately 25% of the maximum current (see typical curves). The duty cycle can be approximated as Duty_Cycle = $V_{OUT}/V_{IN}$.

In this mode, the inductor current is continuous; in the first half of the cycle, the current slopes up when the high-side MOSFET conducts and then, in the second half, slopes back down when the inductor is providing energy to the output capacitor and load. As current enters the inductor in the first half-cycle, it is also continuing through to the load; hence, the load is receiving continuous current from the inductor. By using this method, output ripple is minimized and smaller form-factor inductors can be used. The output capacitor's ESR has the largest effect on output ripple. It is typically under 50 mV; the worst case condition is under light load with higher input battery voltage.

### Pulse-Skipping Mode

When the load requires less than 25% of its maximum, the Si786 enters a mode which drives the gate for one clock cycle and skips the majority of the remaining cycles. Pulse-skipping mode cuts down on the switching losses, the dominant power consumer at low current levels.

In the region between pulse-skipping mode and PWM mode, the controller may transition between the two modes, delivering spurts of pulses. This may cause the current waveform to look irregular, but will not overly affect the ripple voltage. Even in this transitional mode efficiency will stay high.

### Current Limit

The current through an external resistor, is constantly monitored to protect against over-current. A low value resistor is placed in series with the inductor. The voltage across it is measured by connecting it between CS_ and FB_. If this voltage is larger than 100 mV, the high-side MOSFET drive is shut down. Eliminating over-currents protects the MOSFET, the load and the power source. Typical values for the sense resistors with a 3-A load will be 25 mΩ.

### Oscillator and SYNC

There are two ways to set the Si786 oscillator frequency: by using an external SYNC signal, or using the internal oscillator. The SYNC pin can be driven with an external CMOS level signal with frequency from 240 kHz and 350 kHz to synchronize to the internal oscillator. Tying SYNC to either $V_L$ or GND sets the frequency to 200 kHz and to REF sets the frequency to 300 kHz.

Operation at 300 kHz is typically used to minimize output passive component sizes. Slower switching speeds of 200 kHz may be needed for lower input voltages.

### Internal $V_L$ and REF

A 5-V linear regulator supplies power to the internal logic circuitry. The regulator is available for external use from pin $V_L$ , able to source 5 mA. A 10-µF capacitor should be connected between $V_L$ and GND. To increase efficiency, when the 5 V switching supply has voltage greater than 4.5 V, $V_L$ is internally switched over to the output of the 5-V switching supply and the linear regulator is turned off.

The 5-V linear regulator provides power to the internal 3.3-V bandgap reference (REF). The 3.3-V reference can supply 5 mA to an external load, connected to pin REF. Between REF and GND connect a capacitor, 0.22 µF plus 1 µF per mA of load current. The switching outputs will vary with the reference; therefore, placing a load on the REF pin will cause the main outputs to decrease slightly, within the specified regulation tolerance.

$V_L$ and REF supplies stay on as long as V+ is greater than 4.5 V, even if the switching supplies are not enabled. This feature is necessary when using the micropower regulators to keep memory alive during shutdown.

Both linear regulators can be connected to their respective switching supply outputs. For example, REF would be tied to the output of the 3.3 V and $V_L$ to 5 V. This will keep the main supplies up in standby mode, provided that each load current in shutdown is not larger than 5 mA.

### Fault Protection

The 3.3 V and 5 V switching controllers as well as the comparators are shut down when one of the linear regulators drops below 85% of its nominal value; that is, shut down will occur when $V_L$ < 4.0 V or REF < 2.8 V.

## DESIGN CONSIDERATIONS

### Inductor Design

Three specifications are required for inductor design: inductance (L), peak inductor current ($I_{LPEAK}$), and coil resistance ($R_L$). The equation for computing inductance is:

$$L = \frac{(V_{OUT})(V_{IN(MAX)} - V_{OUT})}{(V_{IN(MAX)})(f)(I_{OUT})(LIR)}$$

Where: $V_{OUT}$ = Output voltage (3.3 V or 5 V);
$V_{IN(MAX)}$ = Maximum input voltage (V);
f = Switching frequency, normally 300 kHz;
$I_{OUT}$ = Maximum dc load current (A);
LIR = Ratio of inductor peak-to-peak ac current to average dc load current, typically 0.3.

When LIR is higher, smaller inductance values are acceptable, at the expense of increased ripple and higher losses.

The peak inductor current ($I_{LPEAK}$) is equal to the steady-state load current ($I_{OUT}$) plus one half of the peak-to-peak ac current ($I_{LPP}$). Typically, a designer will select the ac inductor current to be 30% of the steady-state current, which gives $I_{LPEAK}$ equal to 1.15 times $I_{OUT}$.

The equation for computing peak inductor current is:

$$I_{LPEAK} = I_{OUT} + \frac{(V_{OUT})(V_{IN(MAX)} - V_{OUT})}{(2)(f)(L)(V_{IN(MAX)})}$$

### Output Capacitors

The output capacitors determine loop stability and ripple voltage at the output. In order to maintain stability, minimum capacitance and maximum ESR requirements must be met according to the following equations:

$$C_F > \frac{V_{REF}}{(V_{OUT})(R_{CS})(2)(\pi)(GBWP)}$$

and,

$$ESR_{CF} < \frac{(V_{OUT})(R_{CS})}{V_{REF}}$$

Where: $C_F$ = Output filter capacitance (F)
$V_{REF}$ = Reference voltage, 3.3 V;
$V_{OUT}$ = Output voltage, 3.3 V or 5 V;
$R_{CS}$ = Sense resistor (Ω);
GBWP = Gain-bandwidth product, 60 kHz;
$ESR_{CF}$ = Output filter capacitor ESR (Ω).

Both minimum capacitance and maximum ESR requirements must be met. In order to get the low ESR, a capacitance value of two to three times greater than the required minimum may be necessary.

The equation for output ripple in continuous current mode is:

$$V_{OUT(RPL)} = I_{LPP(MAX)} \times \left( ESR_{CF} + \frac{1}{(2 \times \Pi \times f \times C_F)} \right)$$

The equations for capacitive and resistive components of the ripple in pulse-skipping mode are:

$$V_{OUT(RPL)}(C) = \frac{(4)(10^{-4})(L)}{(R_{CS}{}^2)(C_F)} \times \left( \frac{1}{V_{OUT}} + \frac{1}{V_{IN}-V_{OUT}} \right)$$

$$V_{OUT(RPL)}(R) = \frac{(0.02)(ESR_{CF})}{R_{CS}}$$

The total ripple, $V_{OUT(RPL)}$, can be approximated as follows:

if $V_{OUT(RPL)}(R) < 0.5\ V_{OUT(RPL)}(C)$,
then $V_{OUT(RPL)} = V_{OUT(RPL)}(C)$,
otherwise, $V_{OUT(RPL)} = 0.5\ V_{OUT(RPL)}(C) + V_{OUT(RPL)}(R)$.

***Lower Voltage Input***

The application circuit shown here can be easily modified to work with 5.5-V to 12-V input voltages. Oscillation frequency should be set at 200 kHz and increase the output capacitance to 660 μF on the 5-V output to maintain stable performance up to 2 A of load current. Operation on the 3.3-V supply will not be affected by this reduced input voltage.