



Si7888DP
Vishay Siliconix

N-Channel 30-V (D-S) MOSFET

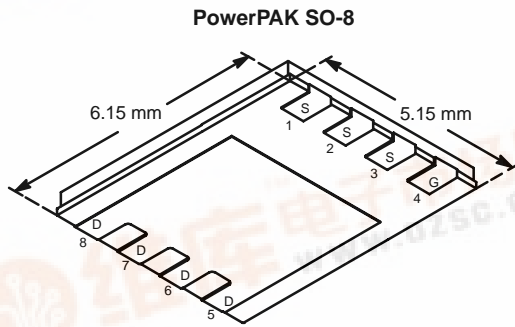
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.012 @ $V_{GS} = 10$ V	15.7
	0.020 @ $V_{GS} = 4.5$ V	12.1

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- Optimized for “High-Side” Synchronous Rectifier Operation
- 100% R_g Tested

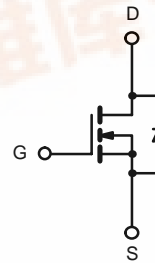
APPLICATIONS

- DC/DC Converters



Bottom View

Ordering Information: Si7888DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	15.7	9.4	A
		$T_A = 70^\circ\text{C}$	12.5	7.5	
Pulsed Drain Current	I_{DM}	± 50			
Continuous Source Current (Diode Conduction) ^a	I_S	4.1	1.5		
Avalanche Current	I_{AS}	20		A	
Single Pulse Avalanche Energy		E_{AS}	20		mJ
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5.0	1.8	W
		$T_A = 70^\circ\text{C}$	3.2	1.1	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient (MOSFET) ^a	R_{thJA}	$t \leq 10$ sec	21	25	$^\circ\text{C/W}$
		Steady State	55	70	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.4	3.0		

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.

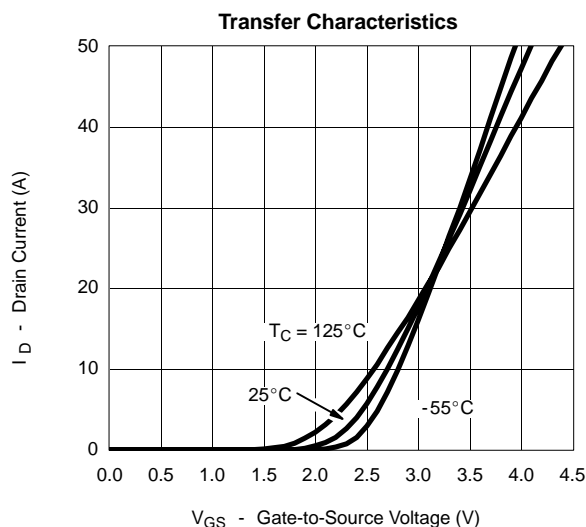
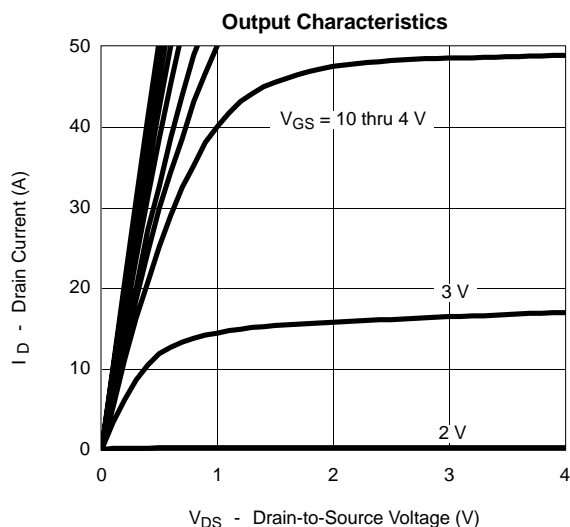


MOSFET SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.80		2	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 70 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 12.4 A		0.010	0.012	Ω
		V _{GS} = 4.5 V, I _D = 9.6 A		0.016	0.020	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 12.4 A		27		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.6 A, V _{GS} = 0 V		0.75	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 5.0 V, I _D = 12.4 A		8.7	10.5	nC
Gate-Source Charge	Q _{gs}			2.4		
Gate-Drain Charge	Q _{gd}			3.5		
Gate Resistance	R _g		0.2	1	1.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		10	20	ns
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			24	50	
Fall Time	t _f			10	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.6 A, di/dt = 100 A/μs		50	75	

Notes

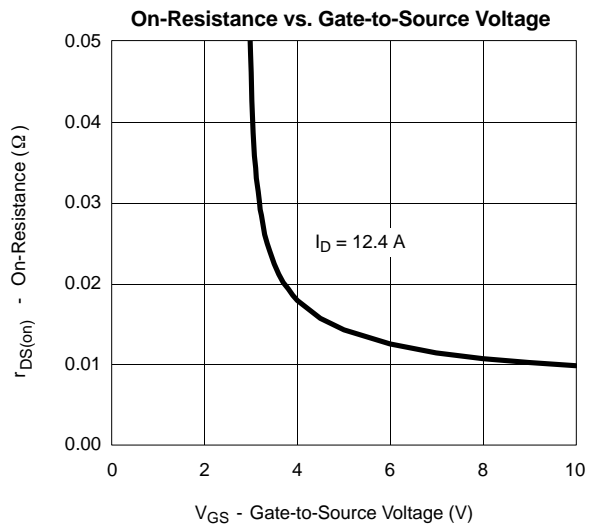
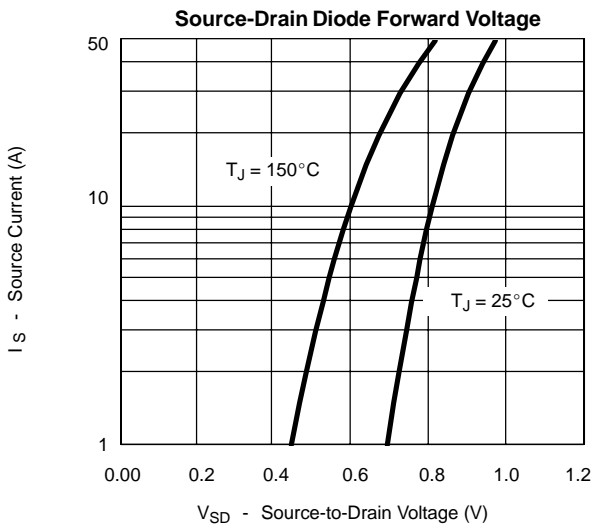
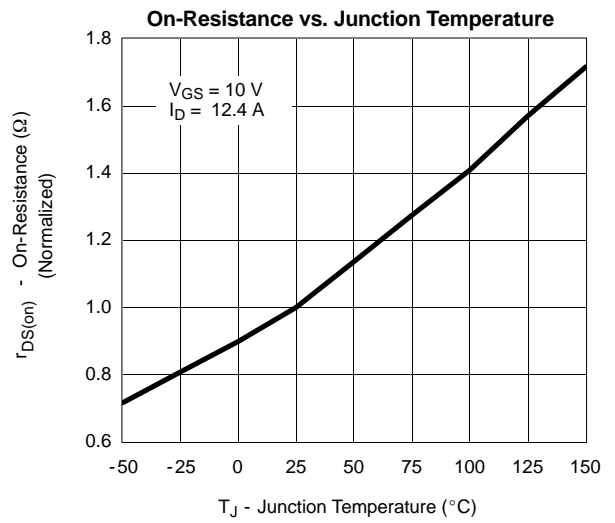
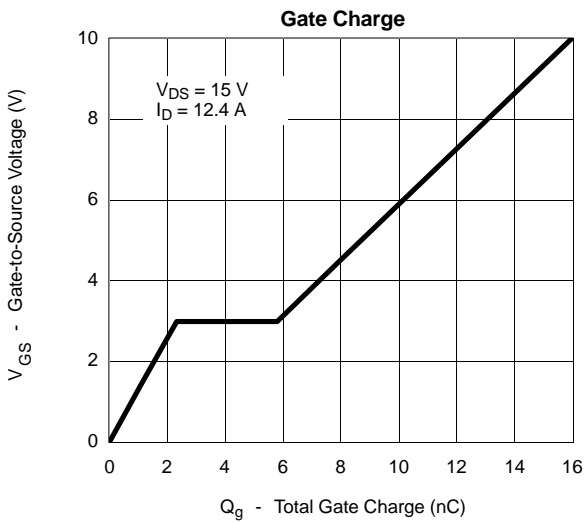
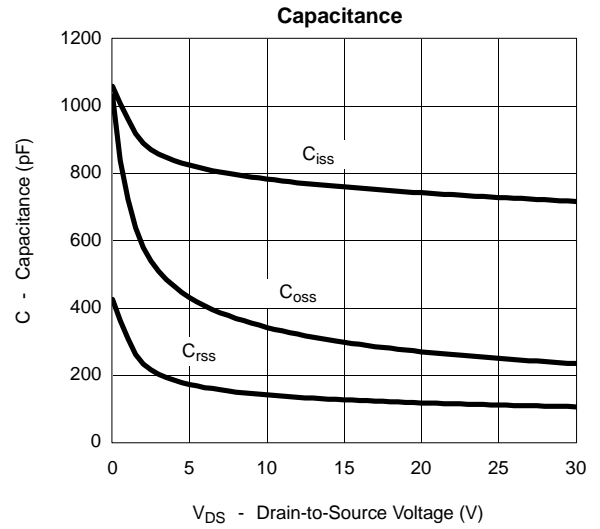
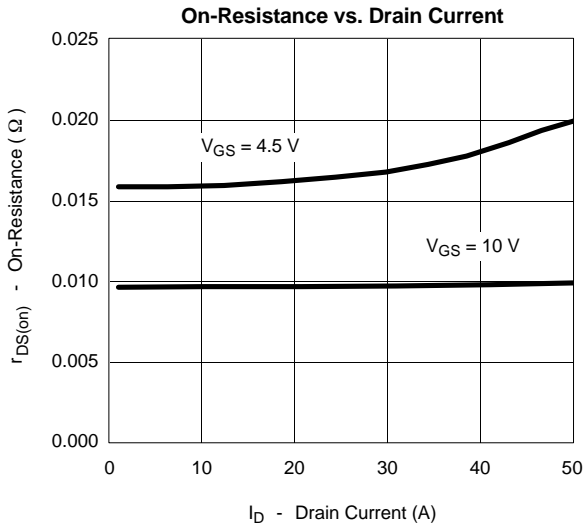
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

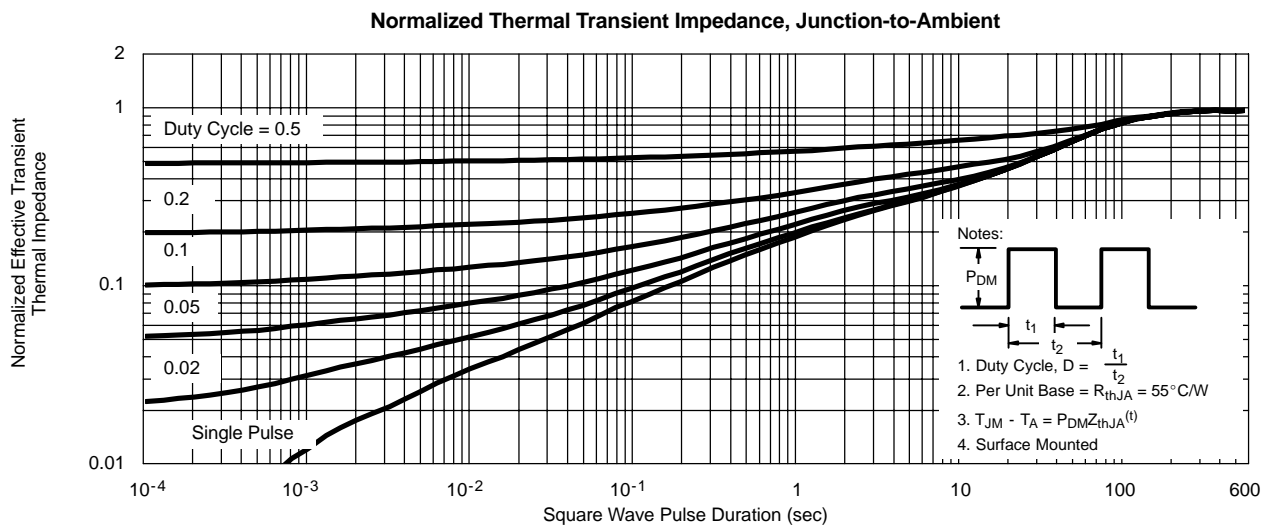
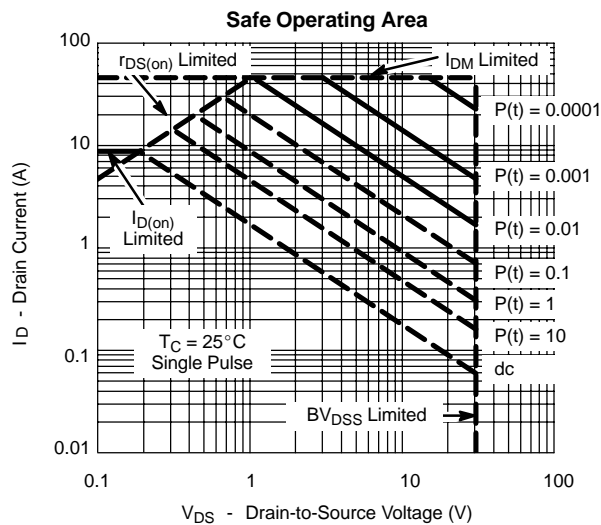
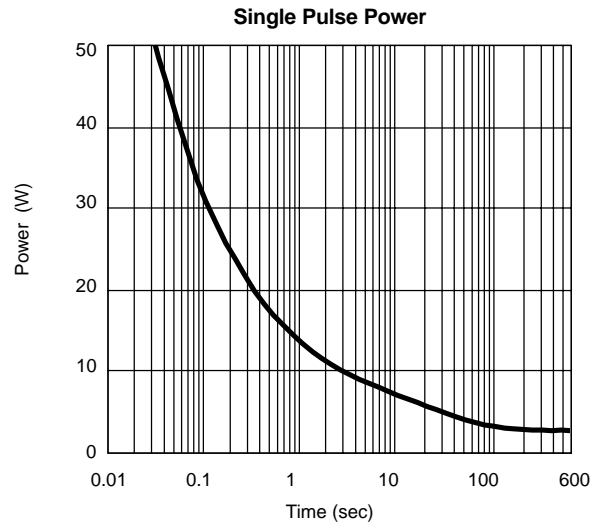
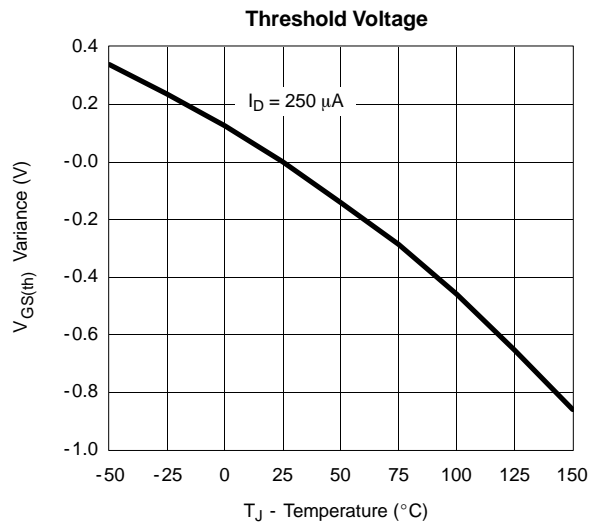




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