

# SPICE Device Model Si7943DP Vishay Siliconix

## **Dual P-Channel 30-V (D-S) MOSFET**

#### **CHARACTERISTICS**

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

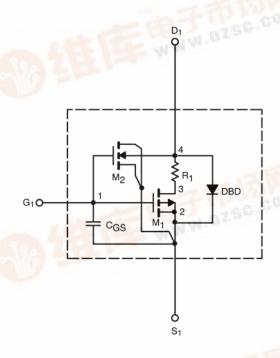
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

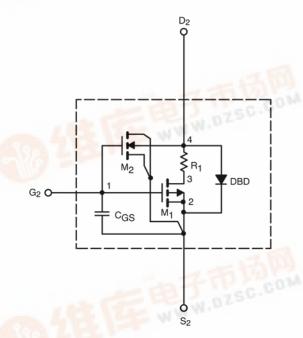
#### **DESCRIPTION**

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static	•				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu A$	1.1		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	235		Α
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = -10 \text{ V}, I_D = -9.4 \text{ A}$	0.020	0.020	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -8.6 \text{ A}$	0.024	0.024	
		$V_{GS} = -2.5 \text{ V}, I_D = -3 \text{ A}$	0.036	0.037	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = -15 \text{ V}, I_D = -9.4 \text{ A}$	23	15	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = -2.9 A, V <sub>GS</sub> = 0 V	-0.81	-0.80	V
Dynamic <sup>b</sup>					
Total Gate Charge	Q <sub>g</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -9.4 \text{ A}$	25	23.5	nC
Gate-Source Charge	$Q_{gs}$		8.5	8.5	
Gate-Drain Charge	$Q_{gd}$		5	5	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = -15 \text{ V}, R_{L} = 15 \Omega$ $I_{D} \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_{G} = 6 \Omega$ $I_{F} = -2.9 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	17	18	ns
Rise Time	t <sub>r</sub>		22	40	
Turn-Off Delay Time	$t_{\text{d(off)}}$		53	100	
Fall Time	t <sub>f</sub>		73	60	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		47	50	

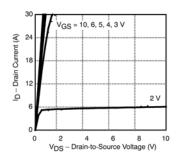
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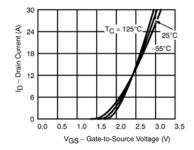
a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%. b. Guaranteed by design, not subject to production testing.

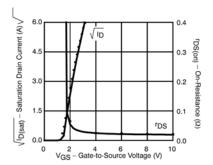


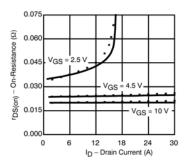
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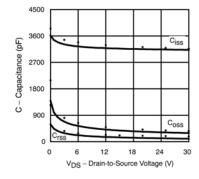
### COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

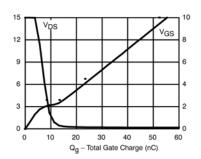












Note: Dots and squares represent measured data.

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