



New Product

**Si8902EDB**  
Vishay Siliconix

## Bi-Directional N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>S1S2</sub> (V)	r <sub>S1S2(on)</sub> (Ω)	I <sub>S1S2</sub> (A)
20	0.045 @ V <sub>GS</sub> = 4.5 V	5.0
	0.048 @ V <sub>GS</sub> = 3.7 V	4.8
	0.057 @ V <sub>GS</sub> = 2.5 V	4.4
	0.072 @ V <sub>GS</sub> = 1.8 V	3.9

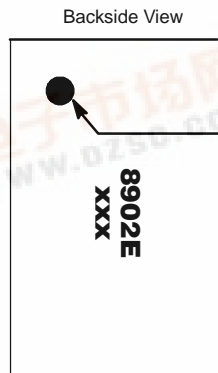
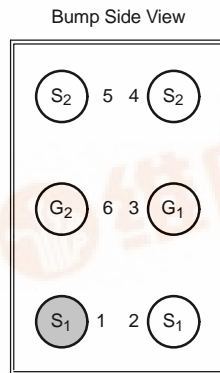
### FEATURES

- TrenchFET® Power MOSFET
- Ultra-Low r<sub>SS(on)</sub>
- ESD Protected: 4000 V
- New MICRO FOOT™ Chipscale Packaging Reduces Footprint Area, Profile (0.65 mm) and On-Resistance Per Footprint Area

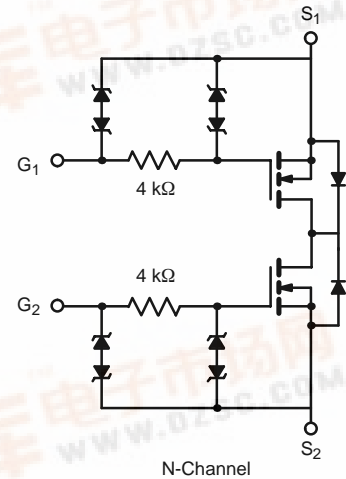
### APPLICATIONS

- Battery Protection Circuit
  - 1-2 Cell Li+/LiP Battery Pack for Portable Devices

### MICRO FOOT™



Device Marking:  
8902E = P/N Code  
xxx = Date/Lot Traceability Code



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Source1—Source2 Voltage	V <sub>S1S2</sub>	20		V	
Gate-Source Voltage	V <sub>GS</sub>	± 12			
Continuous Source1—Source2 Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>S1S2</sub>	T <sub>A</sub> = 25°C	5.0	3.9	A
		T <sub>A</sub> = 85°C	3.4	2.8	
Pulsed Source1—Source2 Current	I <sub>SM</sub>	8		W	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	1.7		1
		T <sub>A</sub> = 85°C	0.8	0.5	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C	
Package Reflow Conditions <sup>c</sup>	VPR	215			
	IR/Convection	220			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 5 sec	60	75	°C/W
		Steady State	95	120	
Maximum Junction-to-Foot <sup>b</sup>	R <sub>thJF</sub>	18	22		

Notes:  
 a. Surface Mounted on 1" x 1" FR4 Board.  
 b. The Foot is defined as the top surface of the package.  
 c. Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.



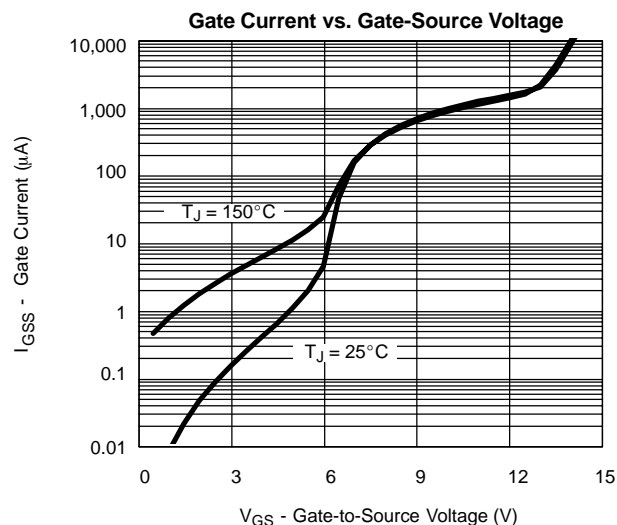
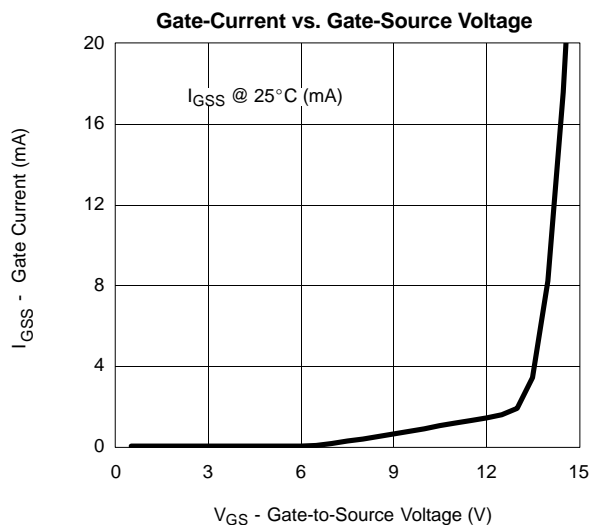
**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>SS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 980 μA	0.45		1.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>SS</sub> = 0 V, V <sub>GS</sub> = ±4.5 V			±4	μA
		V <sub>SS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±10	mA
Zero Gate Voltage Source Current	I <sub>S1S2</sub>	V <sub>SS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>SS</sub> = 16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			5	
On-State Source Current <sup>a</sup>	I <sub>S(on)</sub>	V <sub>SS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	5			A
Source1—Source2 On-State Resistance <sup>a</sup>	r <sub>S1S2(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>SS</sub> = 1 A		0.038	0.045	Ω
		V <sub>GS</sub> = 3.7 V, I <sub>SS</sub> = 1 A		0.041	0.048	
		V <sub>GS</sub> = 2.5 V, I <sub>SS</sub> = 1 A		0.048	0.057	
		V <sub>GS</sub> = 1.8 V, I <sub>SS</sub> = 1 A		0.060	0.072	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>SS</sub> = 10 V, I <sub>SS</sub> = 1 A		20		S
<b>Dynamic<sup>b</sup></b>						
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>SS</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>SS</sub> = 1 A, V <sub>GEN</sub> = 4.5 V, R <sub>G</sub> = 6 Ω		1	1.5	μs
Rise Time	t <sub>r</sub>			3	4.5	
Turn-Off Delay Time	t <sub>d(off)</sub>			17	26	
Fall Time	t <sub>f</sub>			10	15	

Notes

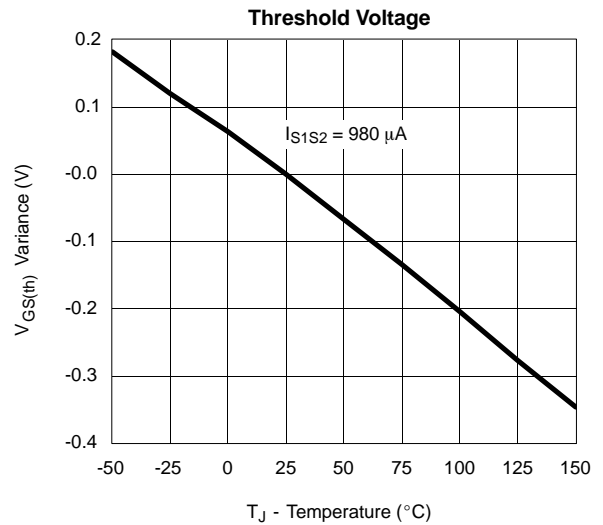
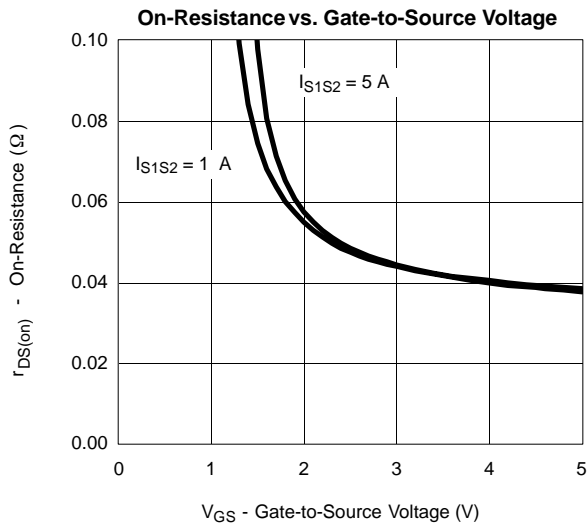
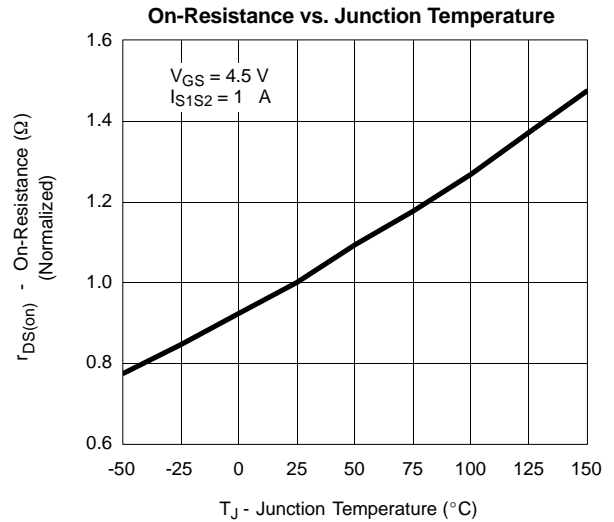
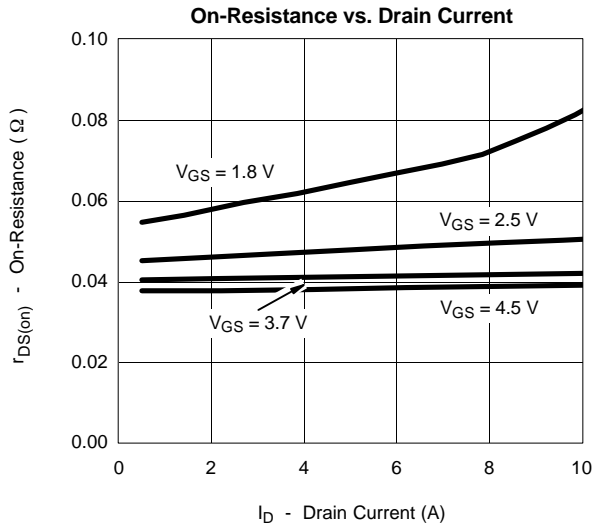
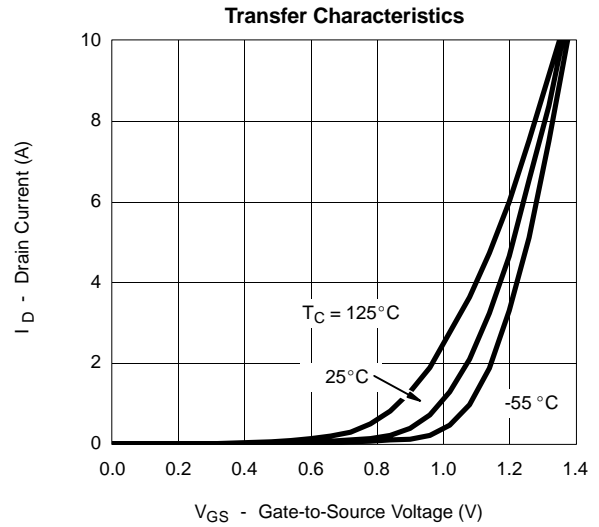
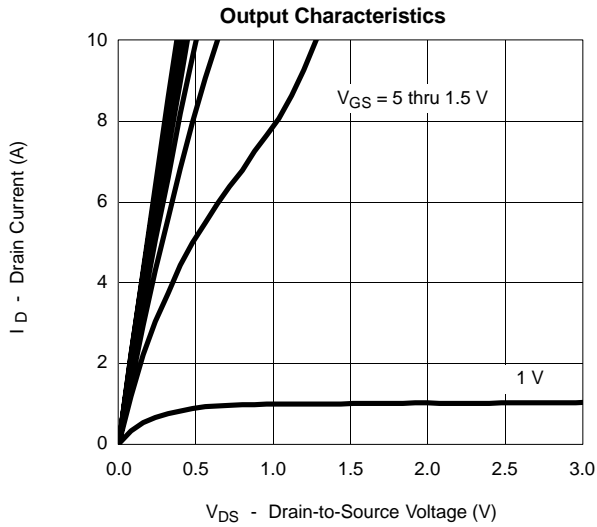
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



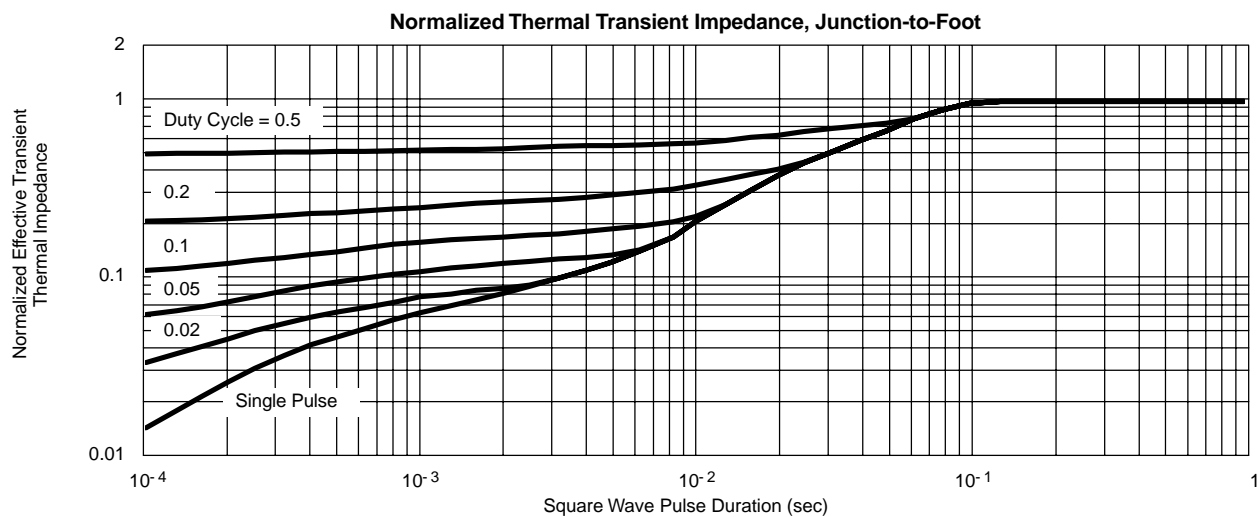
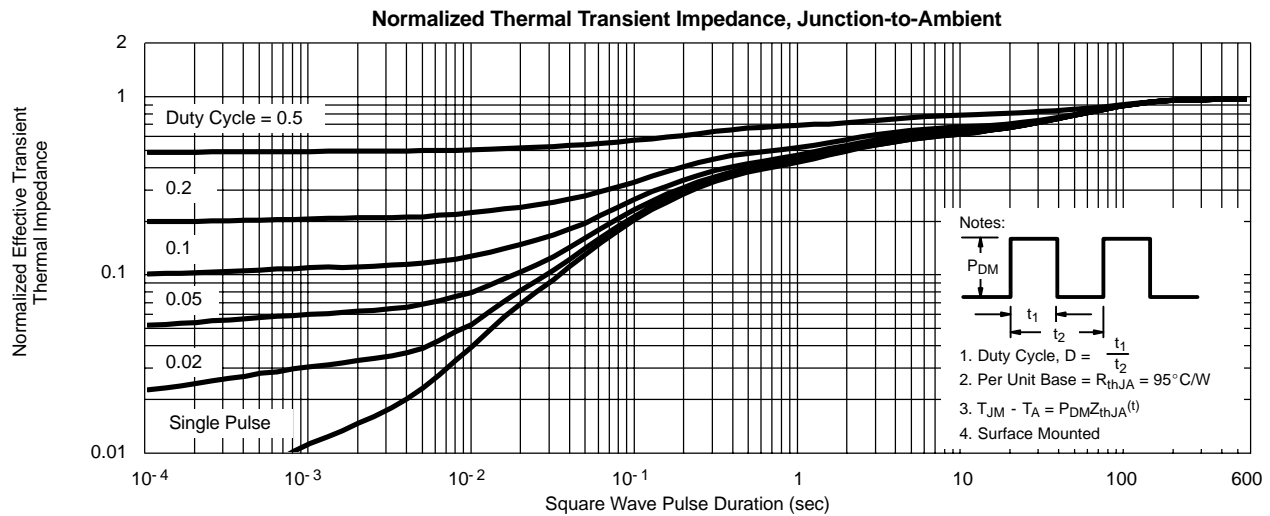
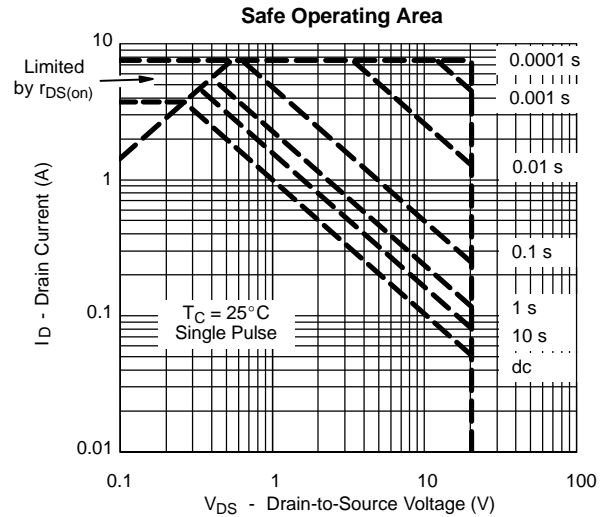
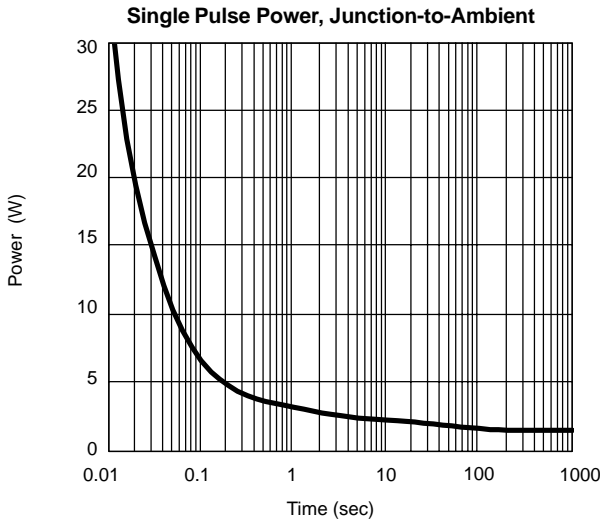


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**





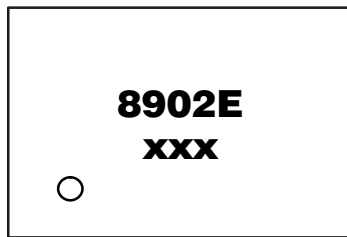
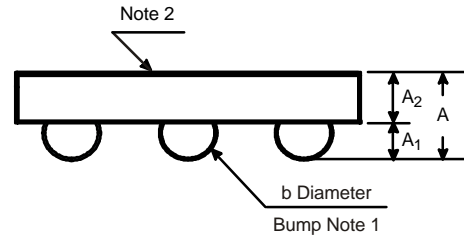
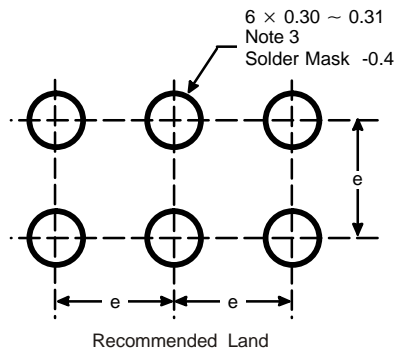
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



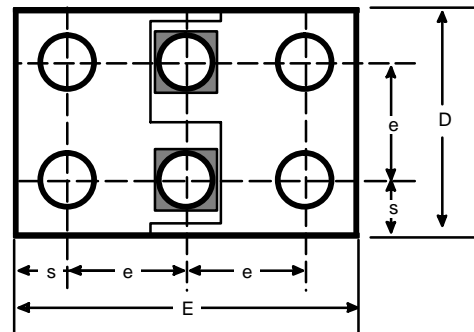


**PACKAGE OUTLINE**

**MICRO FOOT: 6-BUMP (2 X 3, 0.8-mm PITCH)**



Mark on Backside of Die



NOTES (Unless Otherwise Specified):

1. 6 solder bumps are Eutetic 63Sn/37Pb with diameter 0.37 - 0.41 mm
2. Backside surface is coated with a Ag/Ni/Ti layer
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
A	0.600	0.650	0.0236	0.0256
A <sub>1</sub>	0.260	0.290	0.102	0.114
A <sub>2</sub>	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
s	0.380	0.400	0.0150	0.0157

\* Use millimeters as the primary measurement.