FAIRCHILD SEMICONDUCTOR™

September 1986
Revised February 2000

DM74ALS374
Octal 3-STATE D-Type Edge-Triggered Flip-Flop

General Description

This 8-bit register features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provides this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. It is particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the DM74ALS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

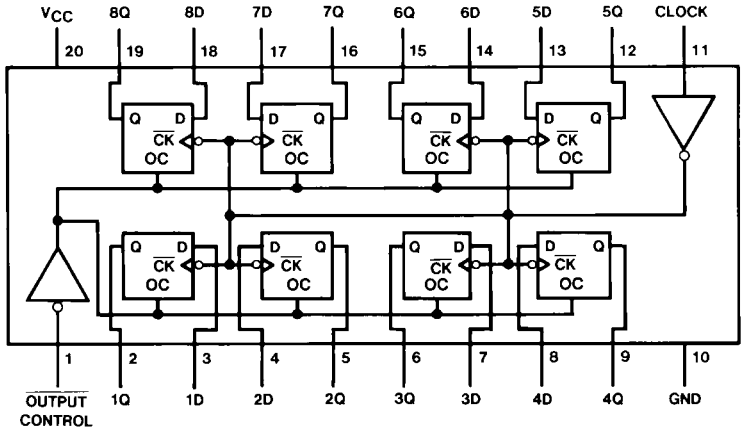
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS TTL counterpart
- Improved AC performance over DM74LS374 at approximately half the power
- 3-STATE buffer-type outputs drive bus lines directly

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74ALS374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

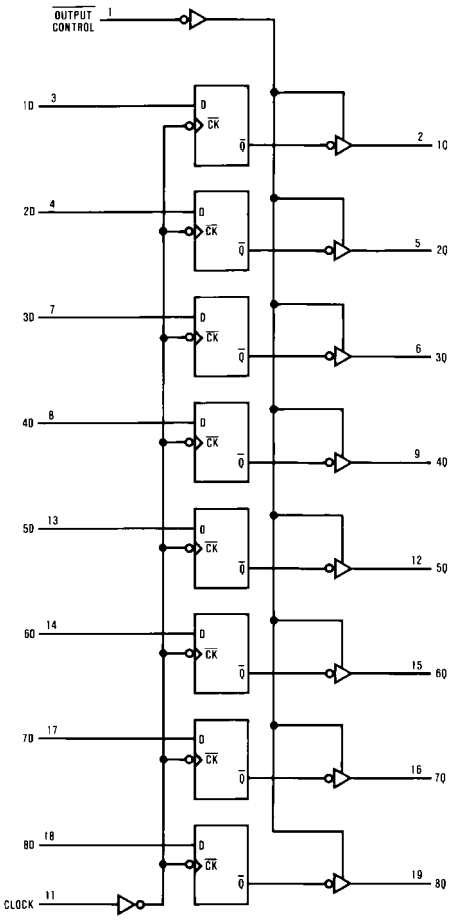


Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = LOW State
H = HIGH State
X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range (Note 2)	−65°C to +150°C
Typical θ_{JA}	
N Package	60.0°C/W
M Package	79.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: This product meets application requirements of 500 temperature cycles from −65°C to +150°C.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−2.6	mA
I_{OL}	LOW Level Output Current				24	mA
f_{CLOCK}	Clock Frequency		0		35	MHz
t_W	Width of Clock Pulse	HIGH	14			ns
		LOW	14			ns
t_{SU}	Data Setup Time (Note 3)		10↑			ns
t_H	Data Hold Time (Note 3)		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 3: The (↑) arrow indicates the positive edge of the Clock is used for reference.

DC Electrical Characteristics

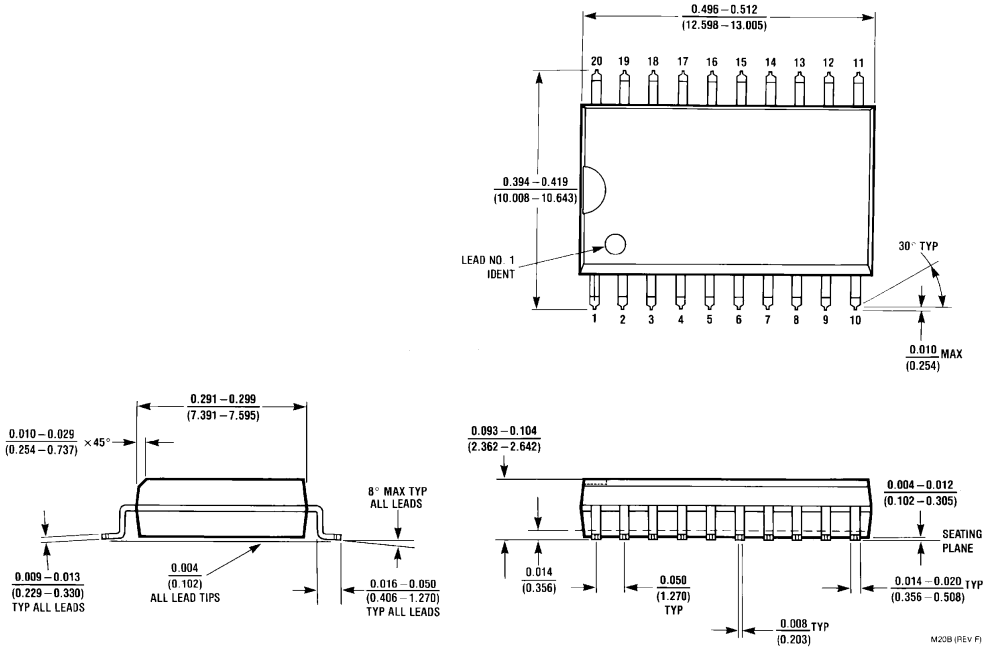
over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = 4.5V$	I_{OH} = Max	2.4	3.2		V
		$V_{CC} = 4.5V$ to 5.5V	$I_{OH} = -400$ µA	$V_{CC} - 2$			V
V_{OL}	LOW Level Output Voltage	$V_{CC} = 4.5V$	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	µA
I_{IL}	LOW Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$				−0.2	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$	$V_O = 2.25V$	−30		−112	mA
I_{OZH}	OFF-State Output Current, HIGH Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 2.7V$				20	µA
I_{OZL}	OFF-State Output Current, LOW Level Voltage Applied	$V_{CC} = 5.5V$, $V_O = 0.4V$				−20	µA
I_{CC}	Supply Current	$V_{CC} = 5.5V$ Outputs Open	Outputs HIGH		11	19	mA
			Outputs LOW		19	28	mA
			Outputs Disabled		20	31	mA

AC Electrical Characteristics

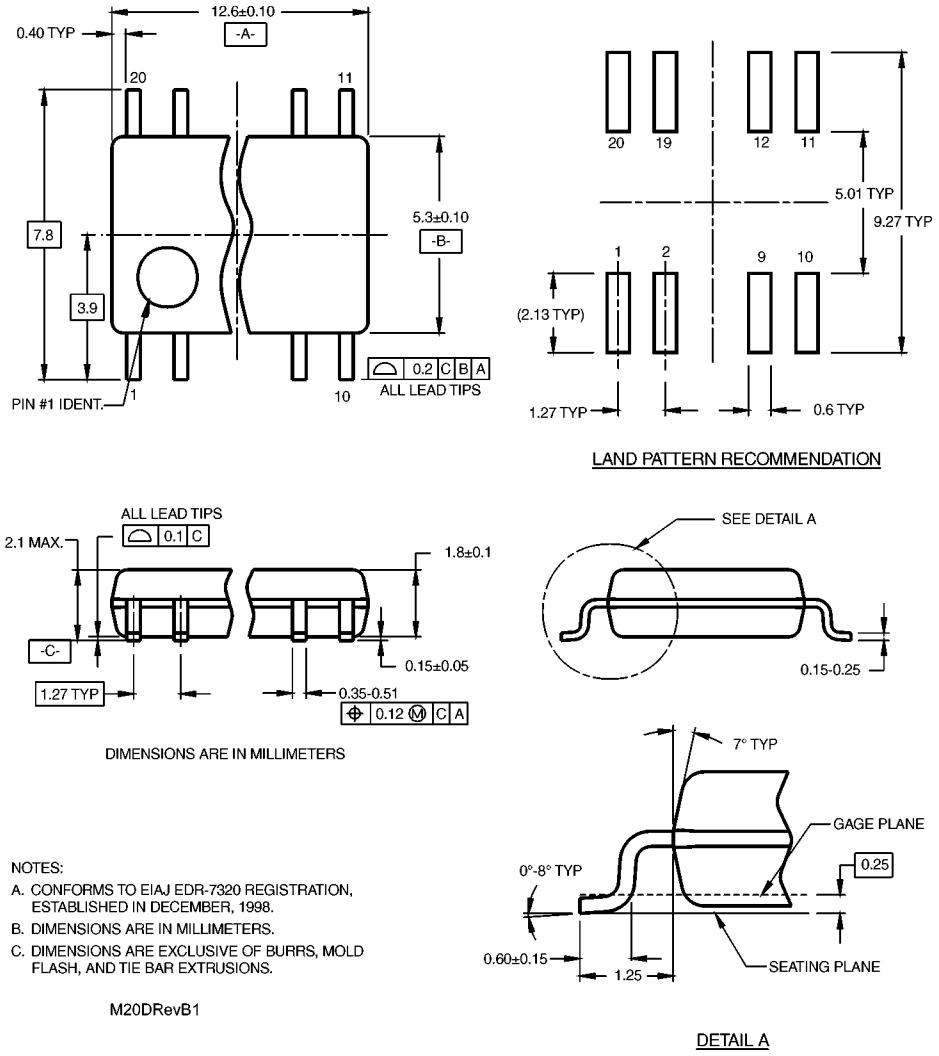
Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V			35		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	R_L = 500Ω C_L = 50 pF	Clock	Any Q	3	12	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		Clock	Any Q	5	16	ns
t_{PZH}	Output Enable Time to HIGH Level Output		Output Control	Any Q	5	17	ns
t_{PZL}	Output Enable Time to LOW Level Output		Output Control	Any Q	7	18	ns
t_{PHZ}	Output Disable Time from HIGH Level Output		Output Control	Any Q	2	10	ns
t_{PLZ}	Output Disable Time from LOW Level Output		Output Control	Any Q	3	18	ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

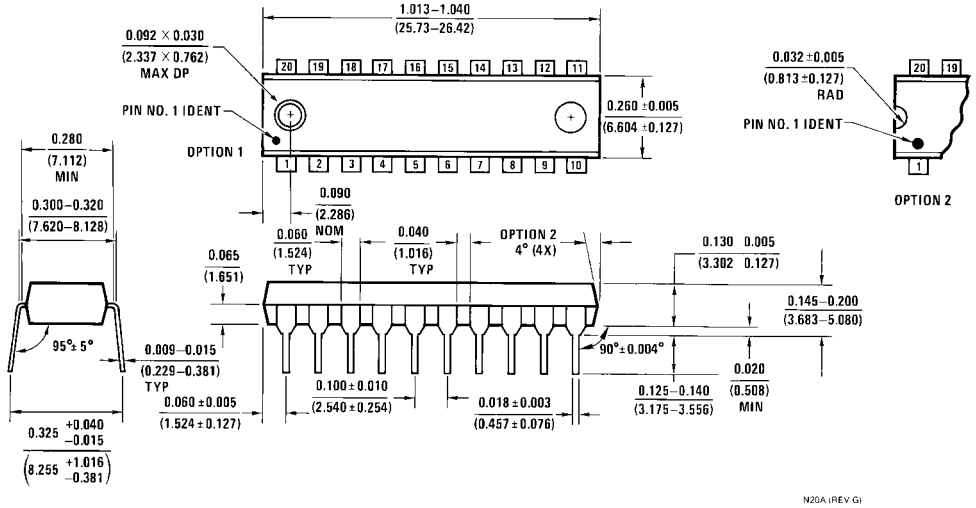
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A