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SL1613

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613 is a bipolar monolithic integrated circuit wideband amplifier intended for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The device provides amplification, limiting and rectification, is suitable for direct coupling and incorporates supply line decoupling. The mid-band voltage gain of the SL1613 is typically 12dB.

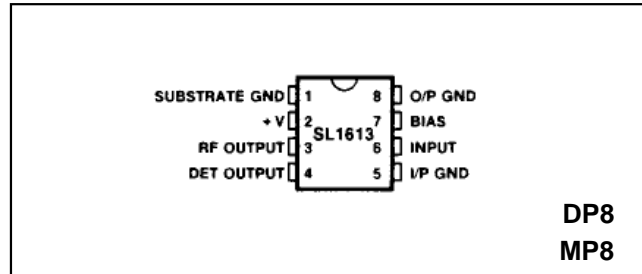


Fig.1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P impedance
- Low O/P impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Field Strength Meters

ABSOLUTE MAXIMUM RATINGS

| | |
|-------------------------------|-----------------|
| Storage temperature range | -55°C to +150°C |
| Operating temperature range | -30°C to +85°C |
| Thermal resistance | |
| Chip-to-ambient | |
| SL1613 DP | 111°C/W |
| SL1613 MP | 163°C/W |
| Chip-to-case | |
| SL1613 DP | 71°C/W |
| SL1613MP | 57°C/W |
| Maximum instantaneous voltage | |
| at video output | +12V |
| Supply voltage | 9V |

ORDERING INFORMATION

SL1613 C DP
SL1613 C MP

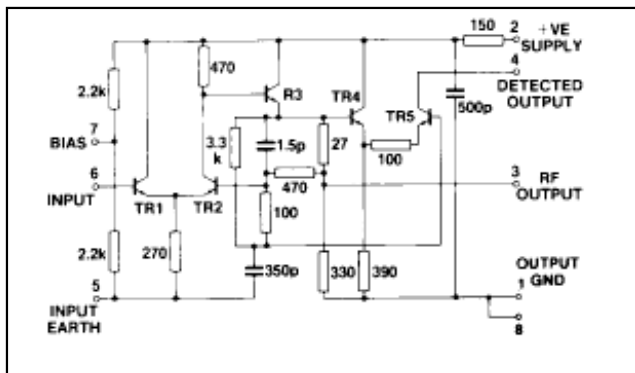


Fig.2 Circuit diagram

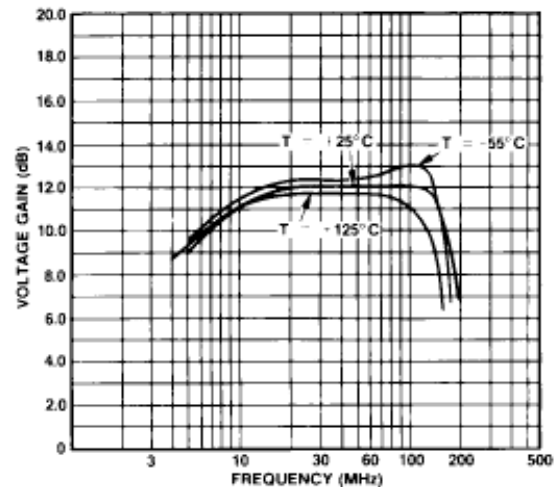


Fig.3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following condiotns (unless otherwise stated)

- TA = +22°C ±2°C
- Supply voltage = +6V
- DC connection between input and bias pins

| Characteristic | Value | | | Units | Conditions |
|---|-------|------|------|-------|---|
| | Min. | Typ. | Max. | | |
| Voltage gain | 10 | 12 | 14 | dB | f = 30MHz, R _s = 10Ω, C _L = 8pF |
| Upper cut-off frequency (Fig. 3) | | 150 | | MHz | R _s = 10Ω, C _L = 8pF |
| Lower cut-off frequency (Fig. 3) | | 5 | | MHz | R _s = 10Ω, C _L = 8pF |
| Propagation delay | | 2 | | ns | |
| Max. rectified video output current (Fig. 4 and 5) | 0.8 | 1 | 1.4 | mA | f = 60MHz, V _{IN} = 500mV rms |
| Variation of gain supply voltage | | 0.7 | | dB/V | |
| Variation of maximum rectified output current with supply voltage | | 25 | | %/V | |
| Maximum input signal before overload | | 1.9 | | V rms | See Note 1 |
| Noise figure (Fig. 6) | | 4.5 | | dB | f = 60MHz, R _s = 450Ω |
| Maximum RF output voltage | | 1.2 | | Vp-p | |
| Supply current | | 1.5 | 20 | mA | |

Note 1. Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction of TR1 on peaks

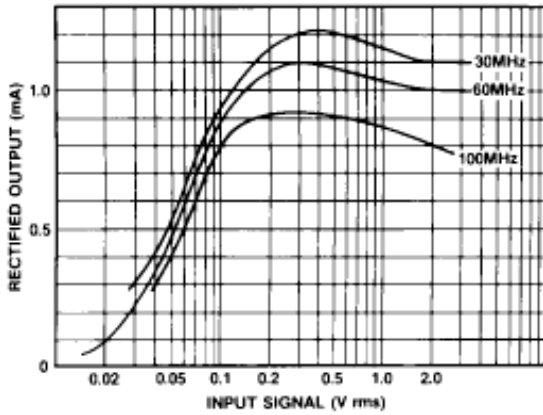


Fig.4 Rectified output current v. input signal

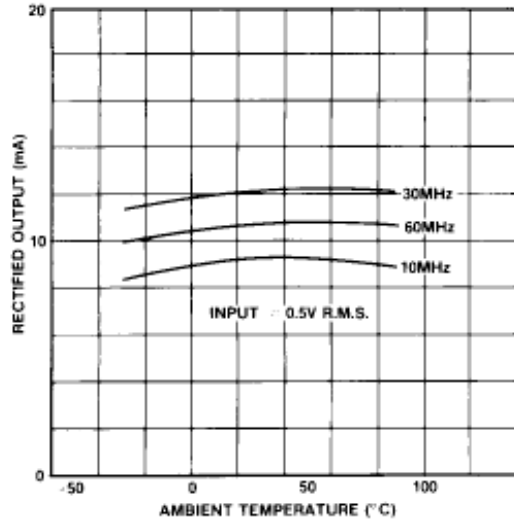


Fig.5 Maximum rectified output current v. temperature

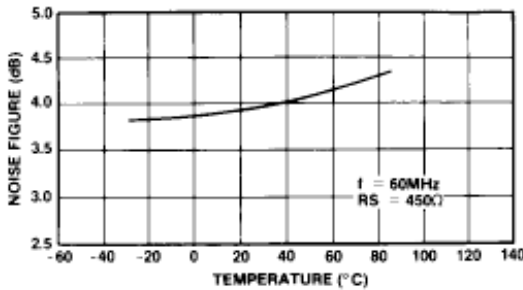


Fig.6 Typical figure v. temperature

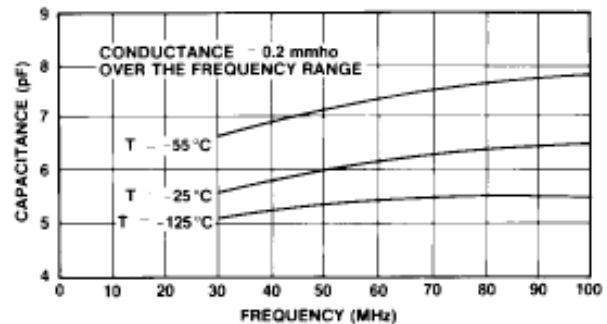


Fig.7 Input admittance with open circuit output

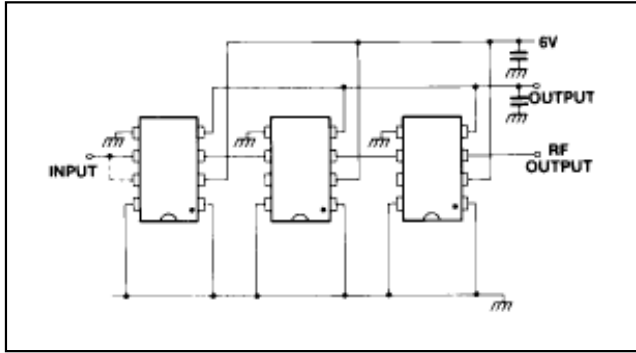


Fig.8 Direct coupled amplifiers

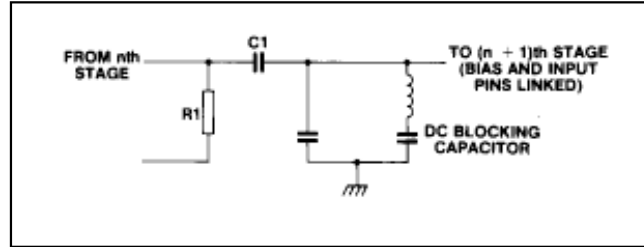


Fig.9 Suitable interstage tuned circuit

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

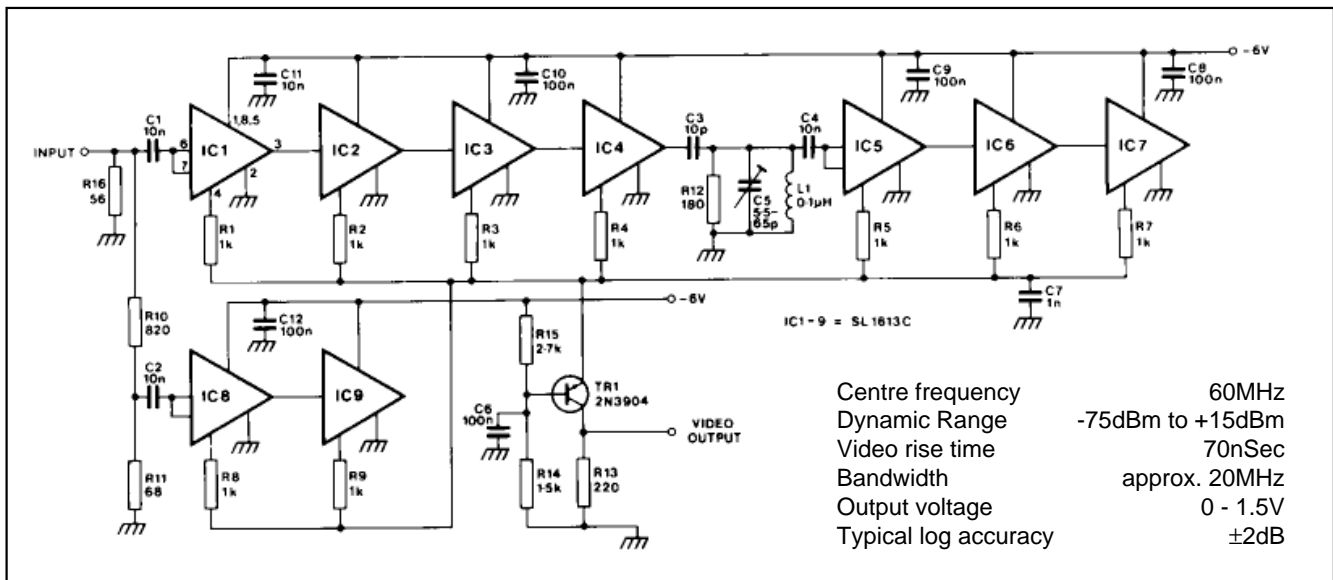
Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple parallel or series circuit cannot be used. This choice of network is also controlled by the need to avoid distorting the logarithmic law: the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A single capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required. Values of supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two ground leads to avoid the introduction of common ground lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

| | Number of stages | | | |
|---------------------|------------------|------|-----|-----|
| | 6 or more | 5 | 4 | 3 |
| Minimum capacitance | 30nF | 10nF | 3nF | 1nF |

The on-chip 500pF supply decoupling capacitor has a resistance of, typically 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V. (See Absolute Maximum Ratings).



Centre frequency 60MHz
 Dynamic Range -75dBm to +15dBm
 Video rise time 70nSec
 Bandwidth approx. 20MHz
 Output voltage 0 - 1.5V
 Typical log accuracy ±2dB

Fig.10 Circuit diagram of low strip



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