GEC PLESSEY
SEMICONDUCTORS

ADVANCE INFORMATION

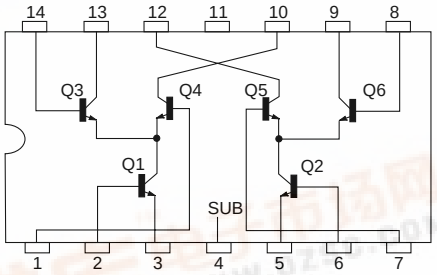
DS 3305 -2.0

SL2364

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2364 is an array of transistors internally connected to form a dual long-tailed pair with tail transistors. This is a monolithic integrated circuit manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2364 is in a 14 SO package and a high performance Dilmon encapsulation.



SL2364C

DC14
MP14

Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package
- Very High f_T - Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed of the following conditions (unless otherwise stated):

T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} / T_{AMB}		-1.7		mV/°C	I_C Tail) = 8mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to | V_{BEQ3} - V_{BEQ4} | and | V_{BEQ5} - V_{BEQ6} |

TYPICAL CHARACTERISTICS

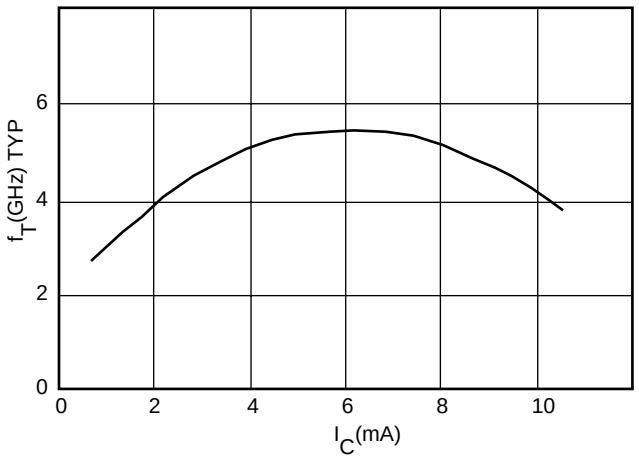


Fig. 2 Collector current

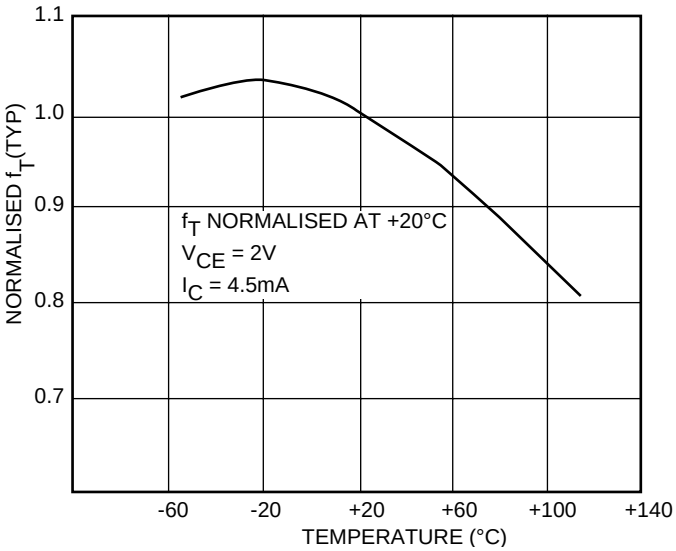


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature -55°C to + 150°C
Maximum junction temperature + 150°C
Package thermal resistance (°C/W):
Chip to case 45 (MP14) 35 (DC14)
Chip to ambient 123 (MP14) 120 (DC14)
VCBO = 10V, VEBO = 2 5V VCEO = 6V. VCIO = 15V IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.