MITEL
SEMICONDUCTOR

SL6679

Direct Conversion FSK Data Receiver

Preliminary Information

Supersedes September 1996 version, DS4410 - 1.5　　DS4410 - 2.1　April 1998

The SL6679 is an advanced Direct Conversion FSK Data Receiver for operation up to 450 MHz. The device integrates all functions to convert a binary FSK modulated RF signal into a demodulated data stream.

Adjacent channel rejection is provided using tuneable gyrator filters. RF and audio AGC functions assist operation when large interfering signals are present and an automatic frequency control (AFC) function is provided to extend centre frequency acceptance.

FEATURES

- Very Low Power Operation from Single Cell
- Superior Sensitivity
- Operation at 512, 1200 and 2400 Baud
- On Chip 1 Volt Regulator
- 1mm Height Miniature Package
- Automatic Frequency Control Function
- Programmable Post Detection Filter
- AGC Detection Circuitry
- Power Down Function
- Battery Strength Indicator

APPLICATIONS

- Pagers, including Credit Card, PCMCIA and Watch Pagers
- Low Data Rate Receivers, e.g. Security Systems

ORDERING INFORMATION

SL6679/KG/TP1N	1mm TQFP device, baked and dry packed, supplied in trays
SL6679/KG/TP1Q	1mm TQFP device, baked and dry packed, supplied in tape and reel

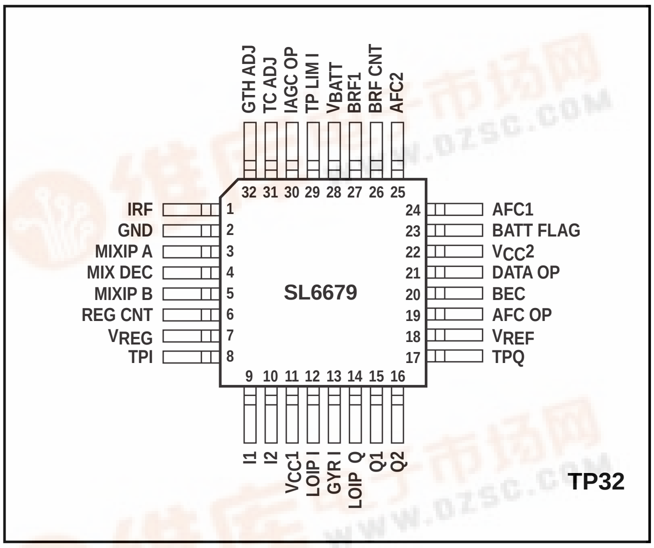


Fig. 1 Pin identification diagram (top view). See Table 1 for pin descriptions

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Operating temperature	−10°C to +55°C
Maximum voltage on any pin w.r.t. any other pin, subject to the following conditions:	+4V
Current, pin 3 (MIXIP), pin 5 (MIXPB), pin 12 (LOIPI) and pin 14 (LOIPB)	<5ma
Most negative voltage on any pin	−0·5V w.r.t. gnd

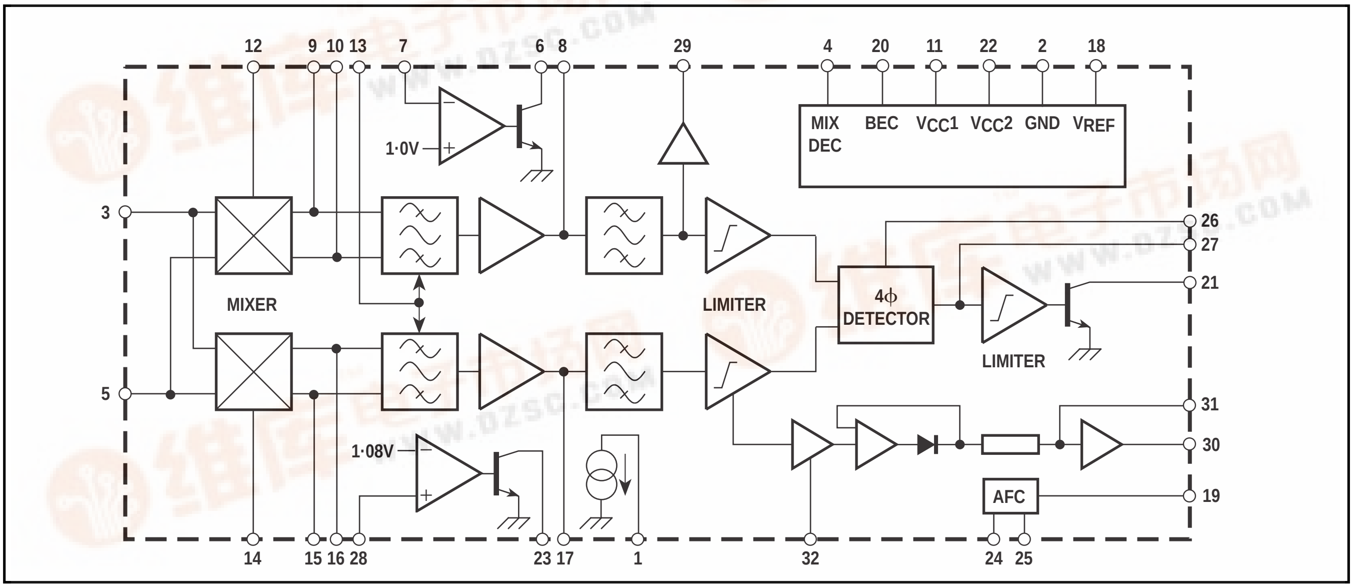


Fig. 2 Block diagram of SL6679

Pin number	Pin name	Pin description
1	IRF	LNA current source
2	GND	Ground
3	MIXIP A	Mixer input A
4	MIX DEC	Mixer biasing decouple
5	MIXIP B	Mixer input B
6	REG CNT	1V regulator control external PNP drive
7	VREG	1V regulator output voltage
8	TPI	I channel pre-gyrator filter test point.
9	I1	Mixer output, I channel
10	I2	Mixer output, I channel
11	VCC1	Positive supply 1
12	LOIP I	LO input channel I
13	GYRI	Gyrator current adjust pin
14	LOIP Q	LO input channel Q
15	Q1	Mixer output, Q channel
16	Q2	Mixer output, Q channel
17	TPQ	Q channel pre-gyrator filter test point
18	VREF	Reference voltage
19	AFC OP	AFC output
20	BEC	Battery economy control
21	DATA OP	Data output pin
22	VCC2	Positive supply 2
23	BATT FLAG	Battery flag output
24	AFC1	AFC characteristic defining pin
25	AFC2	AFC characteristic defining pin
26	BRF CNT	Bit rate filter control
27	BRF1	Bit rate filter 1, output from detector
28	VBATT	Battery flag input voltage
29	TP LIM I	I channel limiter (post gyrator filter) test point, output only
30	IAGC OP	Audio AGC output current
31	TC ADJ	Audio AGC time constant adjust
32	GTH ADJ	Audio AGC gain and threshold adjust. RSSI signal indicator

Table 1 SL6679 pin descriptions

ELECTRICAL CHARACTERISTICS (1)

Electrical Characteristics (1) are guaranteed over the following range of operating conditions unless otherwise stated
T_{AMB} = +25°C, $V_{CC}1$ = 1·3V, $V_{CC}2$ = 2·7V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, $V_{CC}1$	11	0·95	1·3	2·7	V	$V_{CC}1 \leqslant V_{CC}2 - 0{\cdot}8V$
Supply voltage, $V_{CC}2$	22	1·9	2·7	3·5	V	
Supply current, $I_{CC}1$	11	1·20	1·60	2·2	mA	Including IRF
Supply current, $I_{CC}2$	22	260	390	490	µA	
1 volt regulator, V_{REG}	7	0·95	1·0	1·05	V	I_{LOAD} = 3mA, external PNP($\beta \geqslant 100$, V_{CE} = 0·1V)
1 volt regulator load current	7	0·25		3	mA	External PNP ($h_{FE} \geqslant 100$, V_{CE} = 0·1V)
LNA current source, IRF	1	375	500	700	µA	PTAT, voltage on pin 1 = 0·3V and 1·3V
Reference voltage, V_{REF}	18	1·15	1·25	1·31	V	Typical temperature coefficient = +0·1mV/°C
V_{REF} source current	18			20	µA	
V_{REF} sink current	18			1·0	µA	
Data Amplifier						
DATA OP sink current	21	25			µA	Output logic low, pin 21 voltage = 0·3V
DATA OP leakage current	21			1·0	µA	Output logic high, pin 21 voltage = $V_{CC}2$
Output mark:space ratio	21	7:9		9:7		Preamble at 1200 baud, Δf = 4kHz, pin 26 = 0V, BRF capacitor = 560pF, DATA OP pullup resistor = 200kΩ
Battery Economy						
Power down $I_{CC}1$	11		0·5	10	µA	Pin 20 = logic low
Power down $I_{CC}2$	22		2·0	10	µA	Pin 20 = logic low
BEC input logic high	20	$V_{CC}2 - 0{\cdot}3V$		$V_{CC}2$	V	Powered up
BEC input logic low	20	0		0·3	V	Powered down
BEC input current	20	−1·0		1·0	µA	Powered up
BEC input current	20	−1·0		1·0	µA	Powered down
Battery Flag						
V_{BATT} trigger point	28	1·04	1·08	1·12	V	Current sunk by pin 23 = 1µA
BATT FLAG sink current	23			1·0	µA	Pin 28 voltage = 1·04V
BATT FLAG sink current	23	1·0			µA	Pin 28 voltage = 1·12V
BATT FLAG sink current	23	25			µA	Pin 28 voltage = 1·14V
V_{BATT} input voltage	28			2·0	V	
V_{BATT} input current	28	−1·0		1·0	µA	V_{BATT} = 1·14V
V_{BATT} input current	28	−1·0		1·0	µA	V_{BATT} = 1·04V

Continued…

ELECTRICAL CHARACTERISTICS (1) (Cont.)

Electrical Characteristics (1) are guaranteed over the following range of operating conditions unless otherwise stated

T_{AMB} = +25°C, $V_{CC}1$ = 1·3V, $V_{CC}2$ = 2·7V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Mixers						
LO DC bias voltage	12,14		$V_{CC}1$		V	
Gain to TPI	3,5,8,12	38	42	46	dB	LO inputs (12, 14) driven in quadrature: 45mVrms at 450MHz, CW. Mixer inputs (3, 5) driven differentially: 0·45mVrms at 450·004MHz, CW.
Gain to TPQ	3,5,14, 17	38	42	46	dB	As gain to TPI
Match of gain to TPI and TPQ	3,5,8, 12,14,17	−1	0	+1	dB	As gain toTPI
Audio AGC						
IAGC OP max. sink current	30		45		µA	TPI, TPQ signals limiting
IAGC OP leakage current	30			1	µA	No signal applied
AFC						
AFC DC current, I_{AFC4k5}	19		0·0		µA	$f_C = f_{LO}$+4·5kHz, CW
AFC DC current	19	I_{AFC4k5} +0·2	I_{AFC4k5} +0·7		µA	$f_C = f_{LO}$+2·5kHz, CW
AFC DC current	19		I_{AFC4k5} −0·9	I_{AFC4k5} −0·2	µA	$f_C = f_{LO}$+6·5kHz, CW
Bit Rate Filter Control						
BRF CNT input logic high	26	$V_{CC}2$ −0·3		$V_{CC}2$	V	2400 baud
BRF CNT input logic low	26	0		0·1	V	1200 baud
Tristate I/P current window	26	−0·4		+0·4	µA	512 baud
BRF 1 output current	27		3·5		µA	Pin 26 logic high
BRF 1 output current	27		1·7		µA	Pin 26 logic low
BRF 1 output current	27		0·74		µA	Pin 26 logic tristate (open circuit)
BRF CNT input high current	26	−7·5		+15	µA	
BRF CNT input low current	26	−7·5		+7·5	µA	

ELECTRICAL CHARACTERISTICS (2)

Electrical Characteristics (2) are guaranteed over the following range of operating conditions unless otherwise stated. Characteristics are tested at room temperature only and are guaranteed by characterisation test or design.

$T_{AMB} = -10°C$ to $+55°C$, $V_{CC}1 = 1{\cdot}4V$ to $2{\cdot}0V$, $V_{CC}2 = 2{\cdot}3V$ to $3{\cdot}2V$. $V_{CC}1 < V_{CC}2 - 0{\cdot}8V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage, $V_{CC}1$	11	0·95	1·3	2·7	V	$V_{CC}1 \leqslant V_{CC}2 - 0{\cdot}8V$ at $\geqslant 25°C$ only
Supply voltage, $V_{CC}2$	22	1·9	2·7	3·5	V	
Supply current, $I_{CC}1$	11		1·60	2·4	mA	Including IRF
Supply current, $I_{CC}2$	22		350	510	µA	
1 volt regulator, V_{REG}	7	0·93	1·0	1·05	V	I_{LOAD} = 3mA, external PNP($\beta \geqslant 100$, V_{CE} = 0·1V)
1 volt regulator load current	7	0·25		3	mA	External PNP($h_{FE} \geqslant 100$, V_{CE} = 0·1V)
LNA current source, IRF	1	375	500	800	µA	PTAT, voltage on pin 1 = 0·3V and 1·3V
Reference voltage, V_{REF}	18	1·13	1·25	1·33	V	Typical temperature coefficient = +0·1mV/°C
V_{REF} source current	18			18	µA	
V_{REF} sink current	18			0·8	µA	
Turn-on time			9		ms	Stable data O/P when 3dB above sensitivity. C_{VREF} = 2·2µF
Turn-off time			2		ms	Fall to 10% of steady state $I_{CC}1$. C_{VREF} = 2·2µF
Data Amplifier						
DATA OP sink current	21	22			µA	Output logic low, pin 21 voltage = 0·3V
DATA OP leakage current	21			1·5	µA	Output logic high, pin 21 voltage = $V_{CC}2$
Output mark:space ratio	21	7:9		9:7		Preamble at 1200 baud, Δf = 4kHz, pin 26 = 0V, BRF capacitor = 560pF, DATA OP pullup resistor = 200kΩ
Battery Economy						
Power down $I_{CC}1$	11		0·5	12	µA	Pin 20 = logic low
Power down $I_{CC}2$	22		2·0	12	µA	Pin 20 = logic low
BEC input logic high	20	$V_{CC}2 - 0{\cdot}3V$		$V_{CC}2$	V	Powered up
BEC input logic low	20	0		0·3	V	Powered down
BEC input current	20	−1·5		1·5	µA	Powered up
BEC input current	20	−1·5		1·5	µA	Powered down
Battery Flag						
V_{BATT} trigger point	28	1·04	1·08	1·12	V	Current sunk by pin 23 = 1µA
BATT FLAG sink current	23			2	µA	Pin 28 voltage = 1·04V
BATT FLAG sink current	23	2			µA	Pin 28 voltage = 1·12V
BATT FLAG sink current	23	20			µA	Pin 28 voltage = 1·14V
V_{BATT} input voltage	28			2·0	V	
V_{BATT} input current	28	−1·5		1·5	µA	V_{BATT} = 1·14V
V_{BATT} input current	28	−1·5		1·5	µA	V_{BATT} = 1·04V

Continued…

ELECTRICAL CHARACTERISTICS (2) (Cont.)

Electrical Characteristics (2) are guaranteed over the following range of operating conditions unless otherwise stated. Characteristics are tested at room temperature only and are guaranteed by characterisation test or design.

T_{AMB} = −10°C to +55°C, $V_{CC}1$ = 1·4V to 2·0V, $V_{CC}2$ = 2·3V to 3·2V. $V_{CC}1 < V_{CC}2 - 0{\cdot}8V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Mixers						
LO DC bias voltage	12,14		$V_{CC}1$		V	
Gain to TPI	3,5,8,12	35	42	46	dB	LO inputs (12, 14) driven in quadrature: 45mVrms at 450MHz, CW. Mixer inputs (3, 5) driven differentially: 0·45mVrms at 450·004MHz, CW.
Gain to TPQ	3,5,14, 17	35	42	46	dB	As gain to TPI
Match of gain to TPI and TPQ	3,5,8, 12,14,17	−1·5	0	+1·5	dB	As gain toTPI
Audio AGC						
IAGC OP max. sink current	30	30	45	70	µA	TPI, TPQ signals limiting
IAGC OP leakage current	30			1	µA	No signal applied
AFC						
AFC DC current, I_{AFC4k5}	19		0·0		µA	$f_C = f_{LO}$+4·5kHz, CW
AFC DC current	19	I_{AFC4k5} +0·1	I_{AFC4k5} +0·7		µA	$f_C = f_{LO}$+2·5kHz, CW
AFC DC current	19		I_{AFC4k5} −0·9	I_{AFC4k5} −0·1	µA	$f_C = f_{LO}$+6·5kHz, CW
Bit Rate Filter Control						
BRF CNT input logic high	26	$V_{CC}2$ −0·3		$V_{CC}2$	V	2400 baud
BRF CNT input logic low	26	0		0·1	V	1200 baud
Tristate I/P current window	26	−0·4		+0·4	µA	512 baud
BRF 1 output current	27		3·5		µA	Pin 26 logic high
BRF 1 output current	27		1·7		µA	Pin 26 logic low
BRF 1 output current	27		0·74		µA	Pin 26 logic tristate (open circuit)
BRF CNT input high current	26	−10		+10	µA	
BRF CNT input low current	26	−10		+10	µA	

RECEIVER CHARACTERISTICS (450MHz)

Receiver Characteristics (450MHz) are guaranteed over the following range of operating conditions unless otherwise stated. Characteristics are not tested but are guaranteed by characterisation test or design. All measurements made using the characterisation circuit Fig. 5. See Application Note AN137 for details of test method.

T_{AMB} = −10°C to +55°C, $V_{CC}1$ = 1·04V to 2·0V, $V_{CC}2$ = 2·3V to 3·2V, $V_{CC}1 < V_{CC}2 - 0{\cdot}8V$, carrier frequency = 450MHz, BER = 1 in 30, AFC open loop. LNA gain set such that an RF signal of −73dBm at the LNA input, offset from the LO by 4kHz, gives a typical IF signal level of 300mV p-p at TPI and TPQ. LNA noise figure < 2dB

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Sensitivity		−128		dBm	512bps, Δf = 4·5kHz
		−126	−122	dBm	1200bps, Δf = 4·0kHz
		−123	−119	dBm	2400bps, Δf = 4·5kHz. LO = −15dBm
Intermodulation, IP3		57		dB	512bps, Δf = 4·5kHz
	50	55		dB	1200bps, Δf = 4·0kHz
	48	53		dB	2400bps, Δf = 4·5kHz. LO = −15dBm. Channel spacing 25kHz
Adjacent Channel		70		dB	512bps, Δf = 4·5kHz
	62·5	69		dB	1200bps, Δf = 4·0kHz
	60	66		dB	2400bps, Δf = 4·5kHz. LO = −15dBm. Channel spacing 25kHz
Deviation Acceptance					
Up		+1·9		kHz	512bps, Δf = 4·5kHz, no AFC
Down		−2·5		kHz	512bps, Δf = 4·5kHz, no AFC
Up	+1·8	+3·0	+4·6	kHz	1200bps, Δf = 4·0kHz, no AFC
Down	−2·7	−2·3	−1·7	kHz	1200bps, Δf = 4·0kHz, no AFC
Up	+1·7	+2·5	+4·6	kHz	2400bps, Δf = 4·5kHz, no AFC
Down	−3	−2·3	−1·7	kHz	2400bps, Δf = 4·5kHz, no AFC
Centre Frequency Acceptance		±2·8		kHz	512bps, Δf = 4·5kHz, no AFC
	±2·0	±2·5	±2·9	kHz	1200bps, Δf = 4·0kHz, no AFC
	±2·0	±2·5	±3·2	kHz	2400bps, Δf = 4·5kHz, no AFC
AFC Capture Range (AFC Closed Loop)		±4		kHz	512bps, Δf = 4·5kHz. All at sensitivity +3dB or above
		±3·5		kHz	1200bps, Δf = 4·0kHz. All at sensitivity +3dB or above
		±4		kHz	2400bps, Δf = 4·5kHz. All at sensitivity +3dB or above

RECEIVER CHARACTERISTICS (280MHz)

Receiver Characteristics (280MHz) are guaranteed over the following range of operating conditions unless otherwise stated. Characteristics are not tested but are guaranteed by characterisation test or design. All measurements made using the characterisation circuit Fig. 5. See Application Note AN137 for details of test method.

T_{AMB} = −10°C to +55°C, $V_{CC}1$ = 1·04V to 2·0V, $V_{CC}2$ = 2·3V to 3·2V, $V_{CC}1 < V_{CC}2 - 0{\cdot}8V$, carrier frequency = 280MHz, BER = 1 in 30, AFC open loop. LNA gain set such that an RF signal of −73dBm at the LNA input, offset from the LO by 4kHz, gives a typical IF signal level of 300mV p-p at TPI and TPQ. LNA noise figure < 2dB

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Sensitivity		−129		dBm	512bps, Δf = 4·5kHz
	−128	−127	−124	dBm	1200bps, Δf = 4·0kHz
	−127	−124	−121	dBm	2400bps, Δf = 4·5kHz. LO = −15dBm
Intermodulation, IP3		57		dB	512bps, Δf = 4·5kHz
	52	56	60	dB	1200bps, Δf = 4·0kHz
	49	53·5	57	dB	2400bps, Δf = 4·5kHz. LO = −15dBm. Channel spacing 25kHz
Adjacent Channel		72		dB	512bps, Δf = 4·5kHz
	62·5	69	80	dB	1200bps, Δf = 4·0kHz
	60	60	77	dB	2400bps, Δf = 4·5kHz. LO = −15dBm. Channel spacing 25kHz
Deviation Acceptance					
Up		+1·9		kHz	512bps, Δf = 4·5kHz, no AFC
Down		−2·5		kHz	512bps, Δf = 4·5kHz, no AFC
Up	+1·8	+3·0	+4·6	kHz	1200bps, Δf = 4·0kHz, no AFC
Down	−3·8	−2·9	−1·7	kHz	1200bps, Δf = 4·0kHz, no AFC
Up	+1·7	+2·5	+4·6	kHz	2400bps, Δf = 4·5kHz, no AFC
Down	−3·0	−2·3	−1·7	kHz	2400bps, Δf = 4·5kHz, no AFC
Centre Frequency Acceptance		±3·1		kHz	512bps, Δf = 4·5kHz, no AFC
	±2·0	±2·9	±3·1	kHz	1200bps, Δf = 4·0kHz, no AFC
	±2·0	±2·5	±3·2	kHz	2400bps, Δf = 4·5kHz, no AFC
AFC Capture Range (AFC Closed Loop)		±4		kHz	512bps, Δf = 4·5kHz. All at sensitivity +3dB or above
		±3·5		kHz	1200bps, Δf = 4·0kHz. All at sensitivity +3dB or above
		±4		kHz	2400bps, Δf = 4·5kHz. All at sensitivity +3dB or above
1MHz Blocking		75		dB	512bps, Δf = 4·5kHz
	67	75	78	dB	1200bps, Δf = 4·0kHz
	65	73	76	dB	2400bps, Δf = 4·5kHz. LO = −15dBm
Mark:space amplitude modulation acceptance	20	23		dB	2400bps, R14 = 120kΩ (Fig. 5), room temperature only. See Note.

NOTE
The mark:space amplitude acceptance is the maximum amplitude ratio which can occur (for example due to Simulcast conditions) with 2400bps, using a POCSAG decoder with R14 = 120kΩ to achieve an 80% call rate and the lower amplitude set at a sensitivity of +20dB. the maxima and minima of the amplitude modulation correspond to the positive and negative (or vice versa) frequency shifts of the FSK modulation.

OPERATION OF SL6679

Low Noise Amplifier

To achieve optimum performance it is necessary to incorporate a Low Noise RF Amplifier at the front end of the receiver. This is easily biased using the on-chip voltages and current source provided. All voltages and current sources used for bias of the RF amplifier, receiver and mixers should be RF decoupled using 1nF capacitors. The receiver also requires a stable Local Oscillator at the required channel frequency.

Local Oscillator

The Local Oscillator signal is applied to the device in phase quadrature. This can be achieved with the use of two RC networks operating at their −3dB/45° transfer characteristic. The RC characteristics for I and Q channels are combined to give a full 90° phase differential between the LO ports of the device. Each LO port also requires an equal level of drive from the oscillator. This is achieved by forming the two RC networks into a power divider.

Gyrator Filters

The on-chip filters include an adjustable gyrator filter. This may be adjusted by changing the value of the resistor connected between pin 13 and GND. This allows adjustment of the filters' cutoff frequency and allows for compensation for possible process variations.

Audio AGC (Fig. 3)

The Audio AGC consists of a current sink which is controlled by the audio (baseband) signal. It has three parameters that may be controlled by the user. These are the attack (turn on) time, decay (duration) time and threshold level. The attack time is simply determined by the value of the external capacitor connected to TCADJ. The external capacitor is in series with an internal 100kΩ resistor and the time constant of this circuit dictates the attack time of the AGC.

$$\text{i.e. } t_{ATTACK} = 100k\Omega \times C18$$

The decay time is determined by the external resistor connected in parallel with the capacitor CTC. The decay time is simply

$$t_{DECAY} = R17 \times C18$$

When a large audio (baseband) signal is incident on the input to the AGC circuit, the variable current source is turned on. This causes a voltage drop across R13. The voltage potential between V_{REF} and the voltage on pin 31 causes a current to flow in pin 30. This charges up C18 through the 100kΩ internal resistor. As the voltage across the capacitor increases, a current source is turned on and this sinks current from pin 32. The current sink on pin 32 can be used to drive the external AGC circuit by causing a PIN diode to conduct, reducing the signal to the RF amplifier.

RF AGC

The RF AGC is an automatic gain control loop that protects the mixer's RF inputs, Pins 3 and 5, from large out of band RF signals. The loop consists of an RF received signal strength indicator which detect the signal at the inputs of the mixers. This RSSI signal is then used to control the LNA current source (pin 1).

Regulator

The on-chip regulator should be used in conjunction with a suitable PNP transistor to achieve regulation. As the transistor forms part of the regulator feedback loop the transistor should exhibit the following characteristics:

$$H_{FE} > 100 \text{ for } V_{CE} > = 0{\cdot}1V$$

If no external transistor is used, the maximum current sourcing capability of the regulator is limited to 30μA.

Automatic Frequency Control (Fig. 4)

The Automatic Frequency Control consists of a detection circuit which gives a current output at AFC OP whose magnitude and sign is a function of the difference between the local oscillator (f_{LO}) and carrier frequencies (f_C). This output current is then filtered by an off-chip integrating capacitor. The integrator's output voltage is used to control a voltage control crystal oscillator. This closes the AFC feedback loop giving the automatic frequency control function. For an FSK modulated incoming RF carrier, the AFC OP current's polarity is positive, i.e.current is sourced for $f_{LO}<f_C<f_{LO}+4kHz$ and negative, i.e. current is sunk, for $f_{LO}>f_C>f_{LO}-4kHz$. The magnitude of the AFC OP current is a function of frequency offset and the transmitted data's bit stream. If the carrier frequency, (f_C), equals the local oscillator frequency, (f_{LO}) then the magnitude of the current is zero.

BIT RATE FILTER CONTROL

The logic level on pin 26 controls the cutoff frequency of the 1st order bit rate for a given bit rate filter capacitor at pin 27. This allows the cutoff frequency to be changed between f_C, $2f_C$ and $0{\cdot}43f_C$ through the logic level on pin 26. This function is achieved by changing the value of the current in the 4ϕ detector's output stage. A logic zero (0V to 0·1V) on pin 26 gives a cutoff frequency of f_C a logic one ($V_{CC}2-0{\cdot}3V$ to $V_{CC}2$) gives a cut off frequency of $2f_C$ and an open circuit at pin 26 gives a cutoff frequency of $0{\cdot}43f_C$.

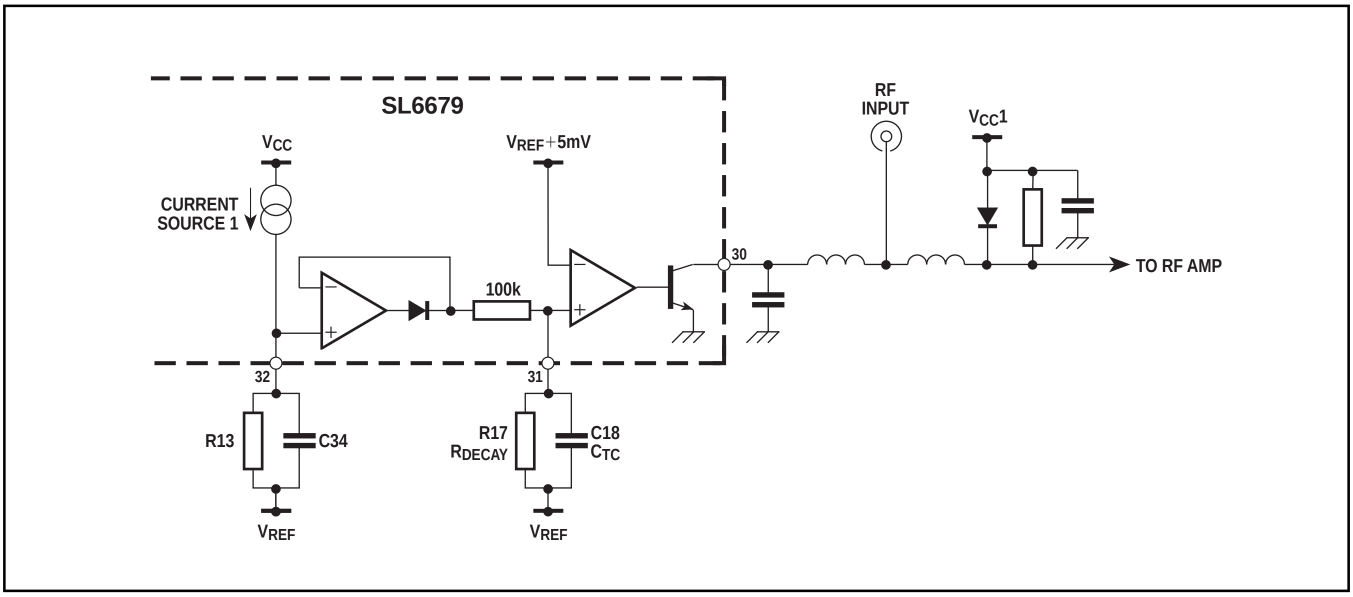


Fig.3 AGC schematic

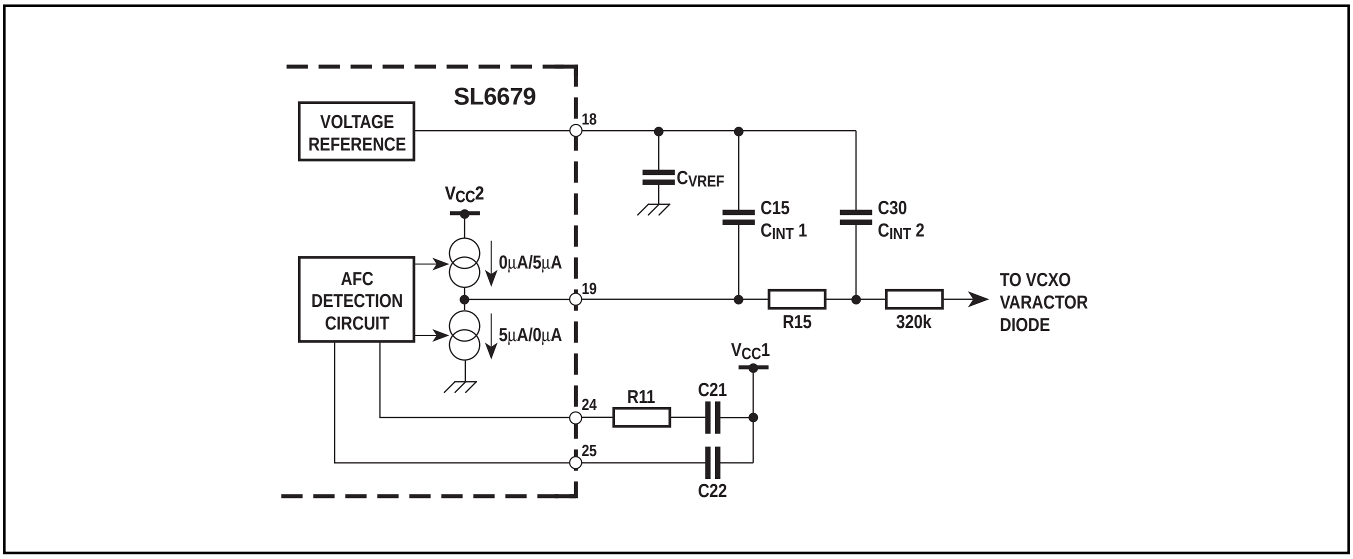


Fig. 4 AFC schematic

Peak deviation (kHz)	Baud rate (bps)	Component (Fig. 4)		
		C22	C21	R11
3·5	512, 1200, 2400	750pF	2·0nF	15kΩ
4	512, 1200, 2400	560pF	1·5nF	15kΩ
4·5	512, 1200, 2400	510pF	1·3nF	15kΩ
5	512, 1200, 2400	470pF	1·2nF	15kΩ
5·5	512, 1200, 2400	430pF	1·1nF	15kΩ

Table 2 AFC defining components

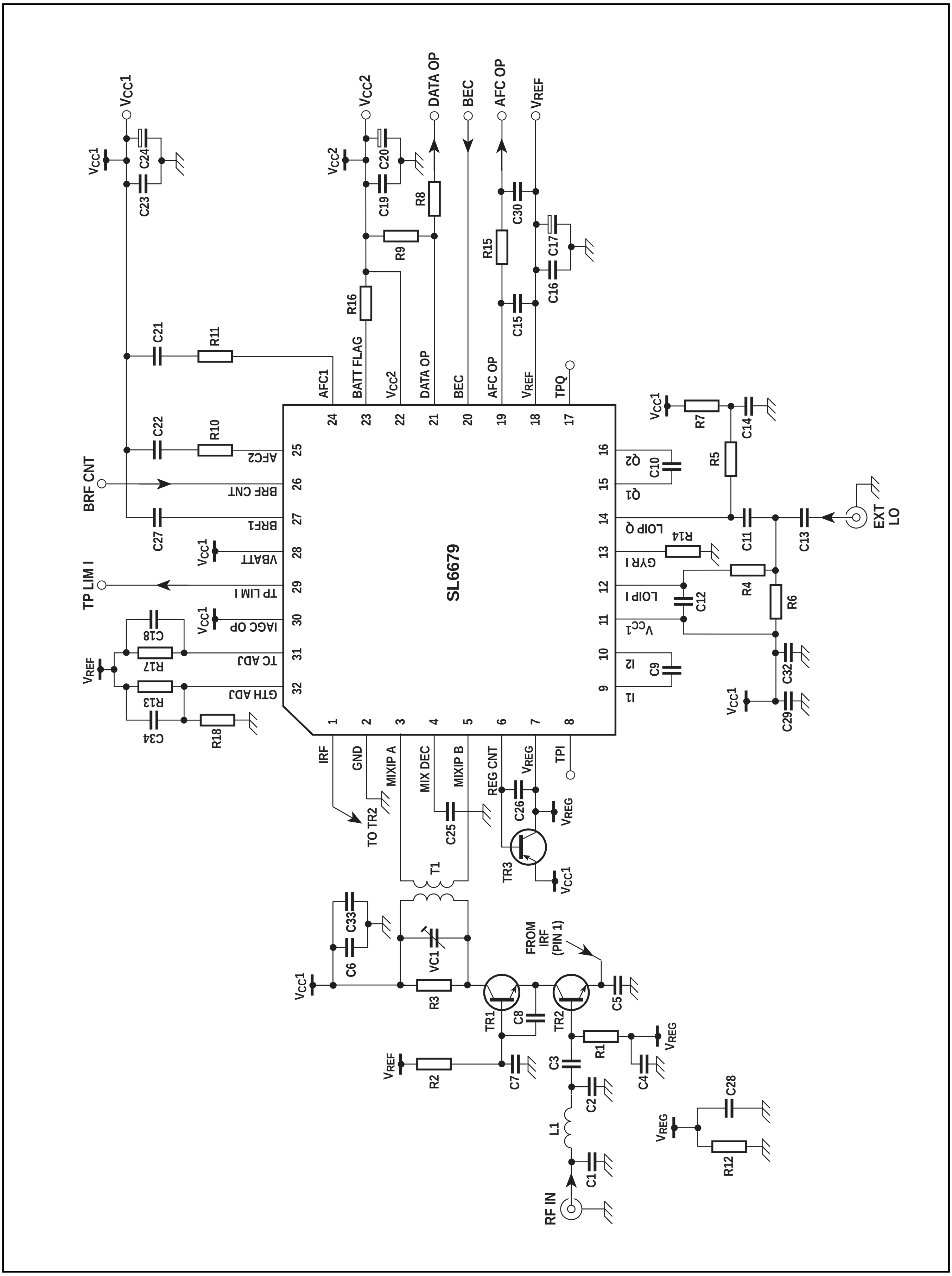


Fig. 5 SL6679 characterisation circuit (see Tables 3 and 4 for component values)

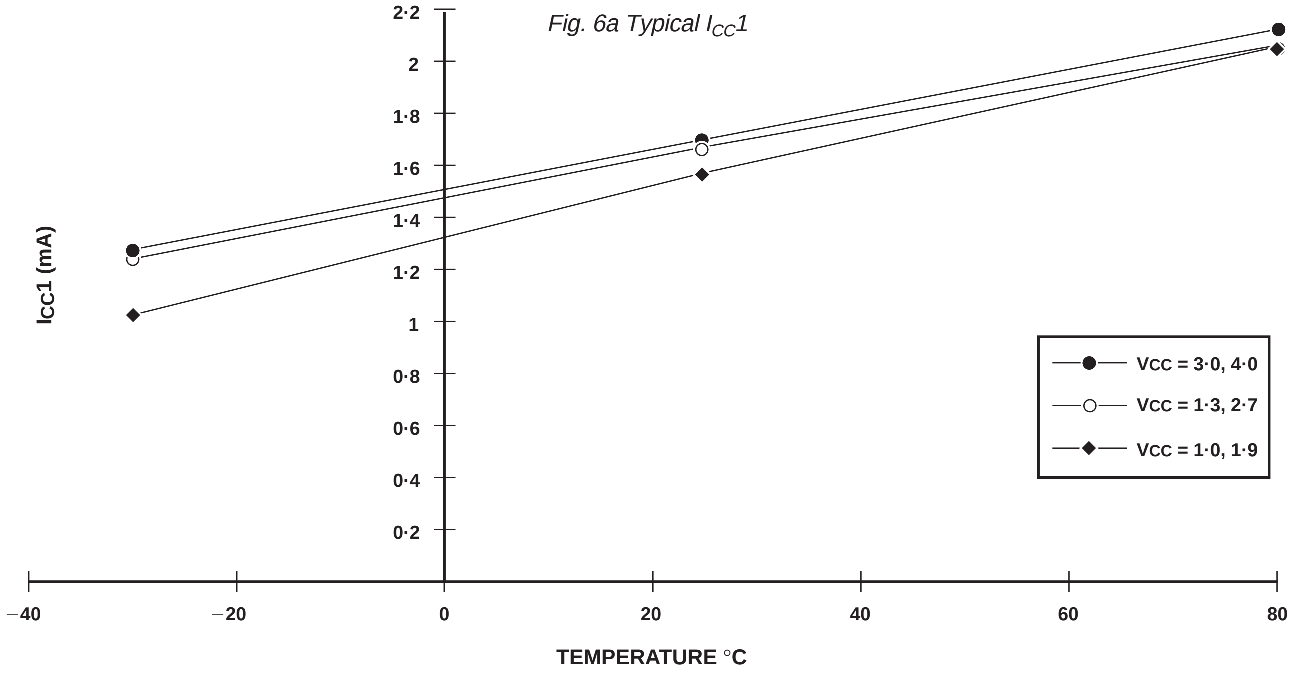
Resistors		Capacitors		Capacitors (cont.)		Inductors	
R1	4·7kΩ	C1	12pF	C18	100nF	L1	56nH
R2	4·7kΩ	C2	O/C	C19	1nF	T1	30nH 1:1, Coilcraft M1686-A
R3	1·5kΩ	C3	220nF	C20	2·2µF	**Transistors**	
R4	100Ω	C4	1nF	C21	1·5nF		
R5	100Ω	C5	1nF	C22	560pF	TR1	Toshiba 2SC5065
R6	100Ω	C6	1nF	C23	1nF	TR2	Toshiba 2SC5065
R7	100Ω	C7	1nF	C24	2·2µF	TR3	FMMT589 (Zetex ZTX550)
R8	430kΩ	C8	3·3pF	C25	100nF		
R9	220kΩ	C9	4·7nF	C26	100nF		
R10	S/C	C10	4·7nF	C27	560pF		
R11	15kΩ	C11	4·7pF	C28	1nF		
R12	2kΩ	C12	5·6pF	C29	1nF		
R13	39kΩ	C13	1nF	C30	1nF		
R14	180kΩ	C14	1nF	C32	100nF		
R15	430kΩ	C15	1nF	C33	100nF		
R16	220kΩ	C16	1nF	C34	100nF		
R17	220kΩ	C17	2·2µF	VC1	3-10pF		
R18	3·3MΩ						

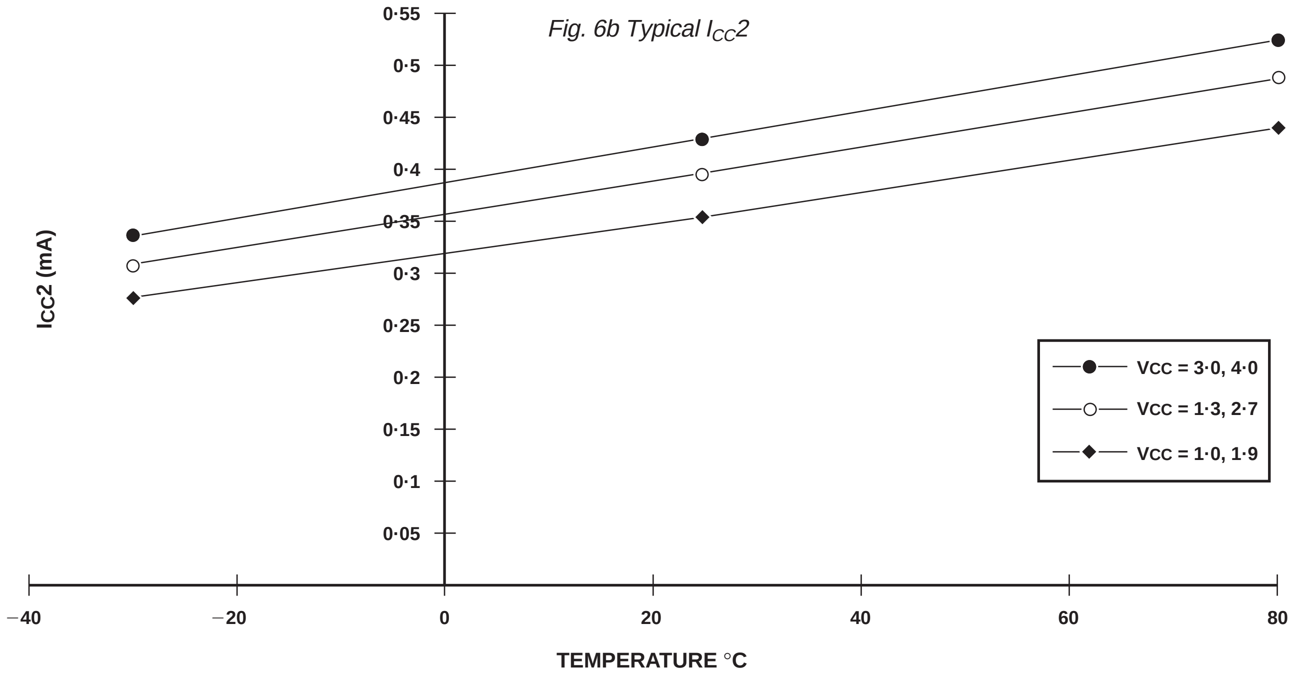
Table 3 Component list for 280MHz characterisation board

Resistors		Capacitors		Capacitors (cont.)		Inductors	
R1	4·7kΩ	C1	O/C	C18	100nF	L1	47nH
R2	4·7kΩ	C2	O/C	C19	1nF	T1	16nH 1:1, Coilcraft Q4123-A
R3	1·5kΩ	C3	1nF	C20	2·2µF	**Transistors**	
R4	100Ω	C4	1nF	C21	1·5nF		
R5	100Ω	C5	1nF	C22	560pF	TR1	Philips BFT25A
R6	100Ω	C6	1nF	C23	1nF	TR2	Philips BFT25A
R7	100Ω	C7	1nF	C24	2·2µF	TR3	FMMT589 (Zetex ZTX550)
R8	430kΩ	C8	3·3pF	C25	100nF		
R9	220kΩ	C9	4·7nF	C26	100nF		
R10	S/C	C10	4·7nF	C27	560pF		
R11	15kΩ	C11	3·9pF	C28	1nF		
R12	2kΩ	C12	3·3pF	C29	1nF		
R13	39kΩ	C13	1nF	C30	1nF		
R14	180kΩ	C14	1nF	C32	100nF		
R15	430kΩ	C15	1nF	C33	100nF		
R16	220kΩ	C16	1nF	C34	100nF		
R17	220kΩ	C17	2·2µF	VC1	3-10pF		
R18	3.3MΩ						

Table 4 Component list for 450MHz characterisation board

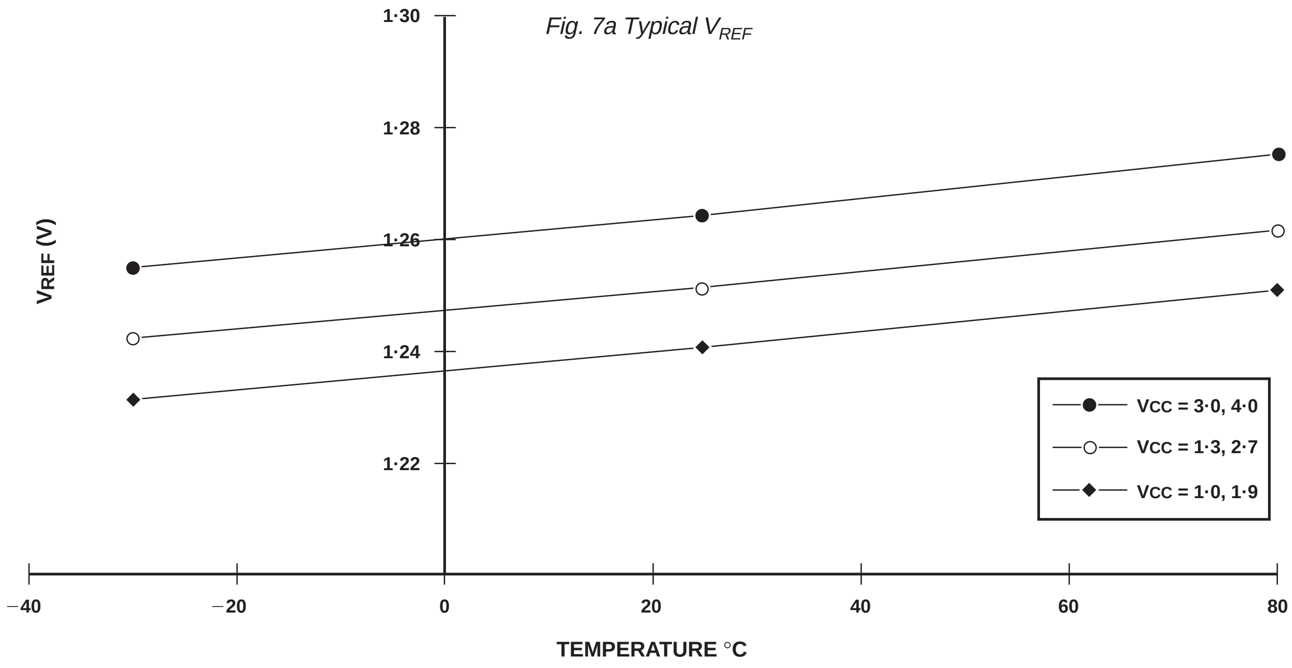
TYPICAL DC PARAMETERS (FIGS. 6 TO 8)

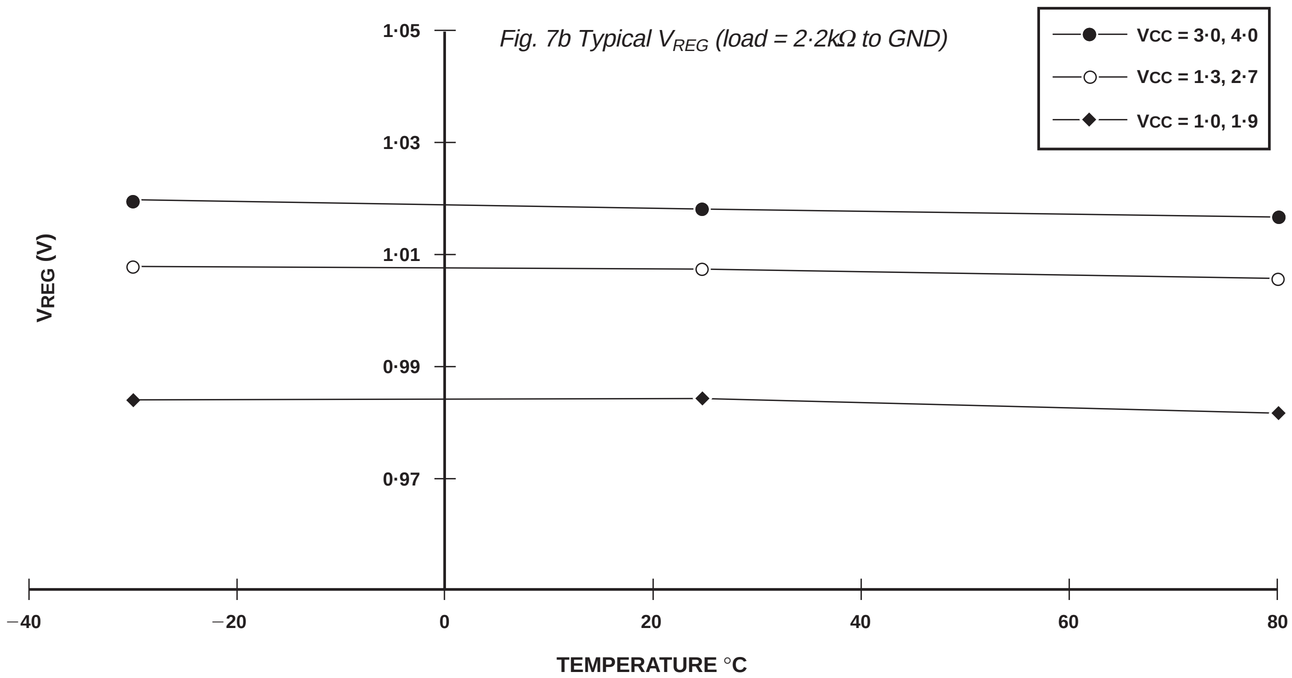




Conditions
Standard Mitel characterisation board (Fig. 5)
$I_{CC}1$ includes IRF LNA current (typ. 500µA) but does not include the regulator load current
The Audio AGC and RF AGC are both inactive
$I_{CC}2$ is measured with BATTFLAG and DATAS OP high, f_C = 282MHz
V_{BATT} connected to $V_{CC}1$

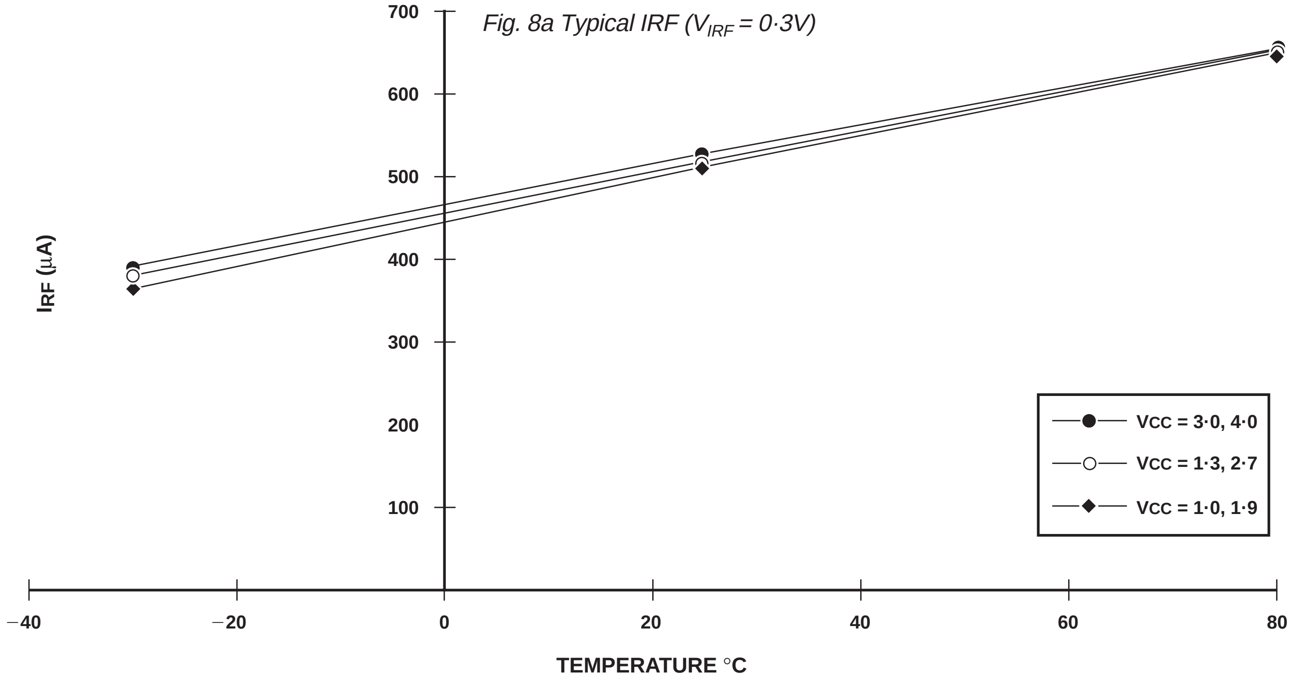
Fig. 6 Typical $I_{CC}1$ and $I_{CC}2$ v. supply and temperature

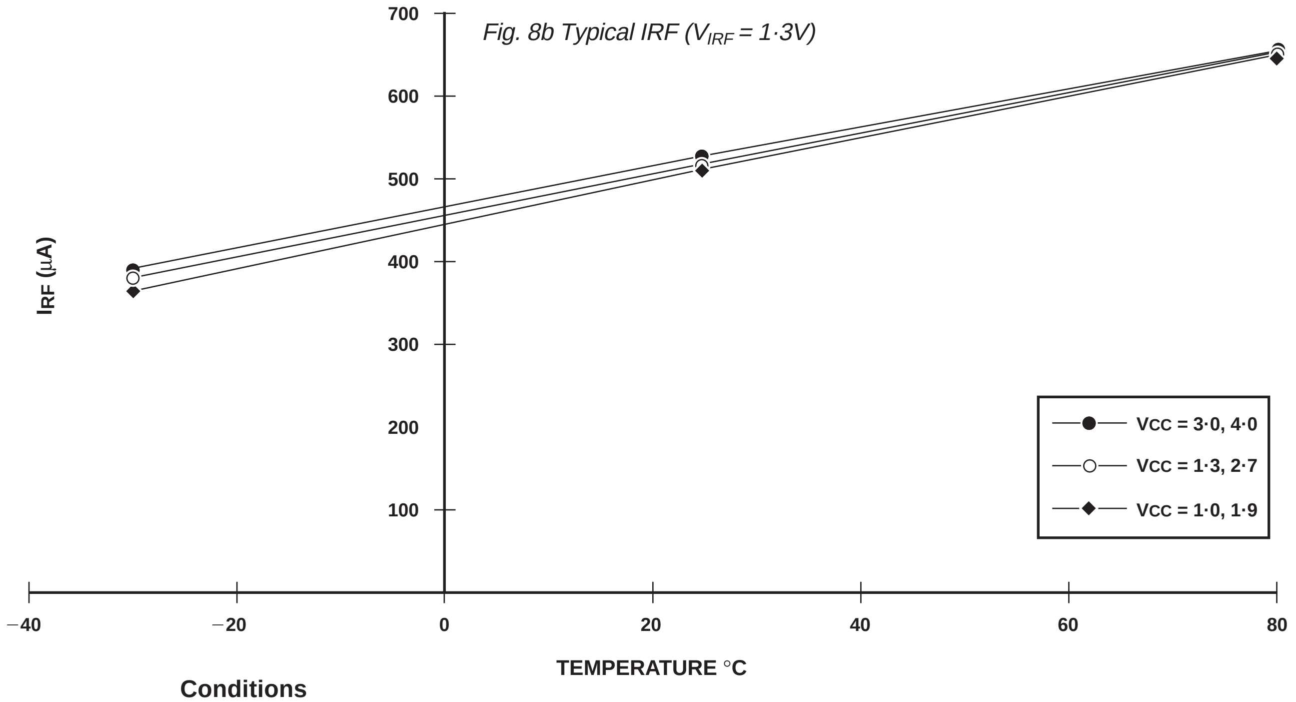




Conditions
Standard Mitel characterisation board (Fig. 5)
$I_{CC}1$ includes IRF LNA current (typ. 500µA) but does not include the regulator load current
The Audio AGC and RF AGC are both inactive
$I_{CC}2$ is measured with BATTFLAG and DATAS OP high, f_C = 282MHz
V_{BATT} connected to $V_{CC}1$

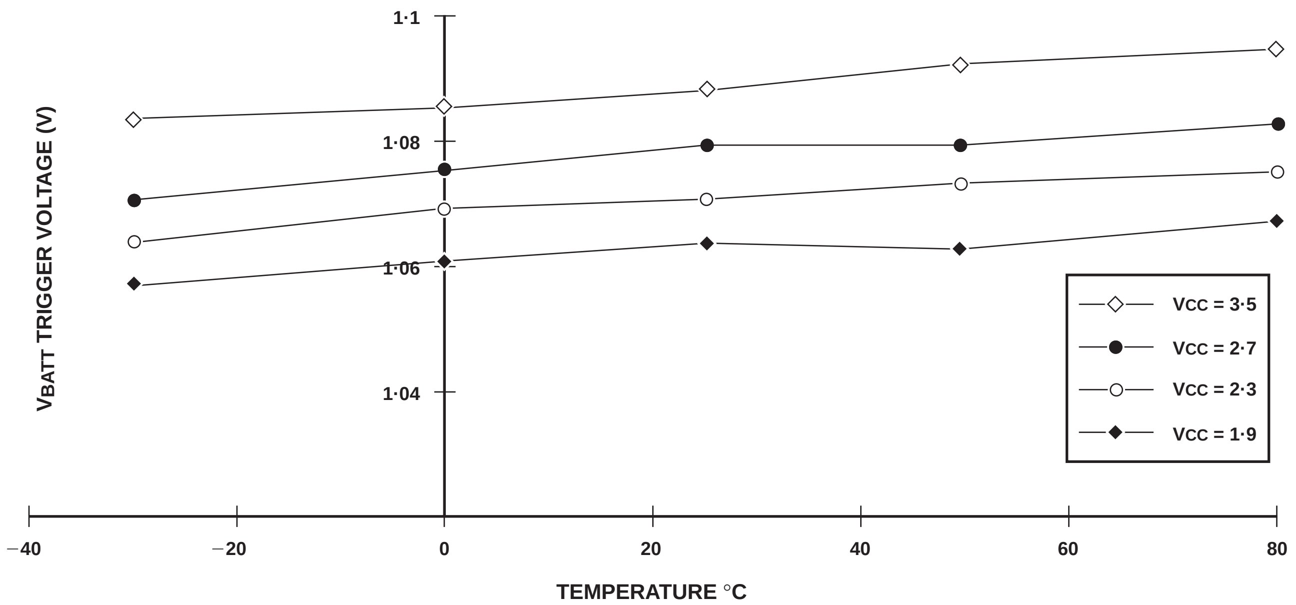
Fig. 7 Typical V_{REF} and V_{REG} v. supply and temperature





Conditions
Standard Mitel characterisation board (Fig. 5)
$I_{CC}1$ includes IRF LNA current (typ. 500µA) but does not include the regulator load current
The Audio AGC and RF AGC are both inactive
$I_{CC}2$ is measured with BATTFLAG and DATAS OP high, f_C = 282MHz
V_{BATT} connected to $V_{CC}1$

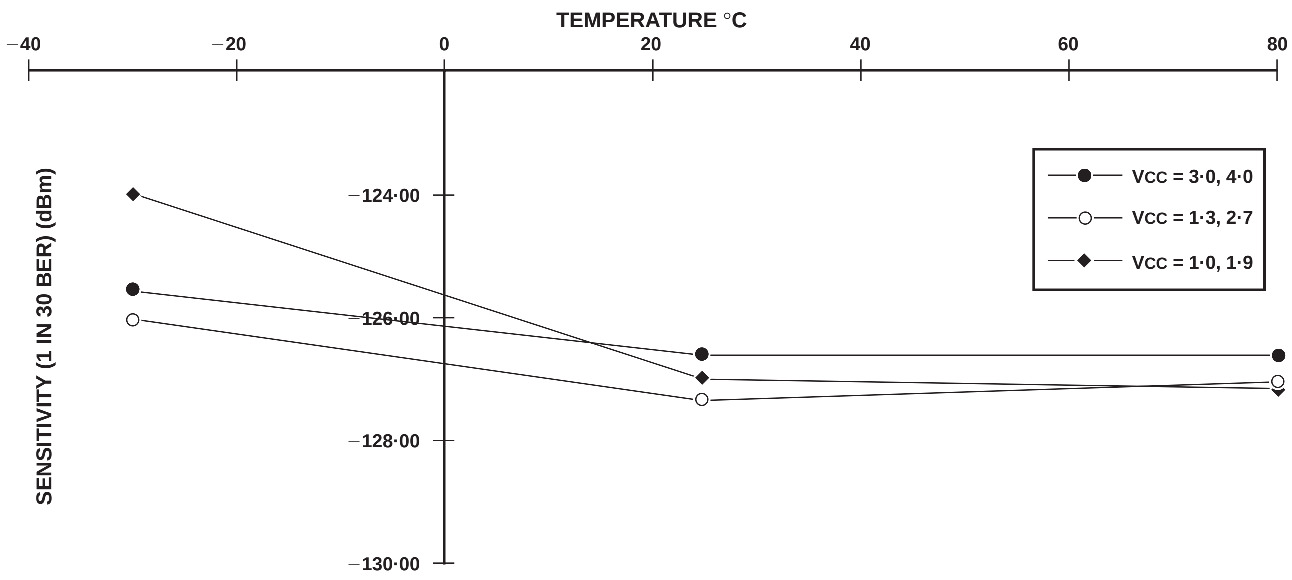
Fig. 8 Typical I_{RF} v. supply and temperature



Conditions
Standard Mitel characterisation board (Fig. 5)
$I_{CC}1$ includes IRF LNA current (typ. 500μA) but does not include the regulator load current
The Audio AGC and RF AGC are both inactive
$I_{CC}2$ is measured with BATTFLAG and DATAS OP high, f_C = 282MHz
V_{BATT} connected to $V_{CC}1$

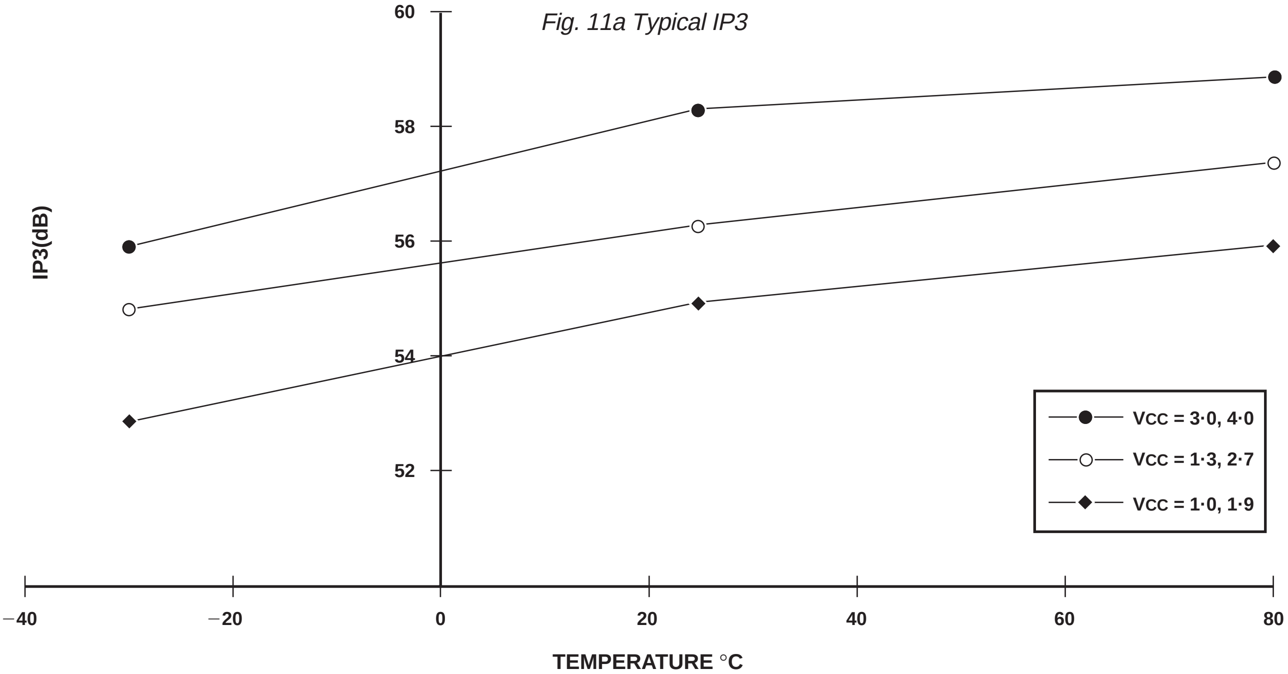
Fig. 9 Typical battery flag trigger voltage ($V_{BATTFLAG} = V_{CC}/2$) v. supply and temperature

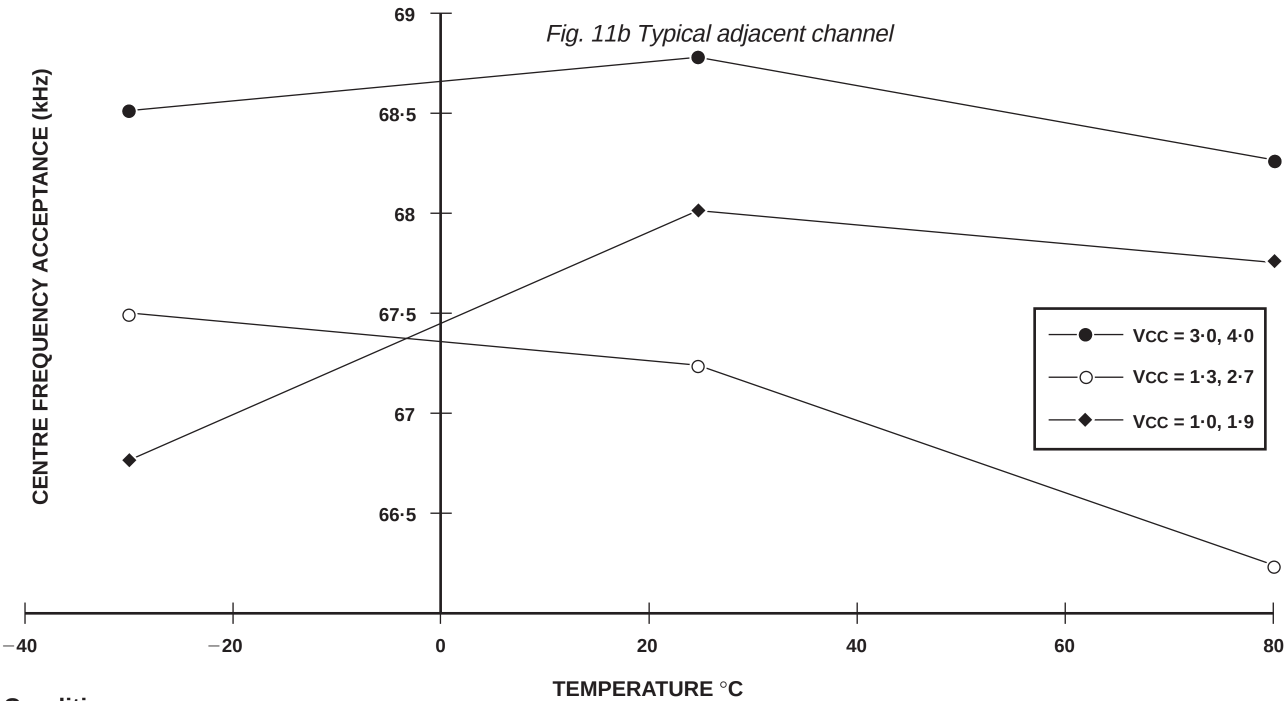
TYPICAL AC PARAMETERS (FIGS. 10 TO 13)



Conditions
282 Mitel characterisation board (Fig. 5), f_C = 282MHz
1200bps baud rate, 4kHz peak deviation frequency, BER 1 in 30
The LNA gain is set such that an RF signal of −73dBm at the LNA input, offset from the LO by 4kHz, gives a typical signal level of 300mVp-p at TPI and TPQ

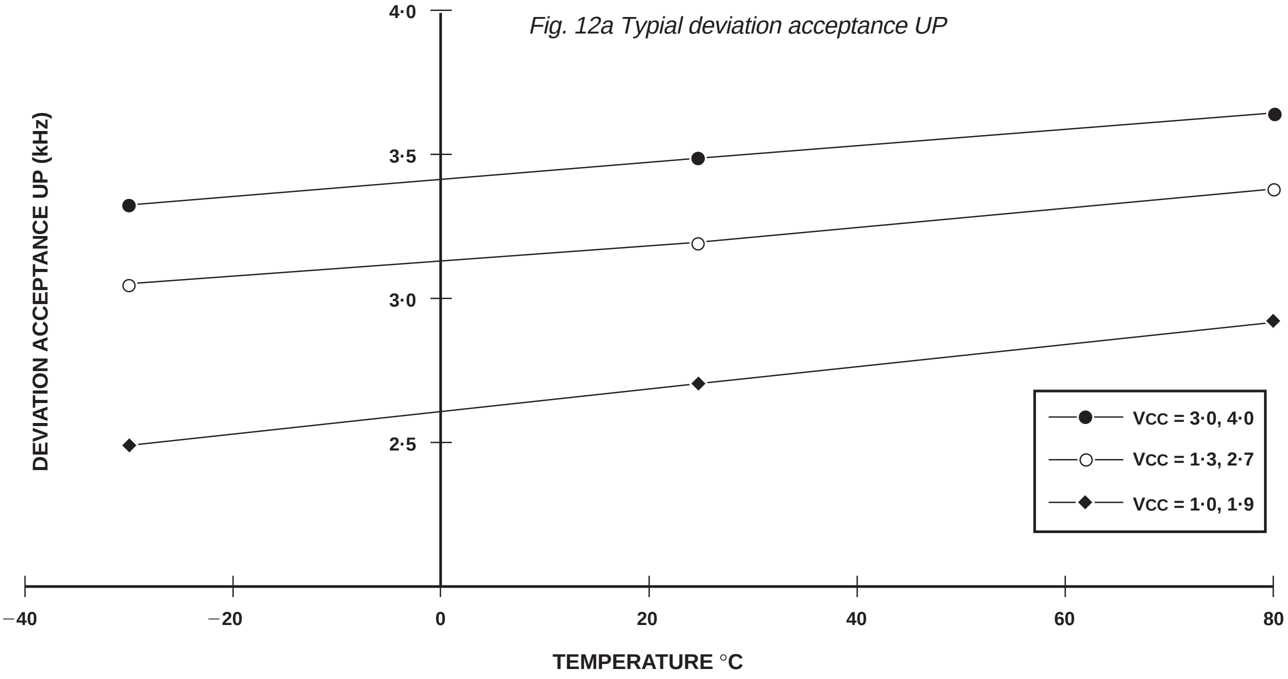
Fig. 10 Typical sensitivity v. supply and temperature

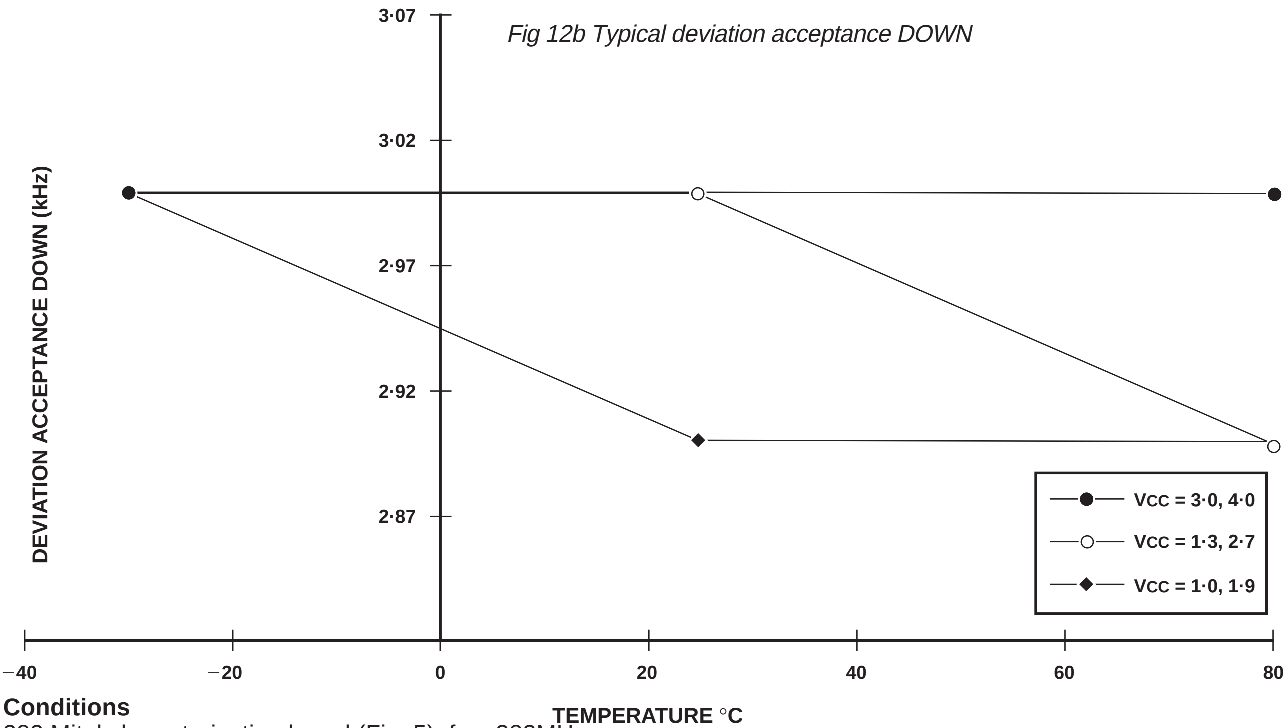




Conditions
282 Mitel characterisation board (Fig. 5), f_C = 282MHz
1200bps baud rate, 4kHz peak deviation frequency, BER 1 in 30
The LNA gain is set such that an RF signal of −73dBm at the LNA input, offset from the LO by 4kHz, gives a typical signal level of 300mVp-p at TPI and TPQ

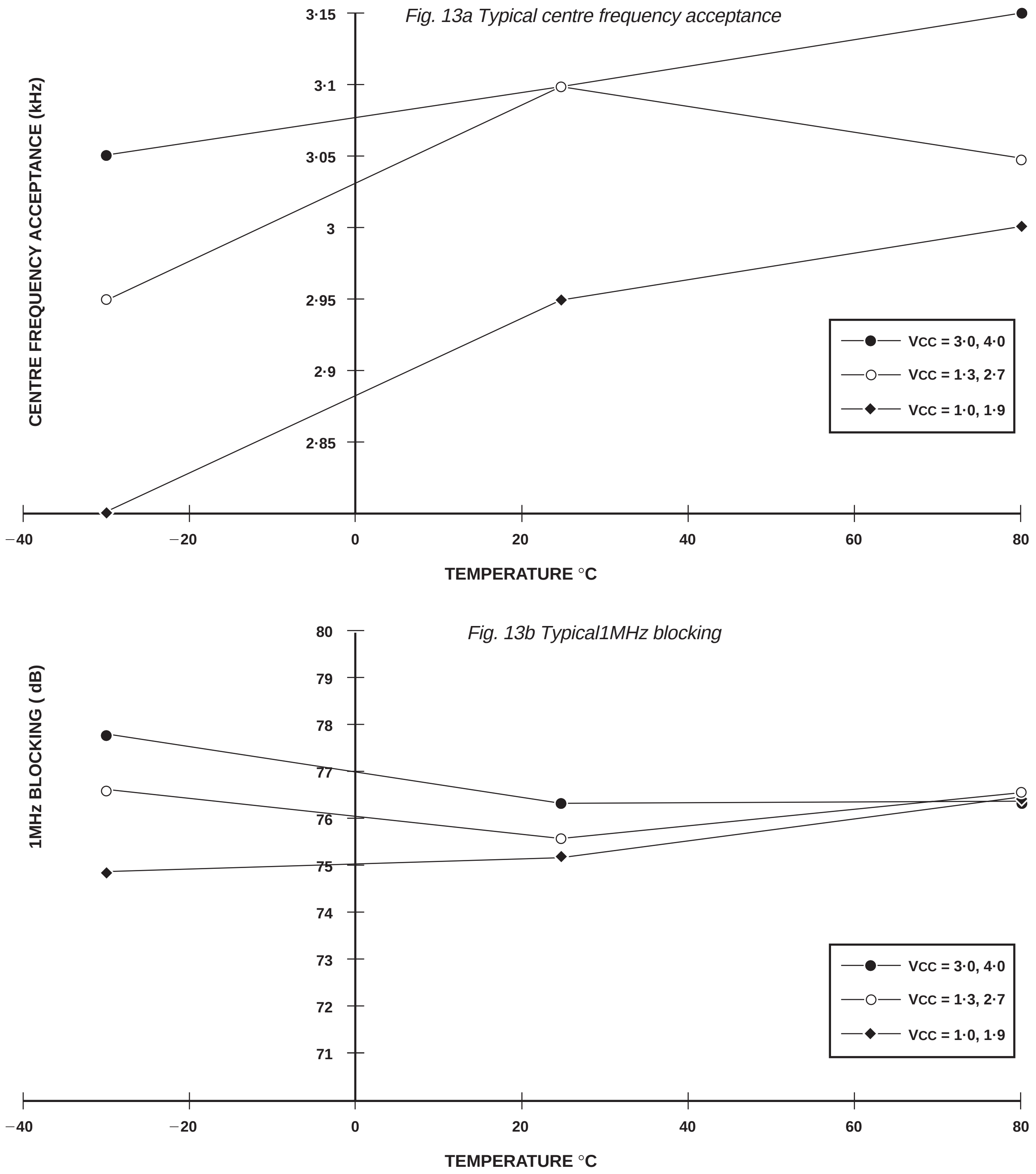
Fig. 11 Typical IP3 and adjacent channel v. supply and temperature





Conditions
282 Mitel characterisation board (Fig. 5), f_C = 282MHz
1200bps baud rate, 4kHz peak deviation frequency, BER 1 in 30
The LNA gain is set such that an RF signal of −73dBm at the LNA input, offset from the LO by 4kHz, gives a typical signal level of 300mVp-p at TPI and TPQ

Fig. 12 Typical deviation acceptance v. supply and temperature

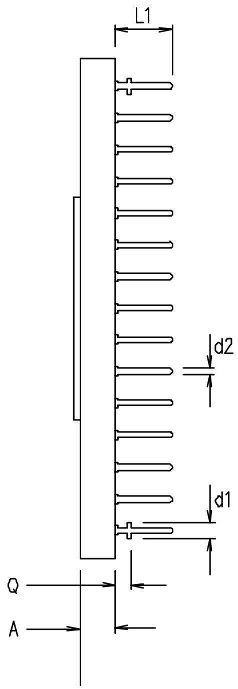


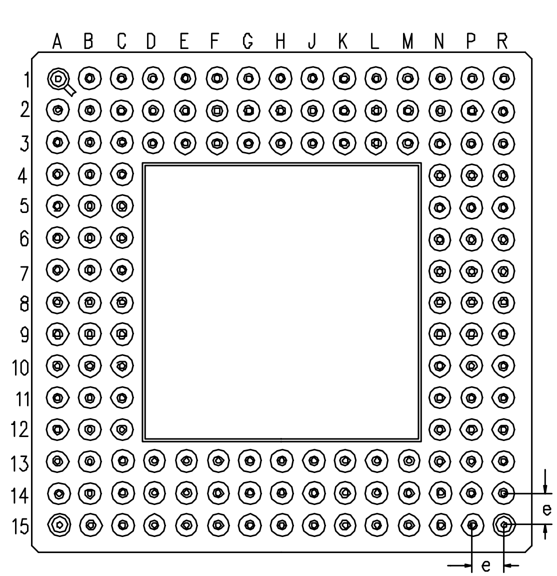
Conditions
282 Mitel characterisation board (Fig. 5), f_C = 282MHz
1200bps baud rate, 4kHz peak deviation frequency, BER 1 in 30
The LNA gain is set such that an RF signal of −73dBm at the LNA input, offset from the LO by 4kHz, gives a typical signal level of 300mVp-p at TPI and TPQ

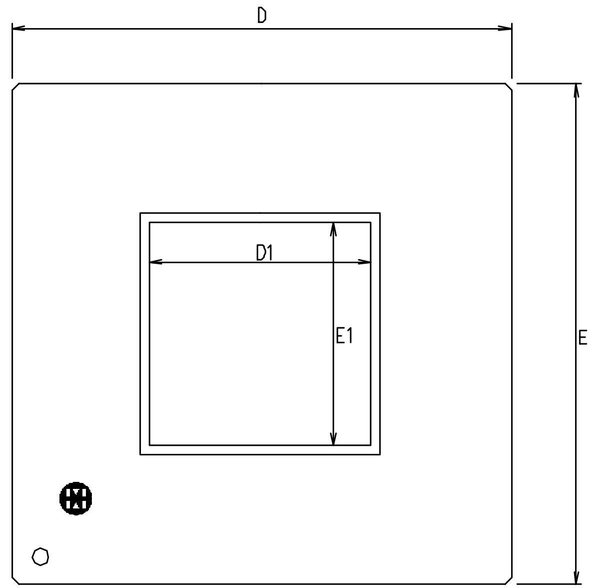
Fig. 13 Typical centre frequency acceptance and 1MHz blocking v. supply and temperature

WIRE BOND PAD / CONNECTOR PIN INTERCONNECTION PLAN

W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.	W/B NO.	PIN NO.
1	C3	27	L1	53	R7	79	M14	105	C14	131	B7
2	B2	28	L2	54	N8	80	L13	106	D13	132	A6
3	B1	29	M1	55	R8	81	M15	107	B15	133	B6
4	D3	30	L3	56	P8	82	L14	108	A15	134	C6
5	C2	31	M2	57	R9	83	K13	109	C13	135	A5
6	C1	32	N1	58	N9	84	L15	110	B14	136	B5
7	D2	33	N2	59	P9	85	K14	111	A14	137	A4
8	E3	34	M3	60	R10	86	J13	112	C12	138	C5
9	D1	35	P1	61	P10	87	K15	113	B13	139	B4
10	E2	36	R1	62	N10	88	J14	114	A13	140	A3
11	F3	37	N3	63	R11	89	J15	115	B12	141	B3
12	E1	38	P2	64	P11	90	H13	116	C11	142	C4
13	F2	39	R2	65	R12	91	H15	117	A12	143	A2
14	G3	40	N4	66	N11	92	H14	118	B11	144	A1
15	F1	41	P3	67	P12	93	G15	119	C10		
16	G2	42	R3	68	R13	94	G13	120	A11		
17	G1	43	P4	69	P13	95	G14	121	B10	S/R	NC
18	H3	44	N5	70	N12	96	F15	122	C9	D/A	NC
19	H1	45	R4	71	R14	97	F14	123	A10	H/S	NC
20	H2	46	P5	72	R15	98	F13	124	B9		
21	J1	47	N6	73	N13	99	E15	125	A9		
22	J3	48	R5	74	P14	100	E14	126	C8		
23	J2	49	P6	75	P15	101	D15	127	A8		
24	K1	50	N7	76	M13	102	E13	128	B8		
25	K2	51	R6	77	N14	103	D14	129	A7		
26	K3	52	P7	78	N15	104	C15	130	C7		







NOTES:-

1 INDEX MARK INDICATES A1 REF CORNER & CAN BE ANY SHAPE

2 PLATING BARS CAN APPEAR IN VARIOUS POSITIONS & SHOULD NOT BE USED FOR ORIENTATION PURPOSES

Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.52		3.08		0.099		0.121
Q	1.07		1.48		0.042		0.058
D	39.60		40.41		1.559		1.591
D1	17.65		17.91		0.695		0.705
E	39.60		40.41		1.559		1.591
E1	17.65		17.91		0.695		0.705
e	2.54 BSC.				0.100 BSC.		
d1	1.14		1.40		0.045		0.055
d2	0.41		0.51		0.016		0.020
L1	4.27		4.88		0.168		0.192
	Pin features						
N	144						
NOTE	SQUARE						

This drawing supersedes 418/ED/39506/106 issue 2

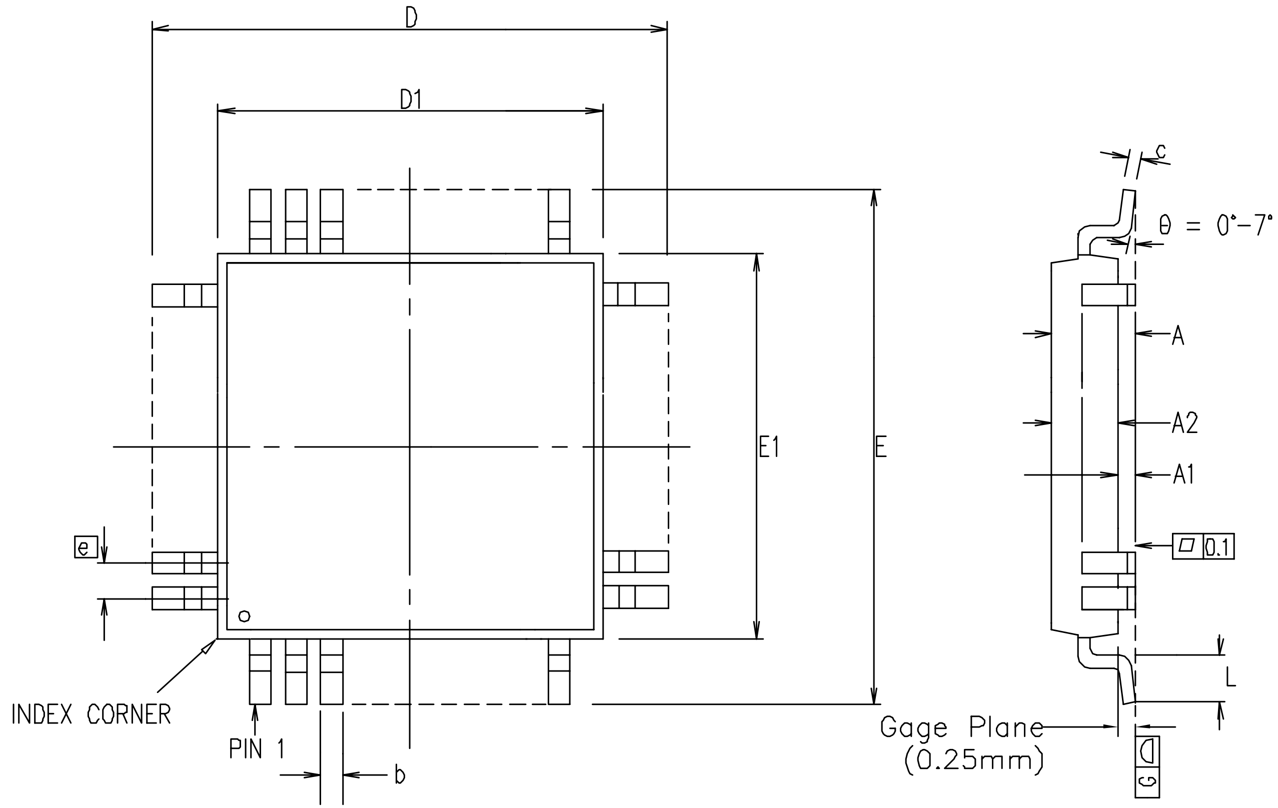
©Mitel						
ISSUE	1	2				
ACN	201923	203635				
DATE	16JAN97	2DEC97				
APPD.						

MITEL SEMICONDUCTOR

ORIGINATING SITE: SWINDON

Title: Outline Drawing for 144 PGA (POWER) (AC

Drawing Number GPD00289



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	9.00 BSC			0.354 BSC	
D1	7.00 BSC			0.276 BSC	
E	9.00 BSC			0.354 BSC	
E1	7.00 BSC			0.276 BSC	
L	0.45	0.75		0.018	0.030
e	0.80 BSC			0.031 BSC	
b	0.30	0.45		0.012	0.018
c	0.09	0.20		0.004	0.008
	Pin features				
N	32				
ND	8				
NE	8				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ABA Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51612/001 (S

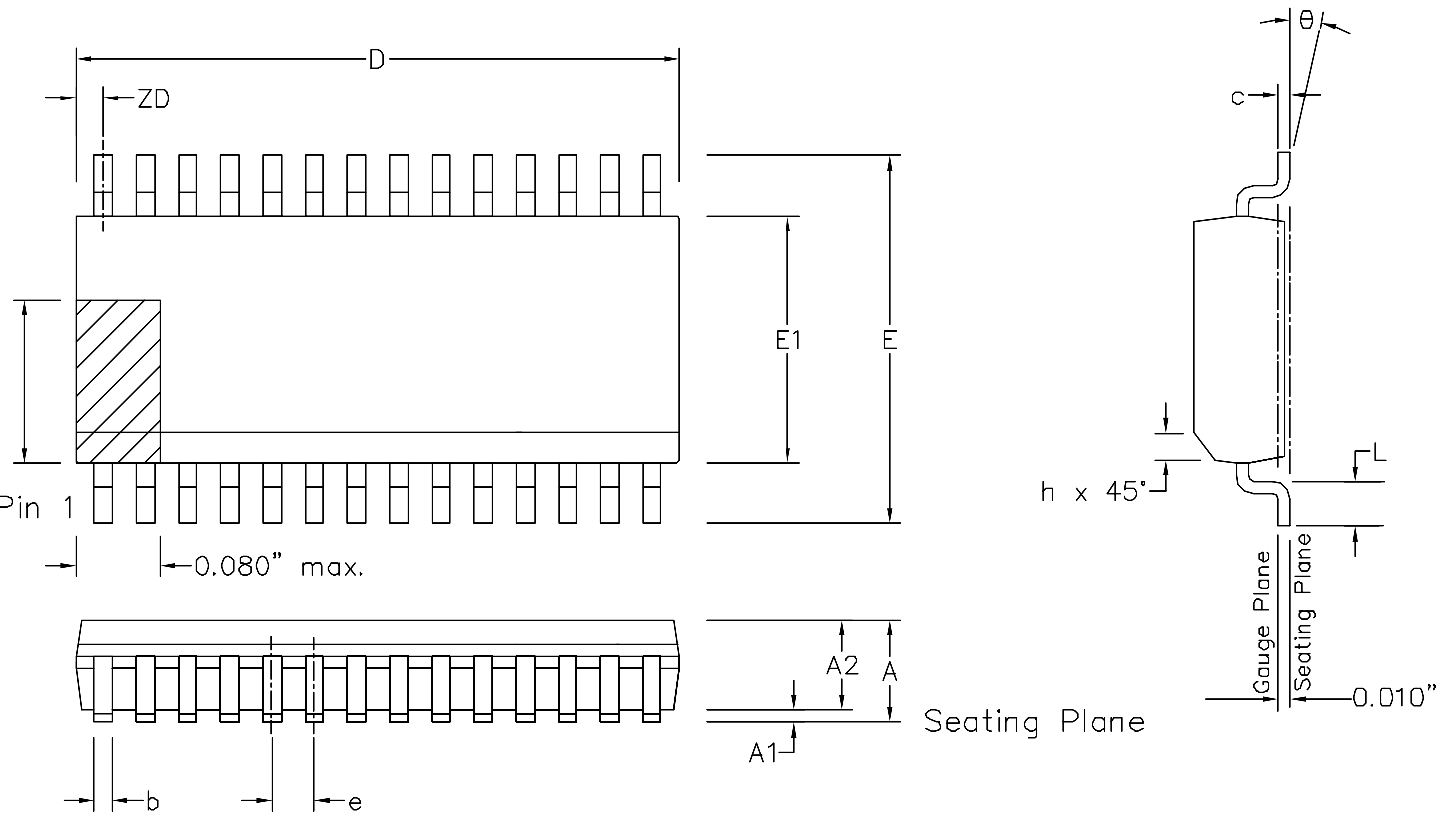
ISSUE	1	2			
ACN	201348	207076			
DATE	25OCT96	6JUL99			
APPROVED					

MITEL SEMICONDUCTOR

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 32 lds TQFP (TP) (7x7x1.0) mm, Body+2.0 mm

Drawing Number
GPD00233



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.386	0.394	9.80	10.01
ZD	0.033 REF.		0.84 REF.	
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025 BSC.		0.64 BSC.	
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
	Pin features			
N	28			
Conforms to JEDEC MO-137AF Iss. A				

This drawing supersedes
418/ED/51617/004 (Swindon/Roborough)
TD/D 1031 (Oldham)

otes:
The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
. Controlling dimensions are in inches.
. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

el					
	1	2			
	201930	207316			
	27FEB97	24AUG99			
D.					

MITEL SEMICONDUCTOR

ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 28L QSOP-0.150" Body Width(QP)

Drawing Number
GPD00292

http://www.mitelsemi.com

World Headquarters - Canada
Tel: +1 (613) 592 2122
Fax: +1 (613) 592 6909

North America
Tel: +1 (770) 486 0194
Fax: +1 (770) 631 8213

Asia/Pacific
Tel: +65 333 6193
Fax: +65 333 6192

Europe, Middle East, and Africa (EMEA)
Tel: +44 (0) 1793 518528
Fax: +44 (0) 1793 518581