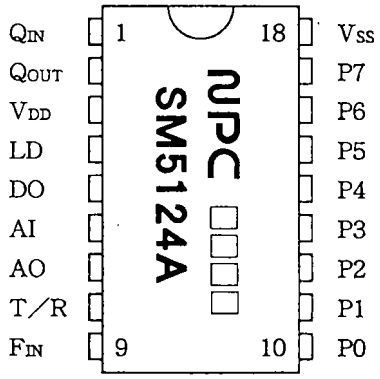
■ OVERVIEW

The SM5124A is a PLL LSI for 40-channel CB transceivers with US specifications using NPC's original molybdenum-gate CMOS technology. Incorporating a high-speed programmable counter for direct division of 27 MHz-band frequencies, the SM5124A eliminates the need for a transmission mixer and simplifies the external circuits.

■ FEATURES

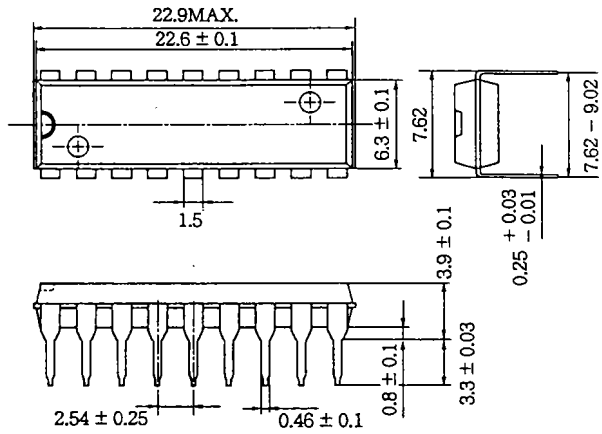
- 27 MHz direct dividing
- 1 crystal PLL synthesizer
- Built-in 40-channel transmission/reception code ROM
- Built-in mis-program detection circuit
- Digital lock detector
- Built-in inverter for active filter
- Built-in 10.24 MHz quartz crystal oscillator circuit
- Supply voltage 5.7 to 6.3 V
- 18-pin plastic DIP
- Molybdenum-gate CMOS construction

■ PINOUT (TOP VIEW)

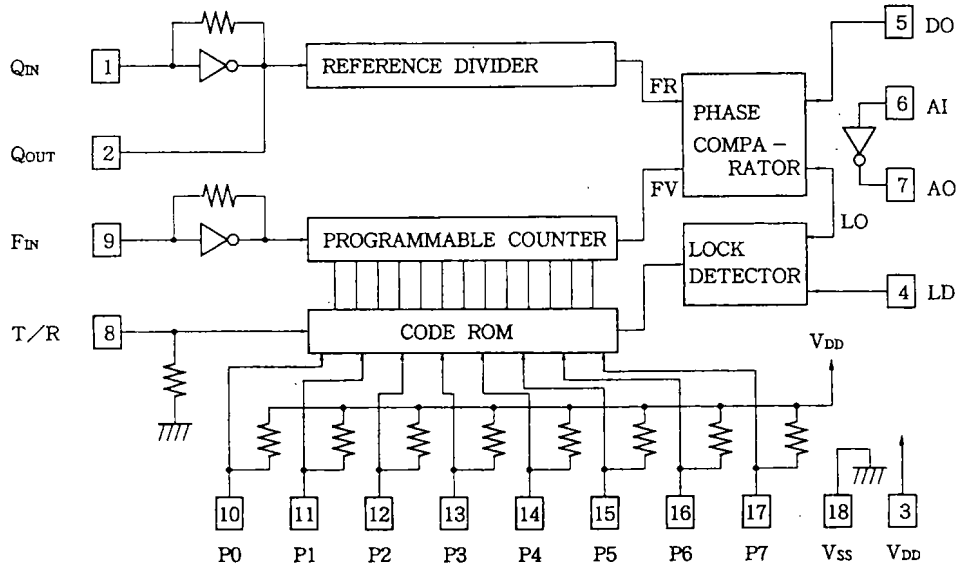


■ PACKAGE DIMENSIONS

(Unit: mm)



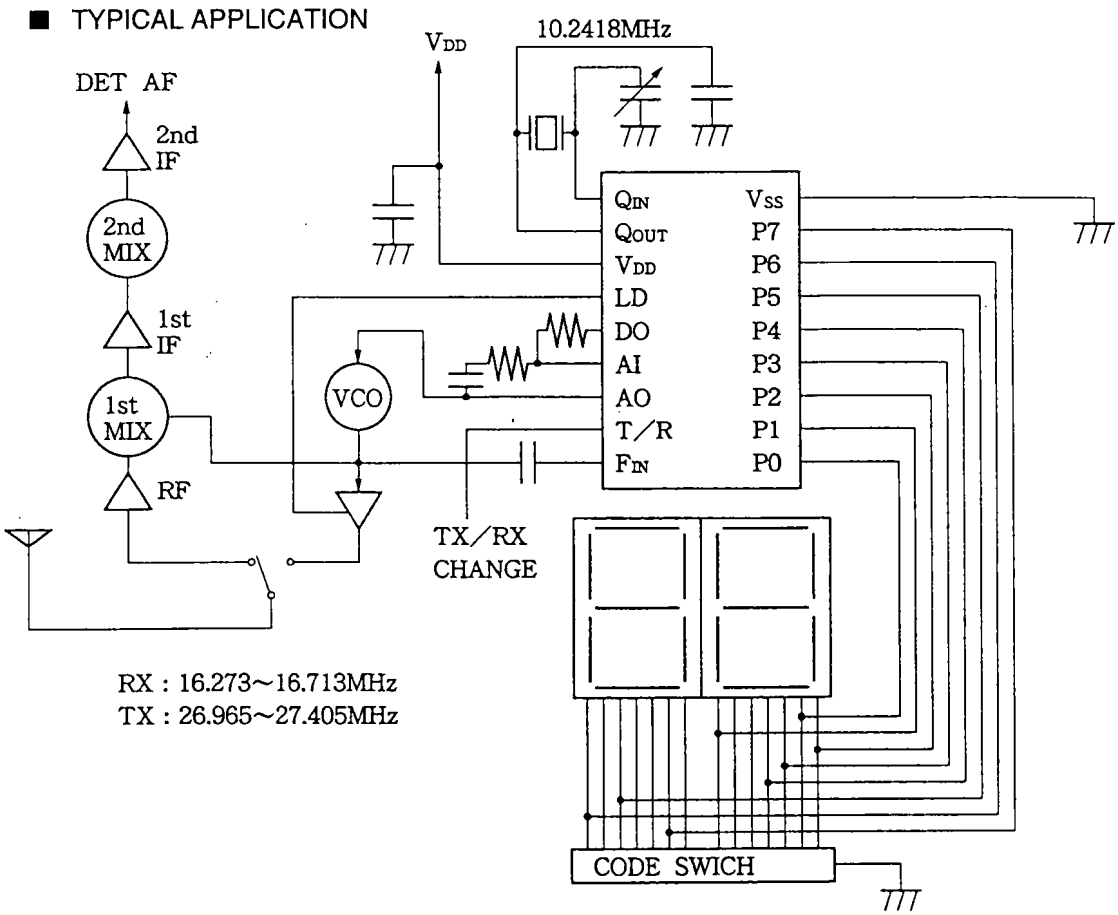
■ BLOCK DIAGRAM



■ PIN DESCRIPTION

NO.	NAME	DESCRIPTION
1	Q_{IN}	Internal quartz crystal oscillator circuit. Internal feedback resistor.
2	Q_{OUT}	
3	V_{DD}	Power supply 5.7 to 6.3 V
4	LD	UNLOCK signal output. Unlock: L, Lock : H
5	DO	Phase detector output. Charge pump circuit for active filter
6	AI	Amplifier input and output for active filter
7	AO	
8	T/R	Transmission/receiving switching input. Internal pull-down resistor. H: transmission, L or open: receiving
9	F_{IN}	Programmable counter input. Internal feedback resistor
10	P0	Channel switching inputs. Internal pull-up resistor
11	P1	Input code is 2-digit LED display code.
12	P2	When segment A of the unit digit is expressed 1A and segment C of the 10's digit is 2C, connections are
13	P3	made as shown below.
14	P4	P0 ·····1F P1 ·····1A P2 ·····1G
15	P5	P3 ·····1E P4 ·····1D P5 ·····2C
16	P6	P6 ·····2A P7 ·····2F
17	P7	
18	V_{SS}	Ground

■ TYPICAL APPLICATION



RX : 16.273~16.713MHz
TX : 26.965~27.405MHz

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

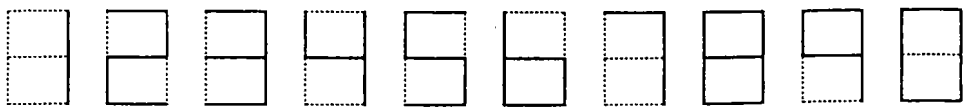
ITEM	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}-V_{SS}	-0.3 to +7.0	V
Input voltage	V_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	V
Power dissipation	V_W	250	mW
Operating temperature	T_{OPR}	-30 to +80	°C
Storage temperature	T_{STG}	-40 to +125	°C
Soldering temperature	T_{SLD}	260±5	°C
Soldering time	t_{SLD}	10	Sec

■ ELECTRICAL CHARACTERISTICS

Ta = -30 to +80 °C, VDD = 5.7 to 6.3 V, Vss = 0 V and QIN = 10.24188 MHz/ 1Vp-p/sine wave unless otherwise specified.

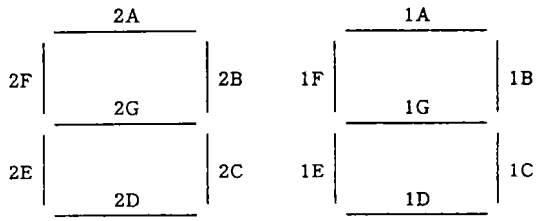
ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	REMARKS
			MIN	TYP	MAX		
Supply voltage	V_{DD}	F_{IN}=27.405MHz/1V_{p-p}/sine wave	5.7	6.0	6.3	V	
Current consumption	I_{DD}	F_{IN}=27.405MHz.1V_{p-p}/sine wave, AI=1/2V_{DD} Excluding pull-up/down resistor current			25	mA	
Maximum operating frequency	$f_{MAX}1$	F_{IN}=1V_{p-p}/sine wave	30			MHz	F_{IN} pin
	$f_{MAX}2$	Q_{IN}=1V_{p-p}/sine wave	12			MHz	Q_{IN} pin
Input voltage range	V_{AC}		1.0		V_{DD}-1.0	V_{p-p}	F_{IN}, Q_{IN} pin
Input voltage	V_{IH}		V_{DD}-1.0		V_{DD}	V	T/R,
	V_{IL}		0		1.0	V	P0 ~ P7 Pin
Input current	$I_{IH}1$	V_{DD}=6.3V, V_{IH}=6.3V			20	µA	F_{IN} pin
	$I_{IH}2$				20	µA	Q_{IN} pin
	$I_{IH}3$				200	µA	T/R pin
	$I_{IL}1$	V_{DD}=6.3V, V_{IL}=0V			20	µA	F_{IN} pin
	$I_{IL}2$				20	µA	Q_{IN} pin
	$I_{IL}3$				200	µA	P0 ~ P7 Pin
Open state voltage	$V_{IO}1$	V_{DD}=6.0V	2.4	3.0	3.6	V	F_{IN} pin
	$V_{IO}2$		2.4	3.0	3.6	V	Q_{IN} pin
	$V_{IO}3$				0.2	V	T/R pin
	$V_{IO}4$		5.8			V	P0 ~ P7 Pin
Output current	$I_{OH}1$	V_{DD}=5.7V, V_{OH}=5.3V, AI=V_{SS}	0.4			mA	LD, DO pin
	$I_{OH}2$		1.0			mA	AO pin
	$I_{OL}1$	V_{DD}=5.7V, V_{OL}=0.4V, AI=V_{DD}	0.4			mA	LD, DO pin
	$I_{OL}2$		1.0			mA	AO pin
Leak current	$I_{LH}1$	V_{DD}=6.3V, V_{LH}=6.3V, Ta=25°C			100	nA	DO pin
	$I_{LH}2$				100	nA	AI pin
	$I_{LL}1$	V_{DD}=6.3V, V_{LH}=0V, Ta=25°C			100	nA	DO pin
	$I_{LL}2$				100	nA	AI pin

■ DISPLAY FONT



■ CODE ROM

The code ROM stores coded data on 40 channels each for transmission and reception. P0 to P7 and T/R pins are used to switch channels. A two-digit LED display code is input to P0 to P7. Segment signals corresponding to P0 to P7 are shown below.



P0 ·····1F P4 ·····1D
P1 ·····1A P5 ·····2C
P2 ·····1G P6 ·····2A
P3 ·····1E P7 ·····2F

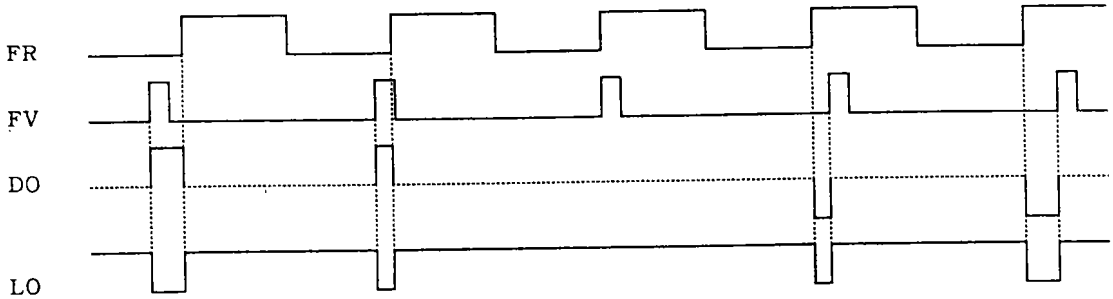
"L" or "OPEN" at the T/R pin indicates receiving, and "H" indicates transmission. The T/R pin is connected to an internal pull-down resistor. If data other than 1 to 40 channel codes is input to P0 to P7, the LD pin goes "L", and the phase detector stops operating at the same time.

■ PHASE DETECTOR AND LOCK DETECTOR

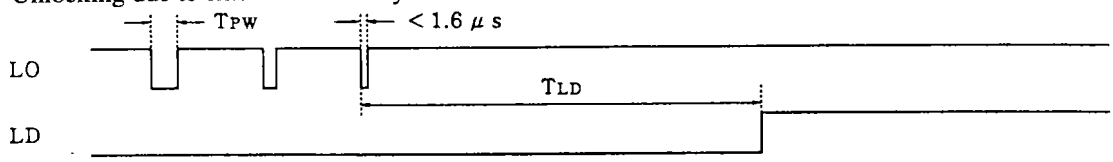
The phase detector compares the reference frequency divider output FR with the programmable counter input frequency divider output FV, then generates the VCO control voltage.

The phase detector also generates the LO signal with a time width equal to the phase difference between FV and FR, then inputs the signal to the lock detector. When the LO signal is 1.6 μs or longer, the lock detector judges that the PLL is unlocked and brings the LD pin "L". The LD pin goes "H" 4.8 ms ±10% after the LO signal becomes 1.6 μs or less.

- Phase detector

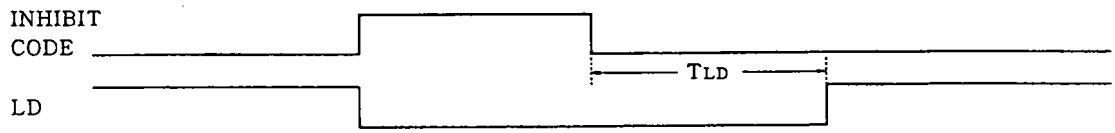


- Unlocking due to external instability



* Locking is detected when TPW<1.6 μs.
TLD=4.8ms ±10%

- Unspecified input code



※TLD = 4.8ms ± 10 %

■ PROGRAM CODE TABLE

FVCO = 0.010001839 × N (MHz)

Channel	2A	2B	2C	2D	2E	2F	2G	1A	1B	1C	1D	1F	1F	1G	T/R=L reception		T/R=H transmission	
	P6		P5			P7		P1			P4	P3	P0	P0	N	FVCO	N	FVCO
1	**H**	H	**H**	H	H	**H**	H	**H**	L	L	**H**	**H**	**H**	**H**	1627	16.273	2696	26.965
2	**H**	H	**H**	H	H	**H**	H	**L**	L	H	**L**	**L**	**H**	**L**	1628	.283	2697	.975
3	**H**	H	**H**	H	H	**H**	H	**L**	L	L	**L**	**H**	**H**	**L**	1629	.293	2698	.985
4	**H**	H	**H**	H	H	**H**	H	**H**	L	L	**H**	**H**	**L**	**L**	1631	.313	2700	27.005
5	**H**	H	**H**	H	H	**H**	H	**L**	H	L	**L**	**H**	**L**	**L**	1632	.323	2701	.015
6	**H**	H	**H**	H	H	**H**	H	**H**	H	L	**L**	**L**	**L**	**L**	1633	.333	2702	.025
7	**H**	H	**H**	H	H	**H**	H	**L**	L	L	**H**	**H**	**H**	**H**	1634	.343	2703	.035
8	**H**	H	**H**	H	H	**H**	H	**L**	L	L	**L**	**L**	**L**	**L**	1636	.363	2705	.055
9	**H**	H	**H**	H	H	**H**	H	**L**	L	L	**H**	**H**	**L**	**L**	1637	.373	2706	.065
10	**H**	L	**L**	H	H	**H**	H	**L**	L	L	**L**	**L**	**L**	**H**	1638	.383	2707	.075
11	**H**	L	**L**	H	H	**H**	H	**H**	L	L	**H**	**H**	**H**	**H**	1639	.393	2708	.085
12	**H**	L	**L**	H	H	**H**	H	**L**	L	H	**L**	**L**	**H**	**L**	1641	.413	2710	.105
13	**H**	L	**L**	H	H	**H**	H	**L**	L	L	**L**	**H**	**H**	**L**	1642	.423	2711	.115
14	**H**	L	**L**	H	H	**H**	H	**H**	L	L	**H**	**H**	**L**	**L**	1643	.433	2712	.125
15	**H**	L	**L**	H	H	**H**	H	**L**	H	L	**L**	**H**	**L**	**L**	1644	.443	2713	.135
16	**H**	L	**L**	H	H	**H**	H	**H**	H	L	**L**	**L**	**L**	**L**	1646	.463	2715	.155
17	**H**	L	**L**	H	H	**H**	H	**L**	L	L	**H**	**H**	**H**	**H**	1647	.473	2716	.165
18	**H**	L	**L**	H	H	**H**	H	**L**	L	L	**L**	**L**	**L**	**L**	1648	.483	2717	.175
19	**H**	L	**L**	H	H	**H**	H	**L**	L	L	**H**	**H**	**L**	**L**	1649	.493	2718	.185
20	**L**	L	**H**	L	L	**H**	L	**L**	L	L	**L**	**L**	**L**	**H**	1651	.513	2720	.205
21	**L**	L	**H**	L	L	**H**	L	**H**	L	L	**H**	**H**	**H**	**H**	1652	.523	2721	.215
22	**L**	L	**H**	L	L	**H**	L	**L**	L	H	**L**	**L**	**H**	**L**	1653	.533	2722	.225
23	**L**	L	**H**	L	L	**H**	L	**L**	L	L	**L**	**H**	**H**	**L**	1656	.563	2725	.255
24	**L**	L	**H**	L	L	**H**	L	**H**	L	L	**H**	**H**	**L**	**L**	1654	.543	2723	.235
25	**L**	L	**H**	L	L	**H**	L	**L**	H	L	**L**	**H**	**L**	**L**	1655	.553	2724	.245
26	**L**	L	**H**	L	L	**H**	L	**H**	H	L	**L**	**L**	**L**	**L**	1657	.573	2726	.265
27	**L**	L	**H**	L	L	**H**	L	**L**	L	L	**H**	**H**	**H**	**H**	1658	.583	2727	.275
28	**L**	L	**H**	L	L	**H**	L	**L**	L	L	**L**	**L**	**L**	**L**	1659	.593	2728	.285
29	**L**	L	**H**	L	L	**H**	L	**L**	L	L	**H**	**H**	**L**	**L**	1660	.603	2729	.295
30	**L**	L	**L**	L	H	**H**	L	**L**	L	L	**L**	**L**	**L**	**H**	1661	.613	2730	.305
31	**L**	L	**L**	L	H	**H**	L	**H**	L	L	**H**	**H**	**H**	**H**	1662	.623	2731	.315
32	**L**	L	**L**	L	H	**H**	L	**L**	L	H	**L**	**L**	**H**	**L**	1663	.633	2732	.325
33	**L**	L	**L**	L	H	**H**	L	**L**	L	L	**L**	**H**	**H**	**L**	1664	.643	2733	.335
34	**L**	L	**L**	L	H	**H**	L	**H**	L	L	**H**	**H**	**L**	**L**	1665	.653	2734	.345
35	**L**	L	**L**	L	H	**H**	L	**L**	H	L	**L**	**H**	**L**	**L**	1666	.663	2735	.355
36	**L**	L	**L**	L	H	**H**	L	**H**	H	L	**L**	**L**	**L**	**L**	1667	.673	2736	.365
37	**L**	L	**L**	L	H	**H**	L	**L**	L	L	**H**	**H**	**H**	**H**	1668	.683	2737	.375
38	**L**	L	**L**	L	H	**H**	L	**L**	L	L	**L**	**L**	**L**	**L**	1669	.693	2738	.385
39	**L**	L	**L**	L	H	**H**	L	**L**	L	L	**H**	**H**	**L**	**L**	1670	.703	2739	.395
40	**H**	L	**L**	H	H	**L**	L	**L**	L	L	**L**	**L**	**L**	**H**	1671	.713	2740	.405

* Channels (1 to 40) are selected based on the states of signals (P0 to P7) in bold letters.

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