

SM565

4-Bit Single-Chip Microcomputer (LCD Driver)

DESCRIPTION

The SM565 is a CMOS 4-bit single-chip microcomputer incorporating carrier output circuit for remote control, ROM, RAM, I/O ports, serial interface, and timer/counter. It provides 5 kinds of interrupts and subroutine stack function using the RAM area. Provided with a 256 segments LCD drive circuit, this microcomputer is applicable to a multi-functional AV remote control system, high performance hand-held LCD games or any other similar system with Low power consumption.

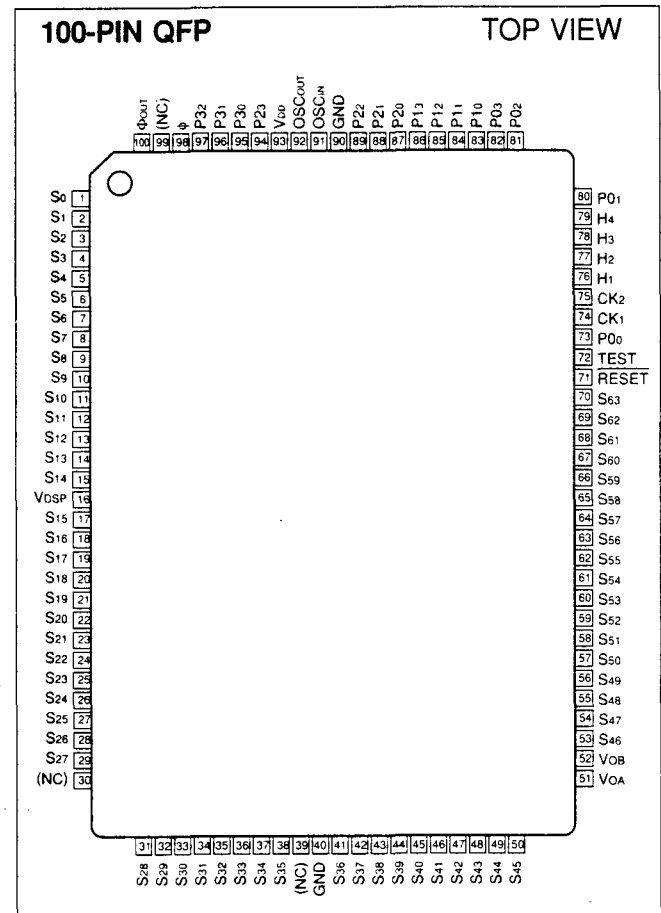
FEATURES

- ROM capacity : 8 192 x 8 bits
- RAM capacity : 256 x 4 bits (including 64 x 4 bits display RAM)
- Instruction sets : 98
- A RAM area is used as stack area
- I/O port :

Input	4
Input/output	11

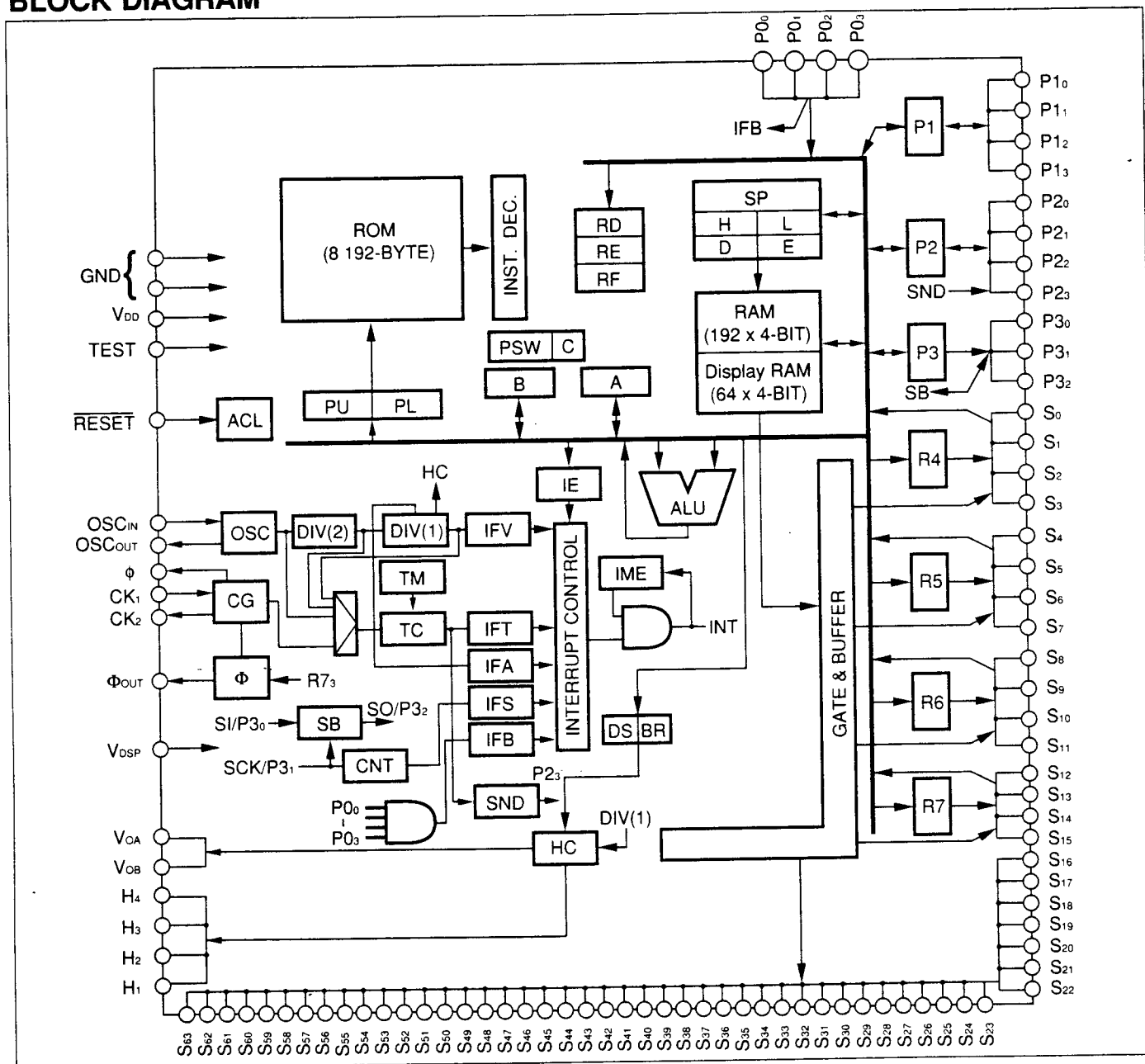
 +16 (Also used as LCD segment port)
- Interrupts :
 - Internal interrupt x 4 (timer/counter, f4 signal, serial I/O, divider overflow)
 - External interrupt x 1 (P0 signal)
- Timer/counter : 8 bits x 1
- Serial interface : 8 bits x 1
- Built-in main clock oscillator for system clock
- Built-in sub clock oscillator for real time clock
- Built-in 15 stages divider for real time clock
- Built-in LCD driver : 256 segments, 1/3 bias, 1/4 duty cycle (If LCD drive circuit is used, a crystal oscillator circuit needs to be constituted between OSC_{IN} and OSC_{OUT}.)

PIN CONNECTIONS



- Built-in carrier output circuit for remote control
 - Carrier frequency 37.9 kHz
 - Basic oscillation frequency (main clock) 455kHz
 - Duty cycle 1/3 or 1/2 (mask option)
 - Reversal polarity (mask option)
- Instruction cycle time : 8.79 μ s (TYP., 455 kHz, at 3 or 5 V)
- Buzzer output
- Standby function
- Supply voltage : 2.4 to 5.5 V
- Package : 100-pin QFP (QFP100-P-1420)

BLOCK DIAGRAM



Nomenclature

A, B	: Accumulators
ACL	: Auto clear
ALU	: Arithmetic logic unit
BR, DS	: Common signal control F/F
CG	: Clock generator
DIV	: Divider
D, E, H, L	: General-purpose registers
HC	: Common signal circuit
IE	: Interrupt enable F/F
IFA, IFB	: Interrupt requests
IFS, IFT, IFV	

IME	: Interrupt master enable F/F
P1-P3	: Registers
PL, PU	: Program counters
PSW	: Program status word register
R4-R7	: General-purpose registers
RD, RE, RF	: Mode registers
SB	: Shift register
SP	: Stack pointer
TC	: Count register
TM	: Modulo register
Φ	: Carrier control circuit

PIN DESCRIPTION

SYMBOL	I/O	CIRCUIT TYPE	FUNCTION
P0 ₀ -P0 ₃	I	Pull up	Acc ← P0 ₀ -P0 ₃
P1 ₀ -P1 ₃	I/O	Pull up	I/O selectable by instructions
P2 ₀ -P2 ₃	I/O	Pull up	I/O selectable independently Sound output only when P2 ₃ pin is used as an output
P3 ₀ -P3 ₃	I/O	Pull up	Serial interface I/O by setting the mode register RE
S ₀ -S ₁₅	O or I/O		Selectable between segment ports and I/O ports through an RC register
S ₁₆ -S ₆₃	O		Display RAM contents output as LCD segment signals
H ₁ -H ₄	O		4-value output capability; used for LCD common output
TEST	I	Pull down	For test (connected to GND normally)
RESET	I	Pull up	Auto clear
φ	O		System clock output
Φ _{OUT}	O		Carrier output pin for remote control
CK ₁ , CK ₂			For system clock oscillation
OSC _{IN} , OSC _{OUT}			For clock oscillation
V _{DSP} , V _{OA} , V _{OB}			Power supply for LCD driver
V _{DD} , GND			Power supply for logic circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{DD}	-0.3 to +7	V	1
	V _{DSP}	-0.3 to +7	V	
Input voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V	1
Output voltage	V _{OUT}	-0.3 to V _{DD} + 0.3	V	1
Output current	I _{OUT}	20	mA	2
Operating temperature	T _{OPR}	-20 to +70	°C	
Storage temperature	T _{STG}	-55 to +150	°C	

NOTES :

1. The maximum applicable voltage on any pin with respect to GND.
2. Sum of current from (or flowing into) output pins.

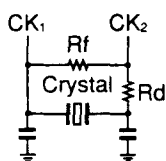
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{DD}		2.4		5.5	V	
	V _{DSP}		2.4		V _{DD}	V	
Basic oscillation frequency	f			455		kHz	
Instruction cycle	t			8.79		μs	
Crystal oscillation frequency	f _{osc}			32.768		kHz	1

NOTE :

1. Starting condition : within 10 seconds after power on.

Oscillation Circuit

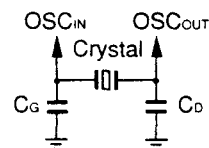


Oscillator circuit 1
 $C1 = 470 \text{ pF}$, $C2 = 470 \text{ pF}$
 $Rf = 1 \text{ M}\Omega$
 $Rd = 1 \text{ k}\Omega$

Oscillator : KBR-455B (Kyocera)

Oscillator circuit 2
 $C1 = 330 \text{ pF}$, $C2 = 330 \text{ pF}$
 $Rf = 1 \text{ M}\Omega$
 $Rd = 1.5 \text{ k}\Omega$

Oscillator : CSB455E (Murata)



$C_G = 33 \text{ pF}$, $C_D = 22 \text{ pF}$

DC CHARACTERISTICS

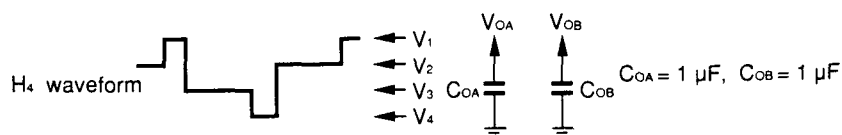
($V_{DD} = 2.4 \text{ to } 5.5 \text{ V}$, $T_a = -20 \text{ to } +70^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH1}		$0.7 \times V_{DD}$		V_{DD}	V	1
	V_{IL1}		0		$0.3 \times V_{DD}$	V	
	V_{IH2}		$V_{DD} - 0.5$		V_{DD}	V	2
	V_{IL2}		0		0.5	V	
Input current	I_{IH}	$V_{IN} = 0 \text{ V}$	2		200	μA	1
Output current	I_{OH1}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	50			μA	3
	I_{OL1}	$V_{OL} = 0.5 \text{ V}$	250			μA	
	I_{OH2}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	50			μA	4
	I_{OH2D}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	160			μA	5
	I_{OL2}	$V_{OL} = 0.5 \text{ V}$	500			μA	6
	I_{OH3}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	20			μA	7
	I_{OH3D}	$V_{OH} = V_{DD} - 0.5 \text{ V}$	90			μA	8
	I_{OL3}	$V_{OL} = 0.5 \text{ V}$	0.2			mA	7
Output impedance	R_C			5	20	$\text{k}\Omega$	9
	R_S			10	40	$\text{k}\Omega$	10
Output voltage	V_1	$V_{DSP} = 3.0 \text{ V}$ No load	2.7		3	V	11
	V_2		1.7	2	2.3	V	
	V_3		0.7	1	1.3	V	
	V_4		0		0.3	V	
Supply current	I_{OP}	$f = 455 \text{ kHz}$, $V_{DD} = 3.0 \text{ V}$		160	320	μA	12
	I_{SB}	Standby current $V_{DSP} = 3.0 \text{ V}$		15	40		13
		$V_{DD} = 3.0 \text{ V}$		8	20		14

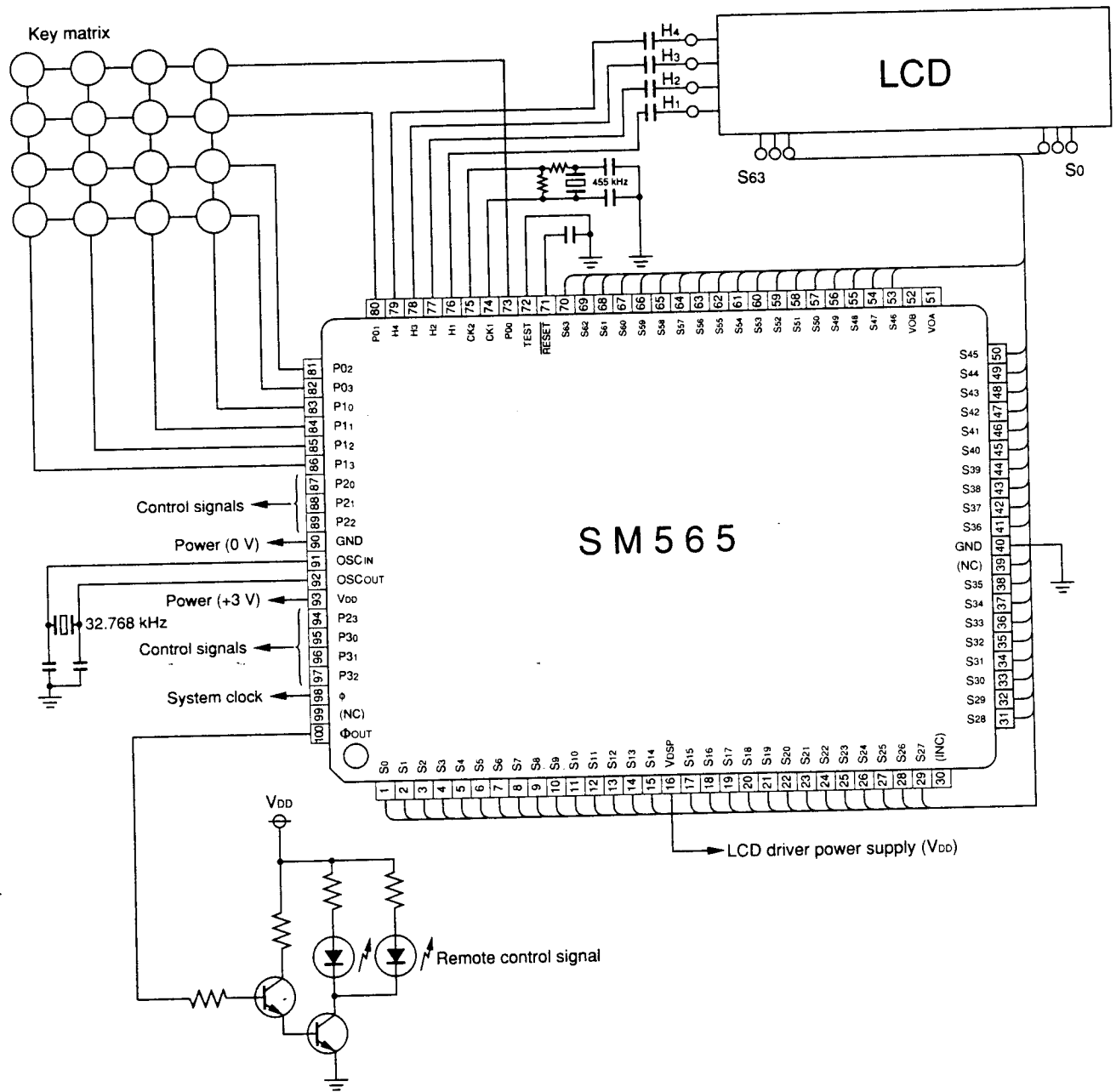
NOTES :

- Applied to pins $P0_0$ - $P0_3$, $\overline{\text{RESET}}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_2$ (during input mode).
- Applied to pins CK_1 , TEST, OSC_{IN} .
- Applied to pin CK_2 .
- Applied to pins $P1_0$ - $P1_3$, $P2_0$ - $P2_2$, $P3_0$ - $P3_2$ (during output mode).
- Applied to pins $P2_3$, Φ_{OUT} (during output mode).
- Applied to pins $P1_0$ - $P1_3$, $P2_0$ - $P2_2$, $P3_0$ - $P3_2$, Φ_{OUT} (during output mode).
- Applied to pins S_0 - S_{15} (during data output mode).

- Pins cited in NOTE 7 are applicable with mask option used.
- Applied to pins H_1 - H_4 .
- Applied to pins S_0 - S_{63} (during LCD output mode).
- Applied to pins H_1 - H_4 , S_0 - S_{63} (during LCD output mode).
- No load condition.
- No load condition when bleeder resistance is ON, $V_{DSP} = 3.0 \text{ V}$, during 32.768 kHz crystal oscillation.
- No load condition when bleeder resistance is OFF, during 32.768 kHz crystal oscillation.



SYSTEM CONFIGURATION EXAMPLE



Singlechip LH7xxxx '790 '789 '791 SMxxxx 'K series MCU Microcontroller MPU Microprocessor
ARM Advanced RISC Machines Databank LCD Controller LCD Driver Controllers Processors Portable
Low Power Low Voltage High Performance Power curve MIPS MIPS/Watt Execution Cycle Multiplier
High Speed Compact Handheld System on Chip System Integration Chip Integration Integration
Superchip Standard Cell Core Core based IC VHDL Verilog Synthesis Chip on Board COB Chip on Flex
COF Device on Board DOB Power Supply Controller Handy Products Development Tools Board Support
Software Tools Tools 2.10 Software Support Emulators Evaluation Boards ICE In-Circuit Emulators
ROM ICE SME Series Programmable User Configurable RTOS Real Time Operating Systems
Third Party Support Software Hardware Yokogawa Digital Cosmic Compiler C Language C Like
Assembler Linker Debugger Debug A/D D/A DAC Analog Digital 10-bit 4-bit 8-bit 16-bit 32-bit
Address bus Data Bus

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