

OVERVIEW

The SM6451AV is a 3-wire serial-controlled electronic variable volume IC for audio applications. It provides electronic volume control for a stereo system (left and right channels), and independent channel attenuation and muting, with greatly enhanced digital zip noise suppression. The chip address function allows up to four SM6451AV devices to be connected and individually controlled over the 3-wire control interface from a single CPU. It is available in 16-pin VSOP packages.

FEATURES

- Stereo inputs and outputs
- Attenuation function
 - 2-channel independent control
 - 1.0 dB/step over 80 steps
 - 0 to -80 dB range
- Mute function
- 3-wire serial data control (MDT, MCK, MLEN)
- Chip addressing (up to 4 devices can be connected in parallel)
- Low noise
 - $\leq 0.002\%$ THD + noise
 - $10 \mu\text{Vrms}$ residual noise
- 5 V single power supply
- Silicon-gate CMOS process

APPLICATIONS

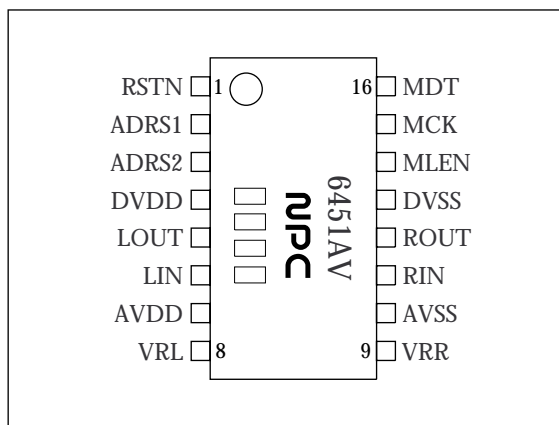
- Audio equipment

ORDERING INFORMATION

| Device | Package |
|----------|-------------|
| SM6451AV | 16-pin VSOP |

PINOUT

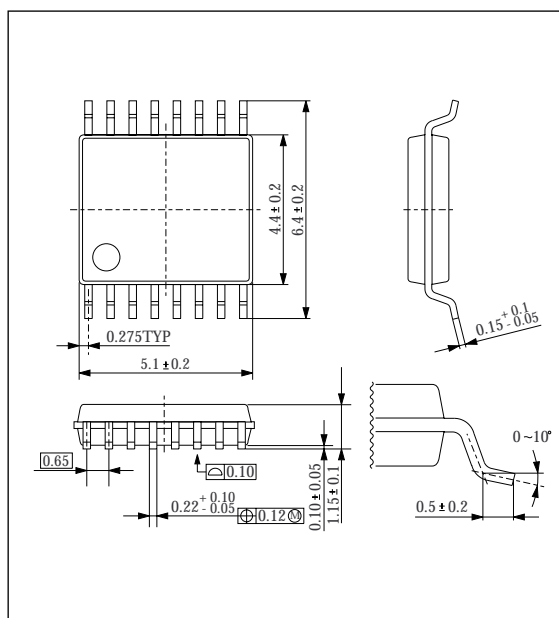
(Top View)



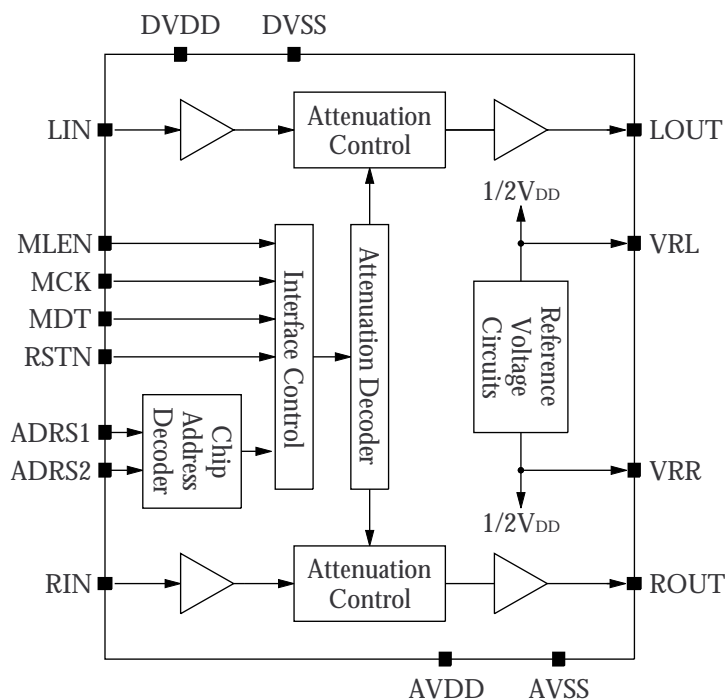
PACKAGE DIMENSIONS

(Unit: mm)

16 pin VSOP



BLOCK DIAGRAM



PIN DESCRIPTION

| Number | Name | I/O ¹ | A/D ¹ | Description |
|--------|-------|------------------|------------------|---|
| 1 | RSTN | Ip | D | System reset input (LOW-level reset) |
| 2 | ADRS1 | Ip | D | Chip address set 1 |
| 3 | ADRS2 | Ip | D | Chip address set 2 |
| 4 | DVDD | - | D | Digital supply |
| 5 | LOUT | O | A | Left-channel audio output |
| 6 | LIN | I | A | Left-channel audio input |
| 7 | AVDD | - | A | Analog supply |
| 8 | VRL | O | A | Left-channel reference voltage ($0.5V_{DD}$). Connect a 10 μ F capacitor between VRL and AVSS. |
| 9 | VRR | O | A | Right-channel reference voltage ($0.5V_{DD}$). Connect a 10 μ F capacitor between VRR and AVSS. |
| 10 | AVSS | - | A | Analog ground |
| 11 | RIN | I | A | Right-channel audio input |
| 12 | ROUT | O | A | Right-channel audio output |
| 13 | DVSS | - | D | Digital ground |
| 14 | MLEN | Ip | D | Microcontroller latch enable input |
| 15 | MCK | Ip | D | Microcontroller clock input |
| 16 | MDT | Ip | D | Microcontroller data input |

1. Ip = input pin with pull-up, A = analog, D = digital

SPECIFICATIONS

Absolute Maximum Ratings

DVSS = AVSS = 0 V, DVDD = AVDD = V_{DD}

| Parameter | Symbol | Rating | Unit |
|-----------------------|------------------|--|------|
| Supply voltage | V _{DD} | -0.3 to 7.0 | V |
| Input voltage | V _{IN} | V _{SS} - 0.3 to V _{DD} + 0.3 | V |
| Power dissipation | P _D | 150 | mW |
| Storage temperature | T _{stg} | -55 to 125 | °C |
| Soldering temperature | T _{sld} | 255 | °C |
| Soldering time | t _{sld} | 10 | s |

Recommended Operating Conditions

DVSS = AVSS = 0 V, DVDD = AVDD = V_{DD}

| Parameter | Symbol | Rating | Unit |
|--------------------------|---|------------|------|
| Supply voltage | V _{DD} | 4.5 to 5.5 | V |
| Supply voltage deviation | DV _{DD} - AV _{DD} , DV _{SS} - AV _{SS} | ±0.1 | V |
| Operating temperature | T _{opr} | -40 to 85 | °C |

DC Characteristics

DVDD = AVDD = V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

| Parameter | Symbol | Condition | Rating | | | Unit |
|---------------------------------------|-------------------|---|--------------------|-----|--------------------|------|
| | | | min | typ | max | |
| DVDD Current consumption | I _{DDD1} | Data transfer stopped, MDT, MCK, MLEN, RSTN, ADRS1, ADRS2 = V _{DD} | - | 0.3 | 1.0 | μA |
| | I _{DDD2} | ADRS1 = ADRS2 = 0V, 1.2 Vrms analog input, ATT = 0 dB, data transfer active | - | 1 | 2 | mA |
| AVDD Current consumption | I _{DDA} | | - | 4.5 | 8 | mA |
| HIGH-level input voltage ¹ | V _{IH} | | 0.7V _{DD} | - | - | V |
| LOW-level input voltage ¹ | V _{IL} | | - | - | 0.3V _{DD} | V |
| Input current ¹ | I _{IL} | V _{IN} = 0 V | - | 230 | 400 | μA |
| Input leakage current ¹ | I _{IH} | V _{IN} = V _{DD} | - | - | 1.0 | μA |

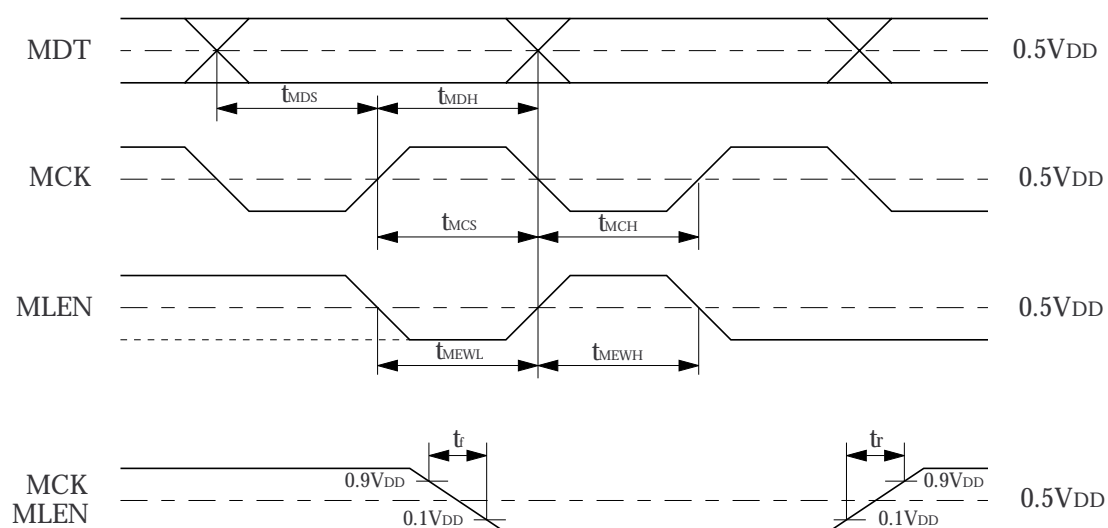
1. MDT, MCK, MLEN, RSTN, ADRS1, ADRS2

AC Digital Characteristics

DVDD = AVDD = V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, Ta = -40 to 85 °C

Serial inputs (MDT, MCK, MLEN)

| Parameter | Symbol | Rating | | | Unit |
|----------------------------|------------|--------|-----|-----|------|
| | | min | typ | max | |
| MCK, MLEN rise time | t_r | - | - | 100 | ns |
| MCK, MLEN fall time | t_f | - | - | 100 | ns |
| MDT setup time | t_{MDS} | 50 | - | - | ns |
| MDT hold time | t_{MDH} | 50 | - | - | ns |
| MLEN setup time | t_{MCS} | 50 | - | - | ns |
| MLEN hold time | t_{MCH} | 50 | - | - | ns |
| MLEN LOW-level pulsewidth | t_{MEWL} | 50 | - | - | ns |
| MLEN HIGH-level pulsewidth | t_{MEWH} | 50 | - | - | ns |



Reset input (RSTN)

| Parameter | Symbol | Rating | | | Unit |
|---------------------------|------------|--------|-----|-----|------|
| | | min | typ | max | |
| RSTN LOW-level pulsewidth | t_{RSTN} | 100 | - | - | ns |

AC Analog Characteristics

$V_{DD} = 5.0\text{ V}$, 1.2 Vrms amplitude, 1 kHz input frequency, 100 k Ω output load resistance, $T_a = 25\text{ }^\circ\text{C}$, AC-coupled inputs

Analog inputs (LIN, RIN)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---------------------------|-----------|--------------------------|--------|------|-----|------------|
| | | | min | typ | max | |
| Input reference amplitude | V_{AI} | | – | 1.2 | – | Vrms |
| Input resistance | R_{IN} | | 40 | 50 | 60 | k Ω |
| Input clipping voltage | V_{CLP} | THD + N = 1%, ATT = 0 dB | – | 1.75 | – | Vrms |

Analog outputs (LOUT, ROU)

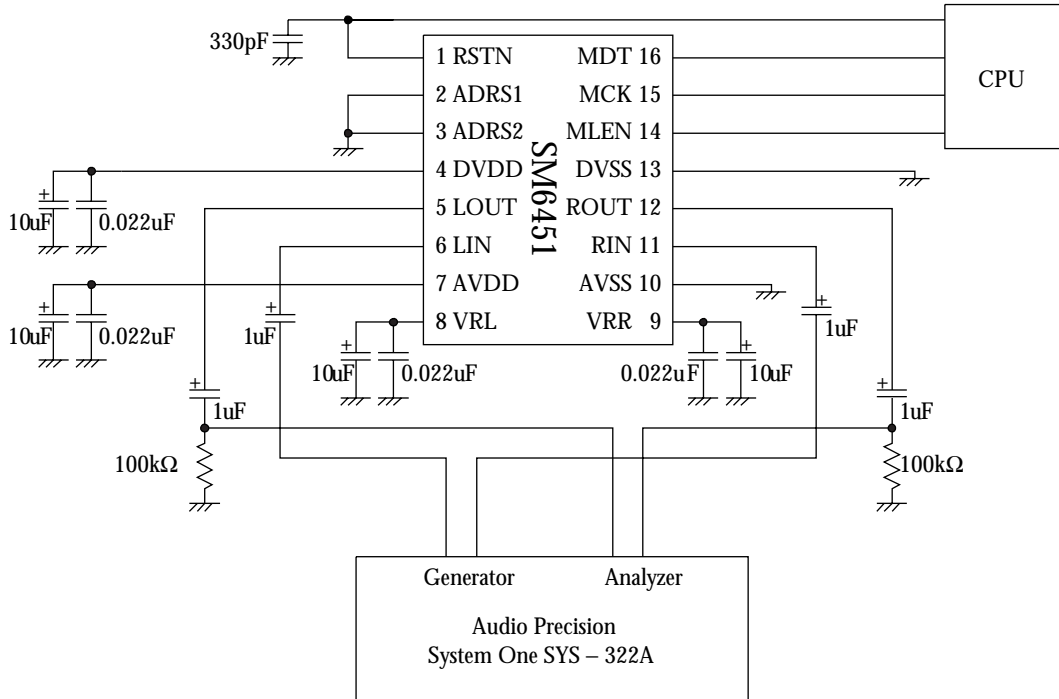
| Parameter | Symbol | Condition | Rating | | | Unit |
|---|------------------|---|--------|--------|--------|------------|
| | | | min | typ | max | |
| Residual noise voltage | V_{NS} | Input signal: 0 Vrms, A-weight filter, 0 dBr = 1.2 Vrms, ATT = 0 dB | – | 10 | 20 | μ Vrms |
| Signal-to-noise ratio | SNR | | 95 | 100 | – | dBr |
| Total harmonic distortion + noise | THD + N | ATT = 0 dB, 20 kHz lowpass filter | – | 0.0017 | 0.0025 | % |
| Gain control range | R_{CNT} | | –80 | – | 0 | dB |
| Step size | Step | | 0.8 | 1 | 1.5 | dB |
| Attenuation error (1k to 20kHz) | ERR ₁ | 0 to –60 dB | –2 | – | 1 | dB |
| | ERR ₂ | –61 to –80 dB | –5 | – | 0 | dB |
| Absolute attenuation (1 kHz) | AT ₀ | ATT = 0 dB | – | –0.1 | – | dB |
| | AT ₂ | ATT = –20 dB | – | –20.1 | – | dB |
| | AT ₄ | ATT = –40 dB | – | –40.3 | – | dB |
| | AT ₆ | ATT = –60 dB | – | –60.5 | – | dB |
| | AT ₈ | ATT = –80 dB | – | –83.0 | – | dB |
| Mute attenuation (1 kHz) | Mute | ATT = Mute | –88 | –92 | – | dB |
| Channel crosstalk | CT | ATT = 0 dB | –105 | –112 | – | dB |
| Frequency response | FR | ATT = 0 dB, $f = 200\text{ kHz}$ | – | –5 | – | dB |
| Quiescent output zip noise voltage (while ATT value adjusting) | N_J | 0 Vrms input | – | – | 3 | mV |
| Minimum driver load resistance | R_{ML} | ATT = 0 dB, THD + N = 1% | – | 6 | 10 | k Ω |

Reference voltage (VRL, VRR)

| Parameter | Symbol | Condition | Rating | | | Unit |
|--------------------------|-----------|-----------|--------------|-------------|--------------|------|
| | | | min | typ | max | |
| Reference voltage output | V_{REF} | | $0.45V_{DD}$ | $0.5V_{DD}$ | $0.55V_{DD}$ | V |

MEASUREMENT CIRCUIT

Chip address: ADRS1 = LOW, ADRS2 = LOW



MICROCONTROLLER INTERFACE

The SM6451AV uses a 3-wire serial interface comprising MDT (data), MCK (clock) and MLEN (latch enable) to select channels and attenuation levels for the addressed device.

Input Timing

The microcontroller data input timing is shown in figure 1.

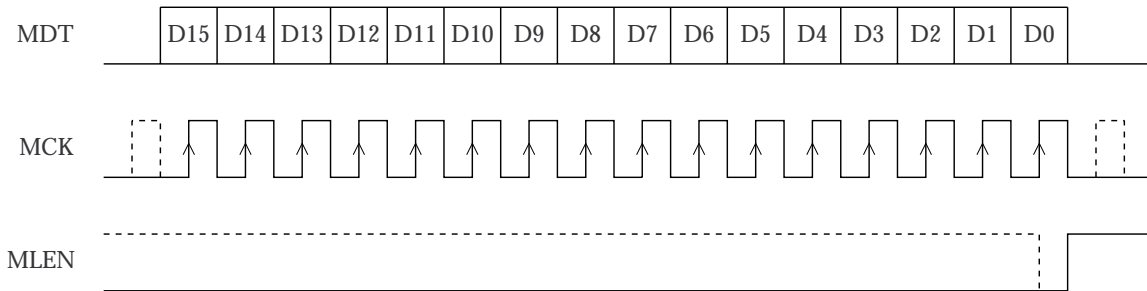


Figure 1. Microcontroller data input timing

Data is shifted into the internal shift register on the rising edge of MCK, and the attenuation value is updated on the rising edge of MLEN. Accordingly, data on MDT should be changed on the falling edge of MCK. The dotted lines for MCK and MLEN also indicate valid timing.

Note, however, a minimum of 16 MCK input pulses are required.

Data Format

The format of microcontroller input data is shown in figure 2.

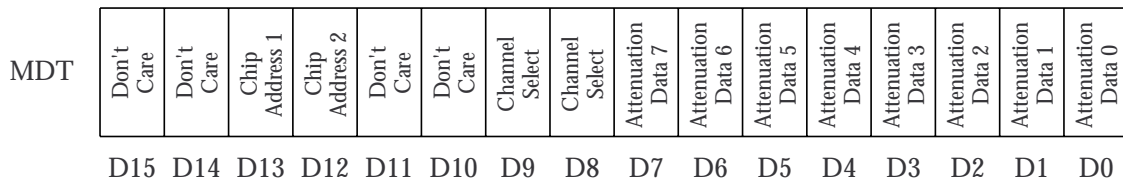


Figure 2. Microcontroller data format

D15, D14

Don't care.

D13, D12

Chip address bits. D13 corresponds to ADRS1 and D12 corresponds to ADRS2. The device is addressed only when ADRS1:ADRS2 matches D13:D12.

Example 1: If D13 = LOW, D12 = HIGH and ADRS1 = LOW, ADRS2 = LOW, then the device is not addressed since ADRS2 and D12 do not match.

Example 2: If D13/D12 = LOW and ADRS1/ADRS2 = LOW, then the device is addressed and all input data is read and the attenuation settings updated.

D11, D10

Don't care.

D9, D8

Channel select bits. The selected channel(s) are shown in table 1.

Table 1. Channel select

| D9 | D8 | Selected channel |
|------|------|------------------------------|
| LOW | LOW | Both left and right channels |
| LOW | HIGH | Left channel |
| HIGH | LOW | Right channel |
| HIGH | HIGH | No change |

D7 to D0

Attenuation register (ATT) set bits.

Table 2. Attenuation setting¹

| Attenuation | ATT _H | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------|------|------|------|------|------|------|------|------|
| 0 dB | 00 | LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW |
| -1 dB | 01 | LOW | LOW | LOW | LOW | LOW | LOW | LOW | HIGH |
| -2 dB | 02 | LOW | LOW | LOW | LOW | LOW | LOW | HIGH | LOW |
| : | : | : | : | : | : | : | : | : | : |
| -15 dB | 0F | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH | HIGH |
| -16 dB | 10 | LOW | LOW | LOW | HIGH | LOW | LOW | LOW | LOW |
| -17 dB | 11 | LOW | LOW | LOW | HIGH | LOW | LOW | LOW | HIGH |
| : | : | : | : | : | : | : | : | : | : |
| -63 dB | 3F | LOW | LOW | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| -64 dB | 40 | LOW | HIGH | LOW | LOW | LOW | LOW | LOW | LOW |
| -65 dB | 41 | LOW | HIGH | LOW | LOW | LOW | LOW | LOW | HIGH |
| : | : | : | : | : | : | : | : | : | : |
| -79 dB | 4F | LOW | HIGH | LOW | LOW | HIGH | HIGH | HIGH | HIGH |
| -80 dB | 50 | LOW | HIGH | LOW | HIGH | LOW | LOW | LOW | LOW |
| Mute | 51 | LOW | HIGH | LOW | HIGH | LOW | LOW | LOW | HIGH |
| Mute | 52 | LOW | HIGH | LOW | HIGH | LOW | LOW | HIGH | LOW |
| : | : | : | : | : | : | : | : | : | : |
| Mute | FE | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | LOW |
| Mute | FF | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |

1. Outputs are muted after system reset.

ANALOG PERFORMANCE CHARACTERISTICS

DVDD = AVDD = 5.0 V, 100 kΩ output load resistance, Ta = 25 °C

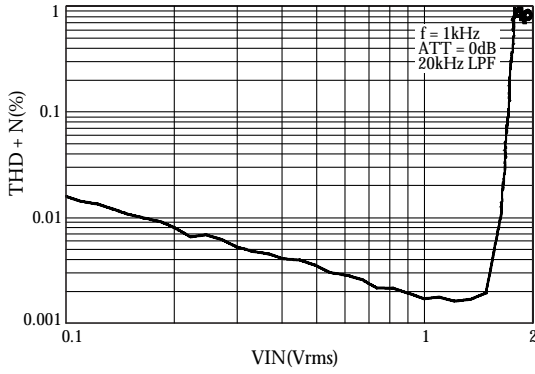


Figure 3. THD + N vs. input amplitude

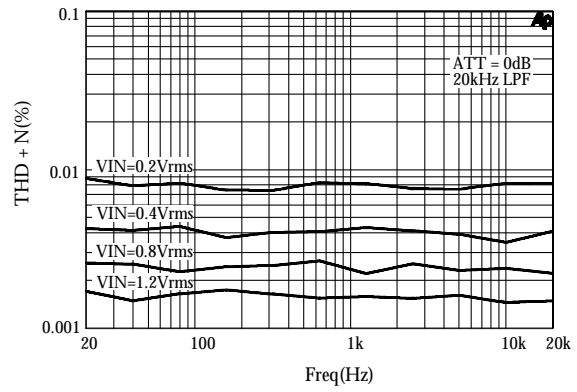


Figure 4. THD + N vs. input frequency

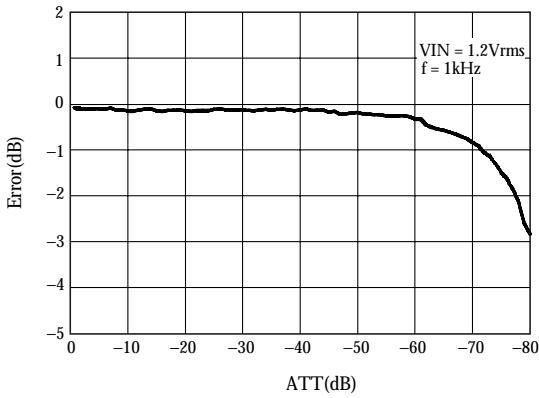


Figure 5. Attenuation error

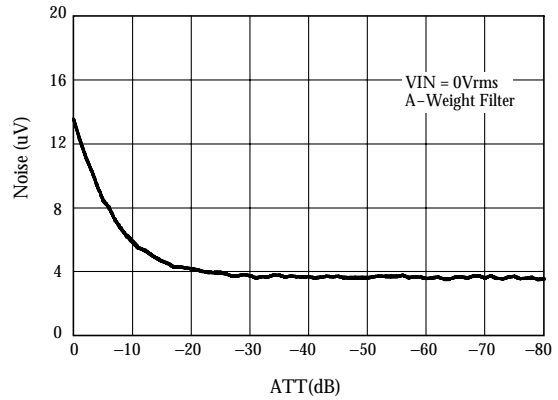


Figure 6. Residual noise vs. ATT

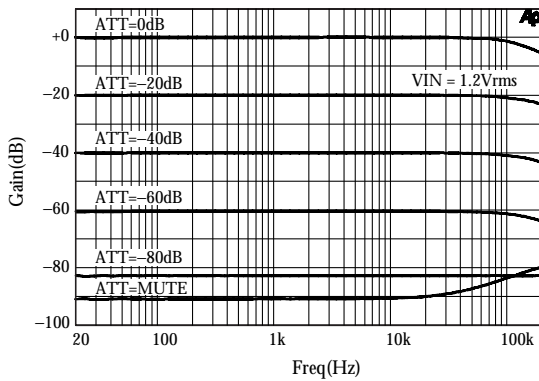


Figure 7. Frequency response

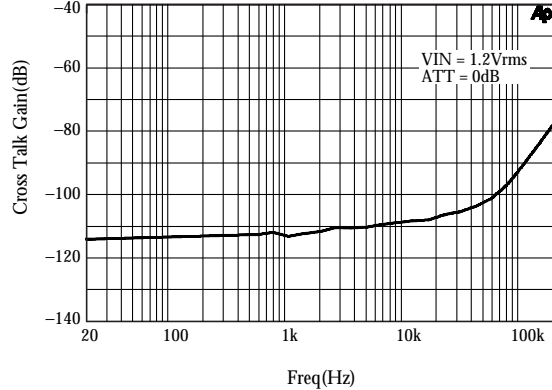


Figure 8. Crosstalk frequency response

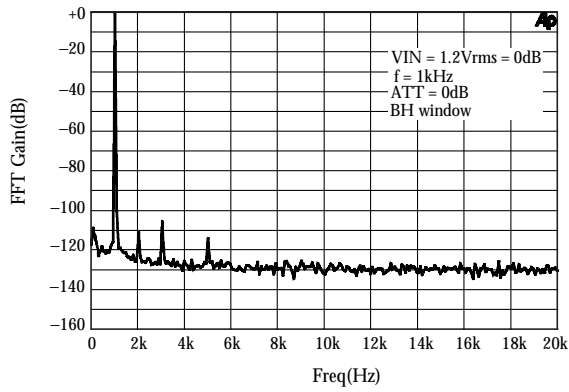


Figure 9. FFT plot (ATT = 0 dB)

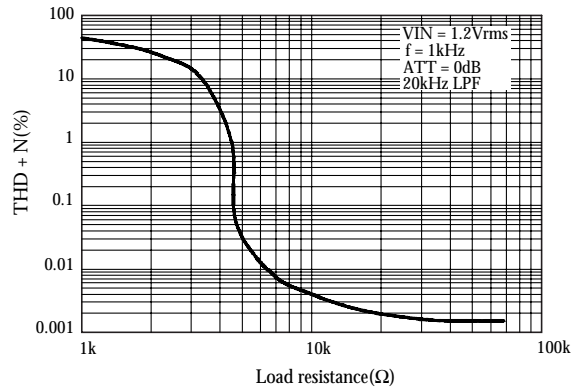


Figure 10. THD + N vs. load resistance

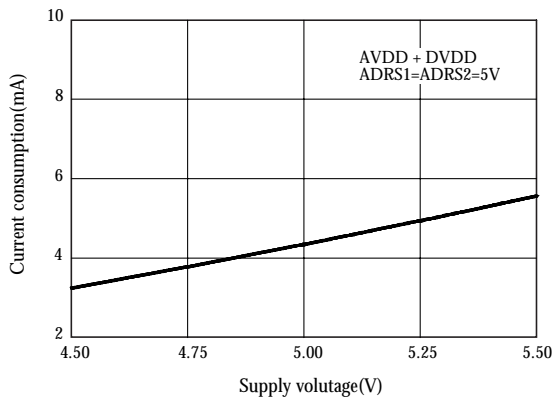


Figure 11. Current consumption vs. supply voltage

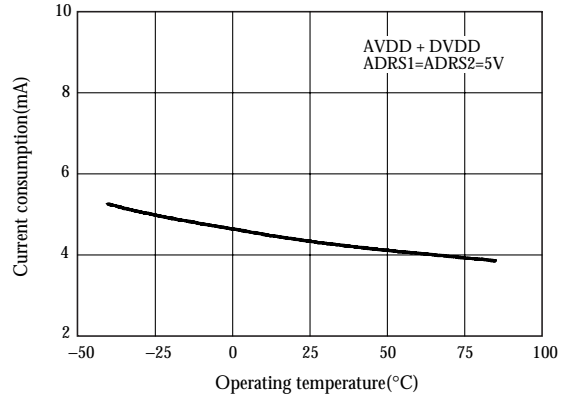


Figure 12. Current consumption vs. temperature

TYPICAL APPLICATIONS

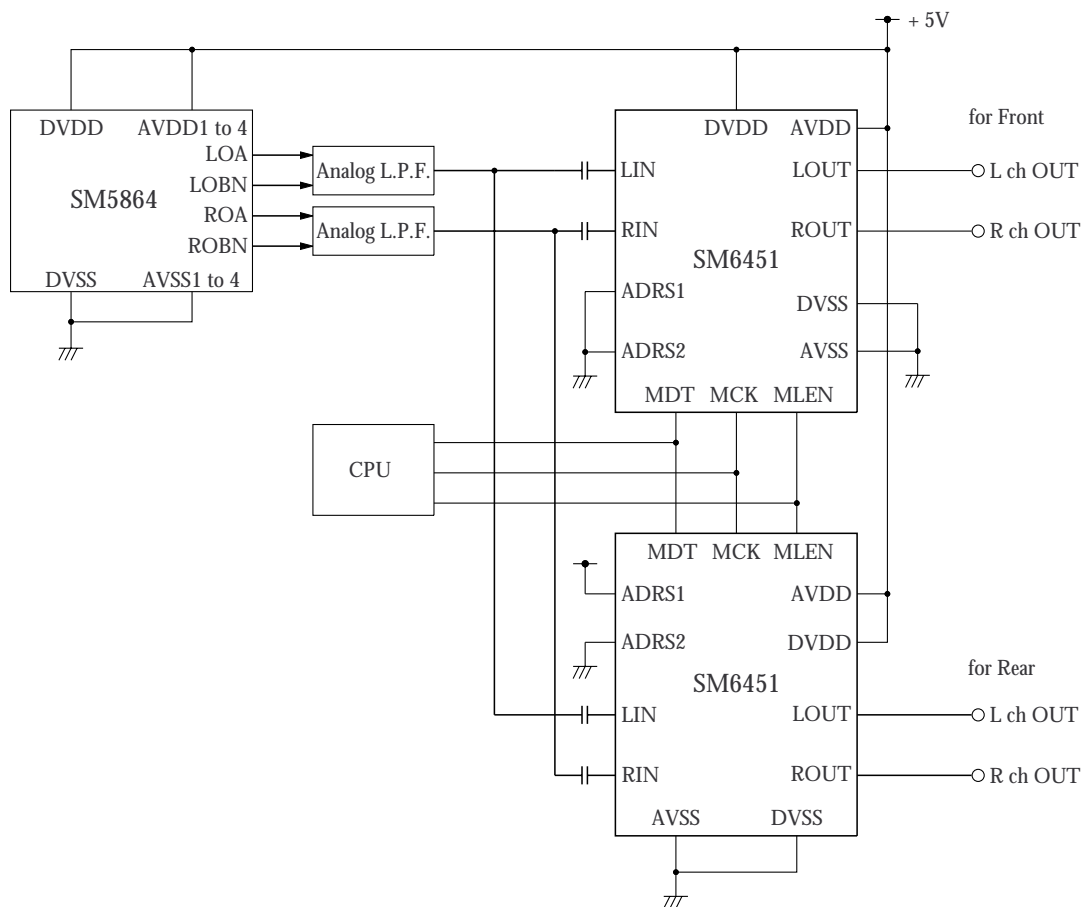
Connection Guidelines

Decoupling capacitors of approximately 10 μF should be connected from AVDD, VRL, VRR to AVSS, and from DVDD to DVSS.

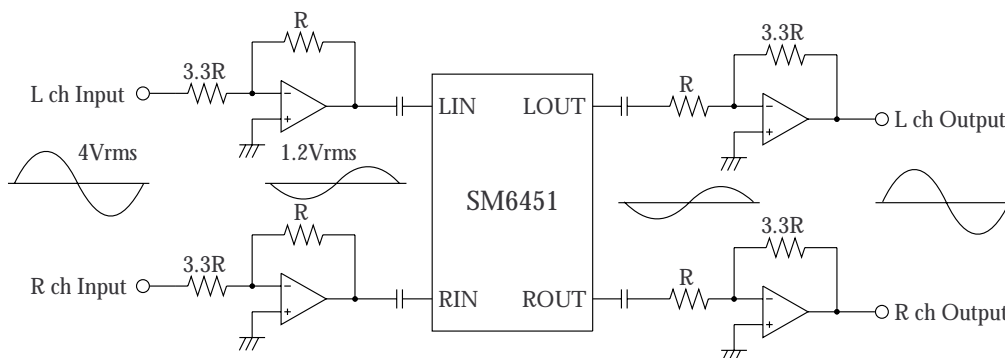
In addition, approximately 0.01 μF capacitors should also be connected from AVDD, VRL, VRR to AVSS, and from DVDD to DVSS to suppress digital switch noise.

An approximately 0.001 μF capacitor connected from RSTN to DVSS will force a system reset when power is applied.

Connection 1 (to DAC)

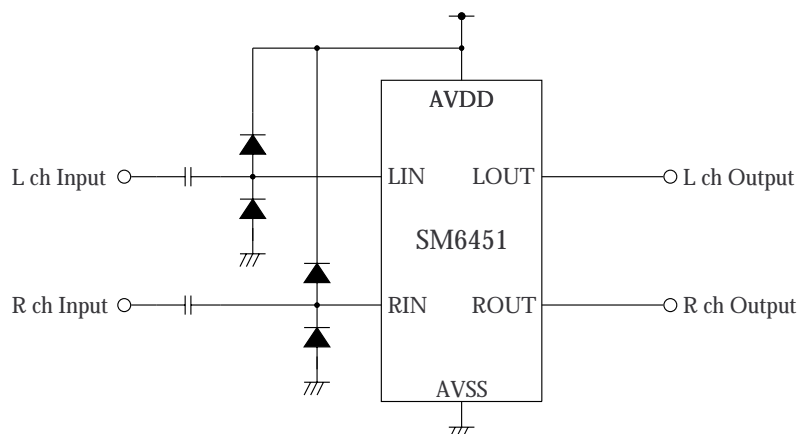


Connection 2



The SM6451AV uses a 1.2 Vrms input reference amplitude. If the input signal is 4 Vrms, then the input must be reduced by a factor of 1/3.3, and the output increased by a factor of 3.3.

Connection 3



When there is a possibility that the input peak-to-peak amplitude will exceed the supply voltage, input protection diodes should be connected to prevent device breakdown.

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