NIPPON PRECISION CIRCUITS INC.

SM8720AV

3-PLL Multi-Output Clock Generator

OVERVIEW

The SM8720AV is a clock generator IC with 3 built-in PLLs. It can simultaneously output a 27MHz master clock and three other clocks with different frequency (CLK1OUT, CLK2OUT, CLK3OUT) derived from the master clock. The 3 generated clocks can be independently turned ON/OFF using control pins and the frequency of CLK3OUT can be switched, allowing unneeded clocks within a system to be switched OFF thereby reducing current consumption. The master clock, supplied by high-stability crystal oscillator external input, allows clocks to be generated with high precision and low jitter and which require no frequency adjustment, making the SM8720AV ideal for digital still cameras and other applications which require multiple high-precision clocks.

FEATURES

- 2.7 to 3.3V supply voltage
- 21mA typ. current consumption
  (V_{DD} = 3.0V, all outputs with no load)
- 27MHz master clock (external input)
  (internal PLL reference clock)
- Generated clocks
  - 27MHz master clock (REFOUT)
  - 22.5792MHz (CLK1OUT)
    (ON/OFF switching using control pin)
  - 48.0000MHz (CLK2OUT)
    (ON/OFF switching using control pin)
  - 36/45/48.6MHz (CLK3OUT)
    (ON/OFF switching using control pin, frequency switching)
- Output load
  - 25pF (REFOUT)
  - 15pF (all outputs excluding REFOUT)
- Low jitter output
  - 140ps typ. peak-to-peak (REFOUT)
  - 220ps typ. peak-to-peak
    (CLK1OUT, CLK3OUT)
  - 220ps typ. peak-to-peak (CLK2OUT)
- 16-pin VSOP package (Pb free)

APPLICATIONS

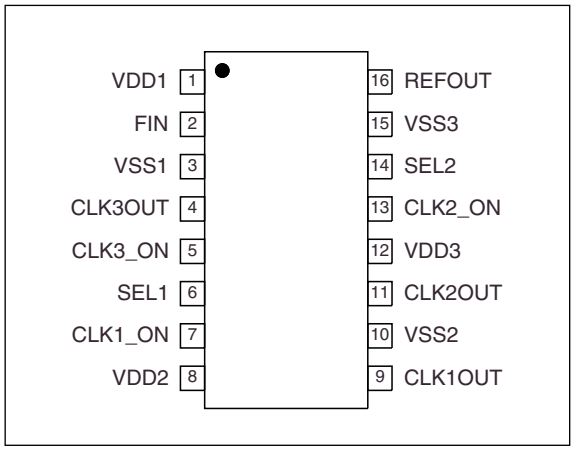
- Digital still cameras

ORDERING INFORMATION

Device	Package
SM8720AV	16-pin VSOP

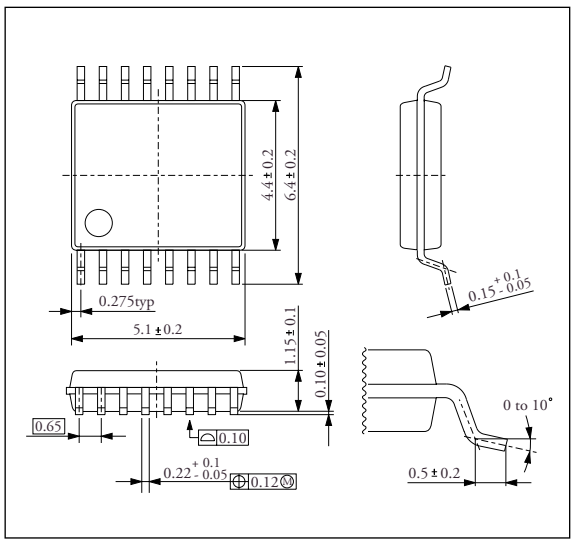
PINOUT

(Top view)

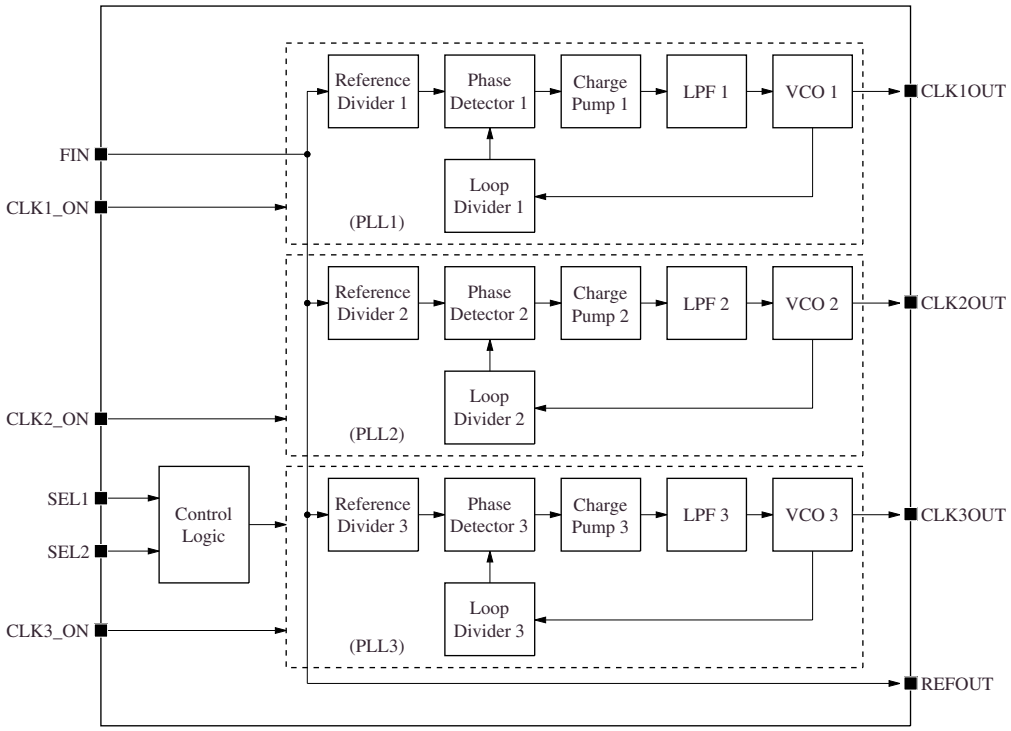


PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.07g



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	VDD1	–	Supply voltage 1
2	FIN	I	Master clock input (27MHz constant input)
3	VSS1	–	Supply ground 1
4	CLK3OUT	O	Clock output 3 (36/45/48.6MHz switchable output)
5	CLK3_ON	I	Output clock enable 3 (HIGH = enable, LOW = disable)
6	SEL1	I	Output select 1
7	CLK1_ON	I	Output clock enable 1 (HIGH = enable, LOW = disable)
8	VDD2	–	Supply voltage 2
9	CLK1OUT	O	Clock output 1 (22.5792MHz constant output)
10	VSS2	–	Supply ground 2
11	CLK2OUT	O	Clock output 1 (48MHz constant output)
12	VDD3	–	Supply voltage 3
13	CLK2_ON	I	Output clock enable 3 (HIGH = enable, LOW = disable)
14	SEL2	I	Output select 2
15	VSS3	–	Supply ground 3
16	REFOUT	O	Master clock output (27MHz constant output)

ABSOLUTE MAXIMUM RATINGS

$V_{DD} = (V_{DD1}, V_{DD2}, V_{DD3})$, $V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3})$ unless otherwise noted.

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD1}, V_{DD2}, V_{DD3}$	–0.3 to 6.5	V
Supply voltage deviation	$V_{DD1} - V_{DD2}, V_{DD1} - V_{DD3}, V_{DD2} - V_{DD3}$	±0.1	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	165	mW
Storage temperature range	T_{STG}	–55 to 125	°C

RECOMMENDED OPERATING CONDITIONS

$V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3}) = 0V$, unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Supply voltage*1	$V_{DD1}, V_{DD2}, V_{DD3}$		2.7	–	3.3	V
Output load capacitance 1	C_{L1}	REFOUT output	–	–	25	pF
Output load capacitance 2	C_{L2}	CLK1OUT, CLK2OUT, CLK3OUT outputs	–	–	15	pF
Master clock frequency	f_{FIN}	External clock input	–	27.0000	–	MHz
Operating temperature	T_{OPR}		–40	–	+85	°C

*1. The supply voltages are with reference to V_{SS} = 0V.
It is recommended that the voltages applied to pins VDD1, VDD2, VDD3 be supplied from a single source.
If various voltage sources are used on pins VDD1, VDD2, VDD3, the voltage supplies should be applied simultaneously. If the timing of applying voltage supplies varies, the device may be damaged.

ELECTRICAL CHARACTERISTICS

DC Characteristics

f_{FIN} = 27.0000MHz, $V_{DD} = (V_{DD1}, V_{DD2}, V_{DD3}) = 3.0 \pm 0.3V$, $V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3}) = 0V$,
Ta = –40 to +85°C unless otherwise noted.

Parameter	Symbol	Pins	Conditions	Rating			Unit
				min	typ	max	
Current consumption	I_{DD}	VDD	V_{DD} = 3.0V, Ta = 25°C, all outputs operating without load	–	21	28	mA
Input voltage	V_{IH}	FIN, SEL1, SEL2, CLK1_ON, CLK2_ON, CLK3_ON*1,*2	V_{DD} = 3.0V	0.8V_{DD}	–	–	V
	V_{IL}			–	–	0.2V_{DD}	V
Input current	I_{IH1}	CLK1_ON, CLK2_ON, CLK3_ON*1	$V_{IN} = V_{DD}$	–	30	80	µA
	I_{IL1}		V_{IN} = 0V	–1	–	–	µA
	I_{IH2}	FIN, SEL1, SEL2*2	$V_{IN} = V_{DD}$	–	–	1	µA
	I_{IL2}		V_{IN} = 0V	–1	–	–	µA
Output voltage	V_{OH}	All outputs	I_{OH} = –2mA	V_{DD} – 0.4	–	–	V
	V_{OL}		I_{OL} = 2mA	–	–	0.4	V

*1. CLK1_ON, CLK2_ON, CLK3_ON pins have Schmitt-trigger inputs with internal pull-down resistance.
*2. SEL1, SEL2 pins have Schmitt-trigger inputs.

AC Characteristics

f_{FIN} = 27.0000MHz, V_{DD} = (V_{DD1}, V_{DD2}, V_{DD3}) = 3.0 ± 0.3V, V_{SS} = (V_{SS1}, V_{SS2}, V_{SS3}) = 0V,
Ta = –40 to +85°C unless otherwise noted.

Parameter	Symbol	Pins	Conditions	Rating			Unit
				min	typ	max	
External input clock frequency	f_{FIN}	FIN	External clock input	–	27.0000	–	MHz
External clock duty cycle*1	Dt_{FIN}	FIN	Ta = 25°C, V_I = 0.5V_{DD}, external clock input	45	50	55	%
Output clock rise time*2	t_r	REFOUT	C_L = 25pF, V_{OL} = 0.2V_{DD} to V_{OH} = 0.8V_{DD} transition	–	–	3.0	ns
		All outputs excluding REFOUT	C_L = 15pF, V_{OL} = 0.2V_{DD} to V_{OH} = 0.8V_{DD} transition	–	–	4.0	ns
Output clock fall time*2	t_f	REFOUT	C_L = 25pF, V_{OH} = 0.8V_{DD} to V_{OL} = 0.2V_{DD} transition	–	–	3.0	ns
		All outputs excluding REFOUT	C_L = 15pF, V_{OH} = 0.8V_{DD} to V_{OL} = 0.2V_{DD} transition	–	–	4.0	ns
Output clock jitter (peak-to-peak)*3,*4	t_{jitter}	REFOUT	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	–	140	200	ps
		CLK1OUT, CLK3OUT	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	220	350	ps
		CLK2OUT	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	–	220	500	ps
Output clock duty cycle	Dt	REFOUT*2,*5	Ta = 25°C, C_L = 25pF, V_O = 0.5V_{DD}	45	50	55	%
		All outputs excluding REFOUT*2	Ta = 25°C, C_L = 15pF, V_O = 0.5V_{DD}	45	50	55	%
Power-up time*2,*6	t_P	All outputs excluding REFOUT		–	1	5	ms

*1. When using an external clock input, it is recommended that FIN duty cycle = 50%, clock signal amplitude = V_{DD} level. Note that the input signal voltage amplitude should not exceed the absolute maximum rating, otherwise the device may be damaged.
*2. Measured using the circuit shown in figure 1 on the NPC standard evaluation board.
*3. Measured using the circuit shown in figure 2 on the NPC standard evaluation board.
*4. Measured using master clock input on FIN with ≤80ps (peak-to-peak) jitter.
*5. Measured using master clock input on FIN with duty cycle = 50%, clock signal amplitude = V_{DD} level.
*6. The power-up time is the time from supply OFF/ON transition or enable LOW/HIGH transition until each output clock reaches its designated frequency to within ±0.1%.

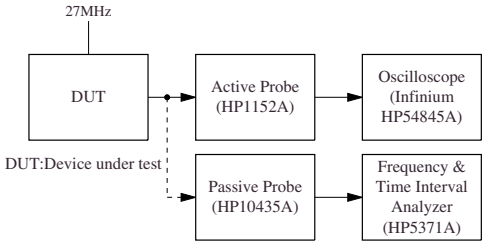


Figure 1. Measurement circuit 1

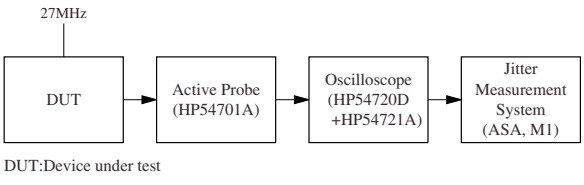


Figure 2. Measurement circuit 2

FUNCTIONAL DESCRIPTION

27MHz Master Clock

The 27MHz master clock is an external clock input on pin FIN as shown in figure 3. It is recommended that the master clock have 27.0000MHz frequency, 50% duty, and V_{DD} level amplitude.

Note that the FIN input clock amplitude voltage level should not exceed the absolute maximum rating, otherwise the device may be damaged.

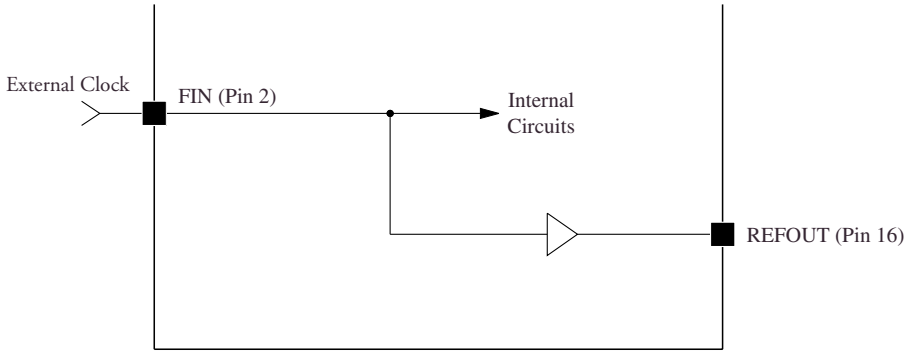


Figure 3. External clock input

Output Clock Frequency

The SM8720AV generates 3 output clocks with frequency 22.5792MHz (CLK1OUT), 48MHz (CLK2OUT), and 36/45/48.6MHz (CLK3OUT), derived from the master clock. In addition, the 27MHz master clock is output on REFOUT. A list of the supported clock frequency and control settings is shown in table 1.

Table 1. Output clock frequency (27.0000MHz master clock frequency)

CLK1_ON (Pin 7)	CLK2_ON (Pin 13)	CLK3_ON (Pin 5)	Output clock frequency [MHz]					
			REFOUT (Pin 16)	CLK1OUT (Pin 9)	CLK2OUT (Pin 11)	CLK3OUT (Pin 4)		
						SEL1 = H (Pin 6) SEL2 = L (Pin 14)	SEL1 = L (Pin 6) SEL2 = L (Pin 14)	SEL1 = L (Pin 6) SEL2 = H (Pin 14)
H	H	H	27.0000	22.5792	48.0000	36.0000	45.0000	48.6000
L			27.0000	L	48.0000	36.0000	45.0000	48.6000
H	L		27.0000	22.5792	L	36.0000	45.0000	48.6000
L			27.0000	L	L	36.0000	45.0000	48.6000
H	H	L	27.0000	22.5792	48.0000	L	L	L
L			27.0000	L	48.0000	L	L	L
H	L		27.0000	22.5792	L	L	L	L
L			27.0000	L	L	L	L	L

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