



Austin Semiconductor, Inc.

# UVEPROM SMJ27C256

## 256K UVEPROM

UV Erasable Programmable  
Read-Only Memory

### AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-86063
- MIL-STD-883

### FEATURES

- Organized 32,768 x 8
- Single +5V ±10% power supply
- Pin-compatible with existing 256K ROM's and EPROM's
- All inputs/outputs fully TTL compatible
- Power-saving CMOS technology
- Very high-speed SNAP! Pulse Programming
- 3-state output buffers
- 400-mV DC assured noise immunity with standard TTL loads
- Latchup immunity of 250 mA on all input and output pins
- Low power dissipation (CMOS Input Levels)
  - ✓ Active - 165mW Worst Case
  - ✓ Standby - 1.7mW Worst Case (CMOS-input levels)

### OPTIONS

- **Timing**
  - 150ns access -15
  - 170ns access -17
  - 200ns access -20
  - 250ns access -25
  - 300ns access -30

### Package(s)

Ceramic DIP (600mils)      J      No. 110

### Operating Temperature Ranges

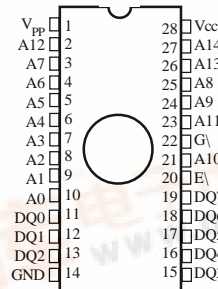
Military (-55°C to +125°C)      M

### MARKING

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### PIN ASSIGNMENT (Top View)

32-Pin DIP (J)  
(600 MIL)



Pin Name	Function
A0 - A14	Address Inputs
DA0-DQ7	Inputs (programming)/Outputs
E\	Chip Enable/Power Down
G\	Output Enable
GND	Ground
V <sub>CC</sub>	5V Supply
V <sub>PP</sub>	13V Programming Power Supply

### GENERAL DESCRIPTION

The SMJ27C256 series is a set of 262,144 bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus. The SMJ27C256 is pin-compatible with 28-pin 256K ROMs and EPROMs. It is offered in a 600mil dual-in-line ceramic package (J suffix) rated for operation from -55°C to 125°C.

Because this EPROM operates from a single 5V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other supply (13V) is needed for programming. All programming signals are TTL level. This device is programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V<sub>pp</sub> of 13V and a V<sub>cc</sub> of 6.5V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

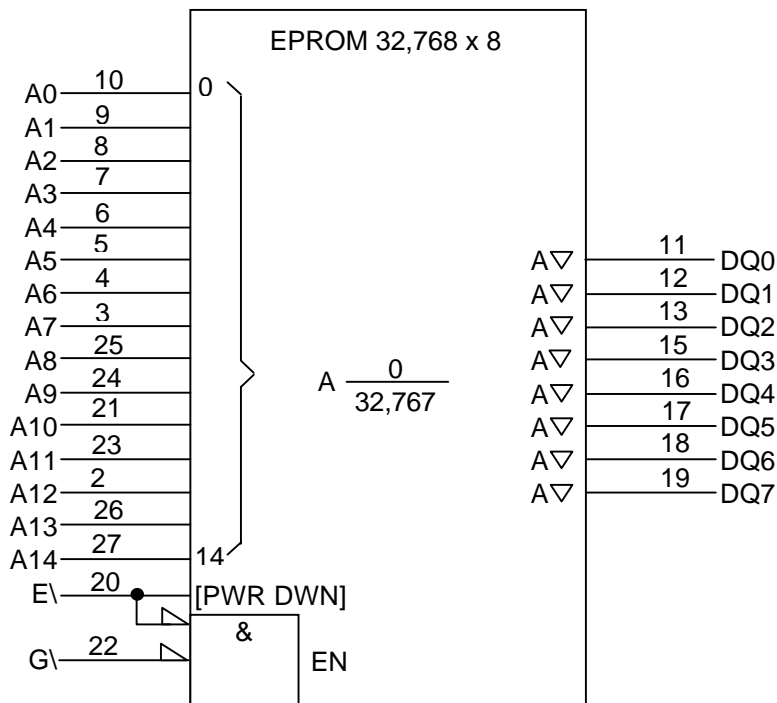




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## FUNCTIONAL BLOCK DIAGRAM\*



\* This symbol is in accordance with ANSI/IEEE std 91-1984 and IEC Publication 617-12.

### OPERATION

The seven modes of operation for the SMJ27C256 are listed in Table 1. The read mode requires a single 5V supply. All inputs are TTL level except for  $V_{PP}$  during programming (13V for SNAP! Pulse), and (12V) on A9 for signature mode.

**TABLE 1. OPERATION MODES**

FUNCTION (PINS)	MODE*						
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE
E\ (20)	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$
G\ (22)	$V_{IL}$	$V_{IH}$	X	$V_{IH}$	$V_{IL}$	X	$V_{IL}$
$V_{PP}$ (1)	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{PP}$	$V_{PP}$	$V_{PP}$	$V_{CC}$
$V_{CC}$ (28)	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
A9 (24)	X	X	X	X	X	X	$V_{ID}$   $V_{ID}$
A0 (10)	X	X	X	X	X	X	$V_{IL}$   $V_{IH}$
DQ0-DQ7 (11-13, 15-19)	Data Out	High-Z	High-Z	Data In	Data Out	High-Z	CODE
							MFG   DEVICE
							97   04

\* X can be  $V_{IL}$  or  $V_{IH}$ .



### READ/OUTPUT DISABLE

When the outputs of two or more SMJ27C256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C256, a low-level signal is applied to  $E\backslash$  and  $G\backslash$ . All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

### LATCHUP IMMUNITY

Latchup immunity on the SMJ27C256 is a minimum of 250mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the printed circuit board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

### POWER DOWN

Active  $I_{CC}$  supply current can be reduced from 25mA (SMJ27C256-15 through SMJ27C256-25) to 500 $\mu$ A (TTL-level inputs) or 300 $\mu$ A (CMOS-level inputs) by applying a high TTL/CMOS signal to the  $E\backslash$  pin. In this mode all outputs are in the high-impedance state.

### ERASURE

Before programming, the SMJ27C256 is erased by exposing the chip through the transparent lid to a high-intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to ensure that all bits are in the logic-high state. Logic-lows are programmed into the desired locations. A programmed logic-low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity x exposure time) is 15W•s/cm<sup>2</sup>. A typical 12mW/cm<sup>2</sup>, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure; therefore, when using the SMJ27C256, the window should be covered with an opaque label.

### SNAP! PULSE PROGRAMMING

The SMJ27C256 EPROM is programmed by using the SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1. This algorithm programs the device in a nominal time of 4 seconds. Actual programming time varies as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable,  $E\backslash$  is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds ( $\mu$ s) followed by a byte-verification step to determine when the addressed byte has been successfully programmed. Up to ten 100 $\mu$ s pulses per byte are provided before a failure is recognized.

The programming mode is achieved when  $V_{PP} = 13V$ ,  $V_{CC} = 6.5V$ ,  $G\backslash = V_{IH}$ , and  $E\backslash = V_{IL}$ . More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is completed, all bits are verified with  $V_{CC} = V_{PP} = 5V$ .

### PROGRAM INHIBIT

Programming can be inhibited by maintaining a high-level input on  $E\backslash$ .

### PROGRAM VERIFY

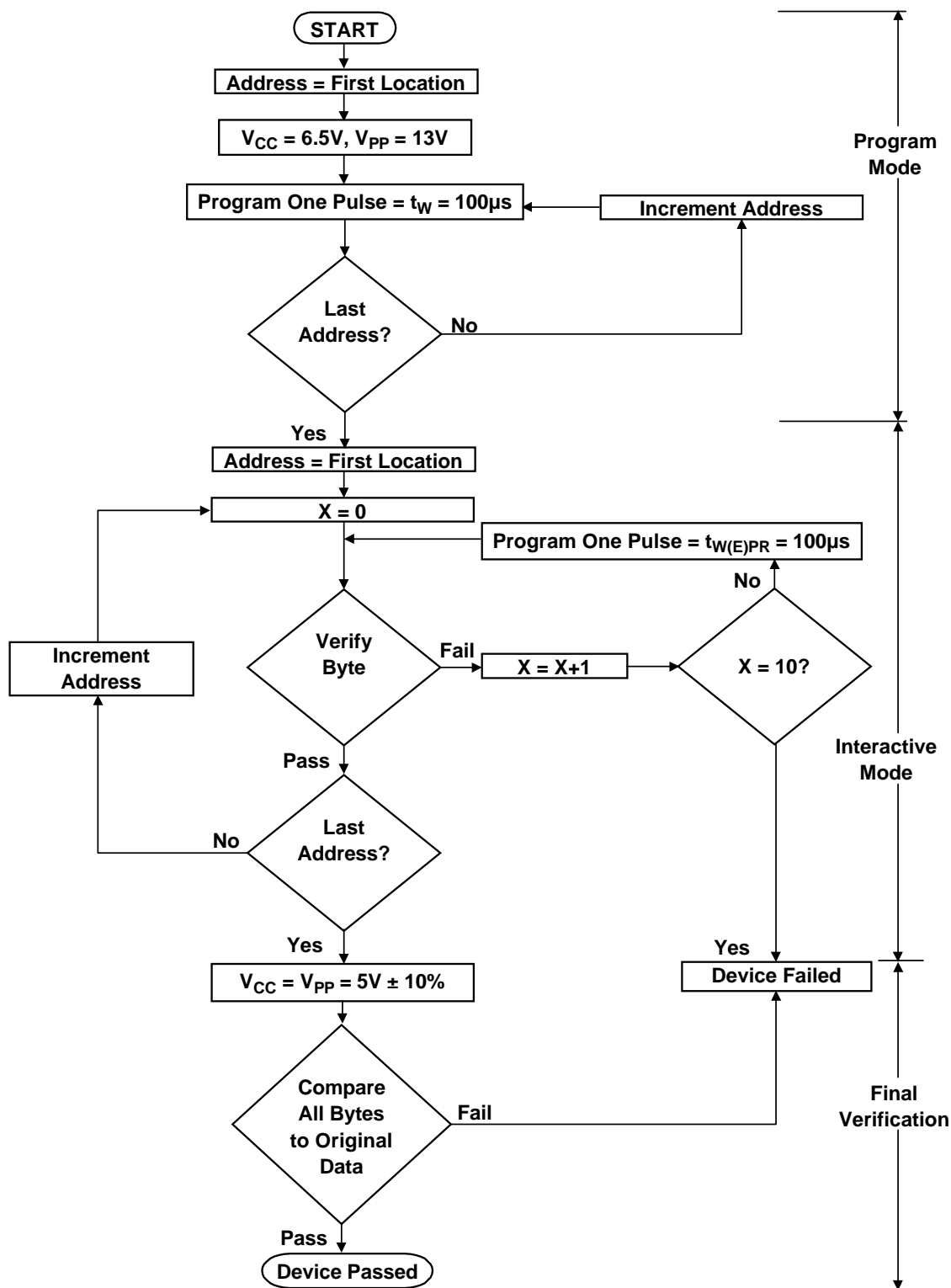
Programmed bits can be verified with  $V_{PP} = 13V$  when  $G\backslash = V_{IL}$ , and  $E\backslash = V_{IH}$ .

### SIGNATURE MODE

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 is forced to 12V  $\pm$ 0.5V. Two identifier bytes are accessed by A0 (terminal 10); i.e.,  $A0 = V_{IL}$  accesses the manufacturer code, which is output on DQ0-DQ7;  $A0 = V_{IH}$  accesses the device code, which is also output on DQ0-DQ7. All other addresses must be held at VIL. Each byte contains odd parity on bit DQ7. The manufacturer code for these devices is 97h and the device code is 04h.



**FIGURE 1. SNAP! PULSE PROGRAMMING FLOW CHART**







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**UVEPROM**  
**SMJ27C256**

**CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE,  $f = 1\text{MHz}^*$**

PARAMETER		TEST CONDITIONS	TYP**	MAX	UNIT
$C_i$	Input capacitance	$V_I = 0V$	6	10	pF
$C_o$	Output capacitance	$V_O = 0V$	10	14	pF

\* Capacitance measurements are made on a sample basis only.

\*\* Typical values are at  $T_A = 25^\circ\text{C}$  and nominal voltages.

**SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE<sup>1,2</sup>**

PARAMETER		TEST CONDITIONS <sup>1,2</sup>	-15		-17		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	see Figure 2		150		170	ns
$t_{a(E)}$	Access time from E\			150		170	ns
$t_{en(G)R}$	Output enable time from G\			70		70	ns
$t_{dis}$	Disable time of output from G\ or E\, whichever occurs first <sup>3</sup>		0	55	0	55	ns
$t_{v(A)}$	Output data valid time after change of address, E\, or G\, whichever occurs first <sup>3</sup>		0		0		ns

PARAMETER		TEST CONDITIONS <sup>1,2</sup>	-20		-25		-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	see Figure 2		200		250		300	ns
$t_{a(E)}$	Access time from E\			200		250		300	ns
$t_{en(G)R}$	Output enable time from G\			75		100		120	ns
$t_{dis}$	Disable time of output from G\ or E\, whichever occurs first <sup>3</sup>		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, E\, or G\, whichever occurs first <sup>3</sup>		0		0		0		ns

**NOTES:**

1. Timing measurements are made at 2V for logic high and 0.8V for logic low (see figure 2).

2. Common test conditions apply for  $t_{dis}$  except during programming.

3. Value calculated from 0.5V delta to measured output level. This parameter is only sampled and not 100% tested.

**SWITCHING CHARACTERISTICS FOR PROGRAMMING:  $V_{CC} = 6.5V$  and  $V_{PP} = 13V$  (SNAP! Pulse),  $T_A = 25^\circ\text{C}$**

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from G\	0	130	ns
$t_{en(G)W}$	Output enable time from G\		150	ns



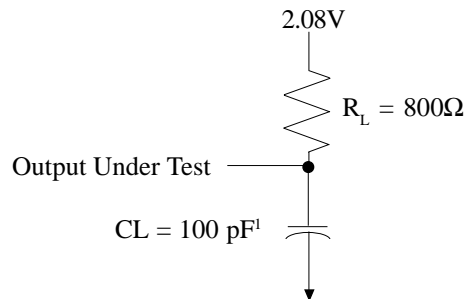
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**RECOMMENDED TIMING REQUIREMENTS FOR PROGRAMMING:  $V_{CC} = 6.5$  and  $V_{PP} = 13$  (SNAP! Pulse),  $T_A = 25^\circ\text{C}$  (See Figure 2)**

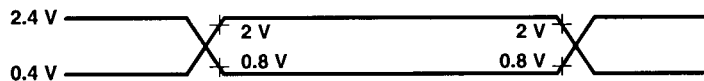
		MIN	TYP	MAX	UNIT
$t_{h(A)}$	Hold Time, Address	0			$\mu\text{s}$
$t_{h(D)}$	Hold Time, Data	2			$\mu\text{s}$
$t_{w(E)PR}$	Pulse Duration, Initial Program	95	100	105	$\mu\text{s}$
$t_{su(A)}$	Setup Time, Address	2			$\mu\text{s}$
$t_{su(G)}$	Setup Time, G\	2			$\mu\text{s}$
$t_{su(E)}$	Setup Time, E\	2			$\mu\text{s}$
$t_{su(D)}$	Setup Time, Data	2			$\mu\text{s}$
$t_{su(VPP)}$	Setup Time, $V_{PP}$	2			$\mu\text{s}$
$t_{su(VCC)}$	Setup Time, $V_{CC}$	2			$\mu\text{s}$

## PARAMETER MEASUREMENT INFORMATION



**NOTES:**

1.  $C_L$  includes probe and fixture capacitance.

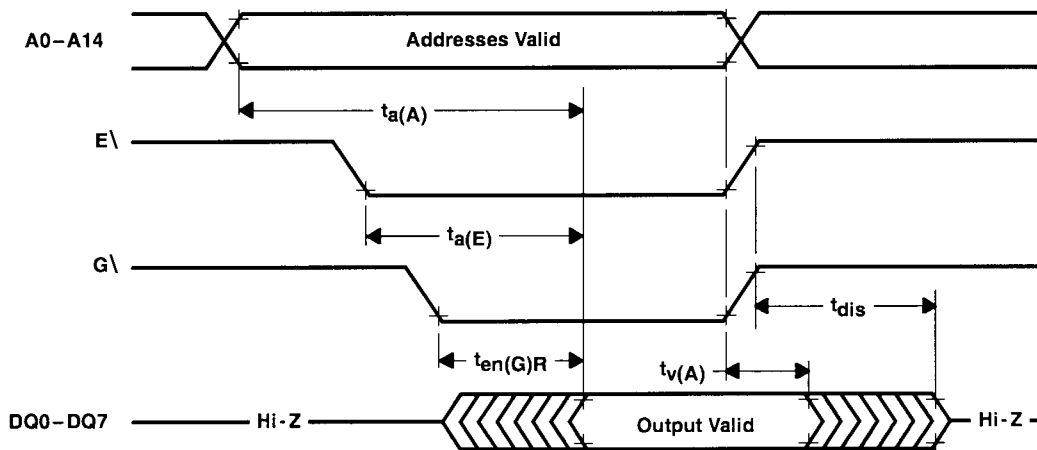


The AC testing inputs are driven at 2.4V for logic high and 0.4V for logic low. Timing measurements are made at 2V for logic high and 0.8V for logic low for both inputs and outputs.

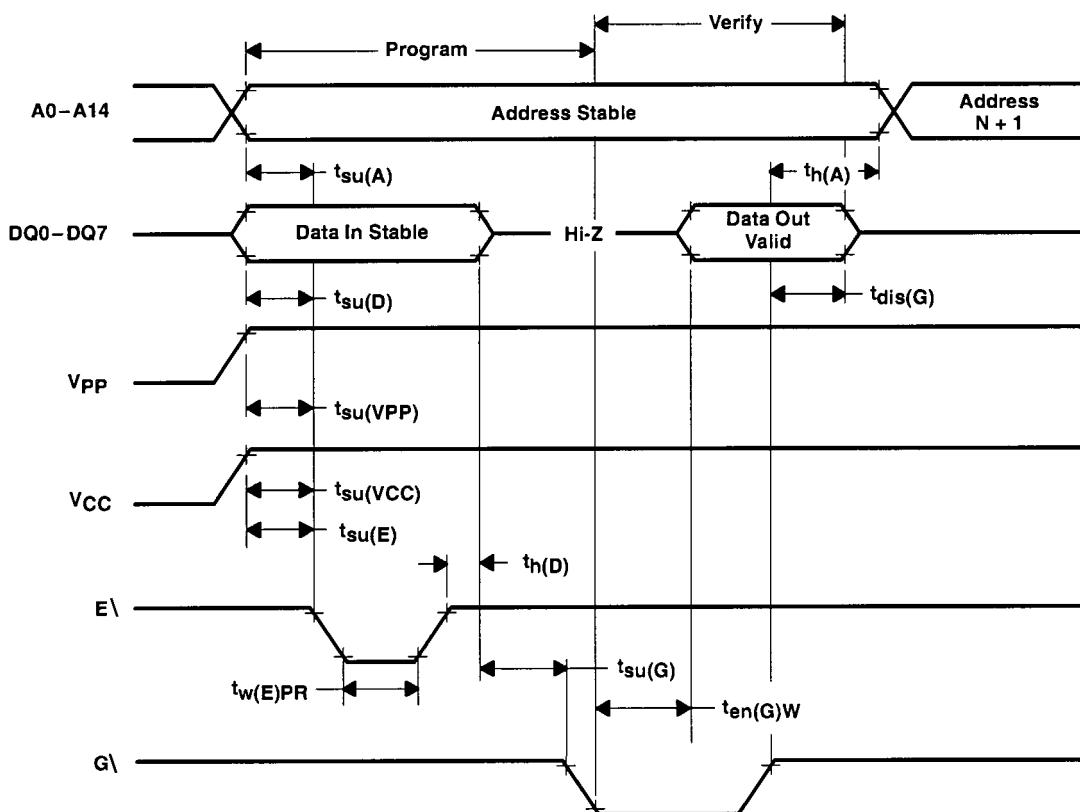
**FIGURE 2. LOAD CIRCUIT AND VOLTAGE WAVEFORMS**



**FIGURE 3. READ-CYCLE TIMING**



**FIGURE 4. PROGRAM-CYCLE TIMING (SNAP! PULSE PROGRAMMING)**





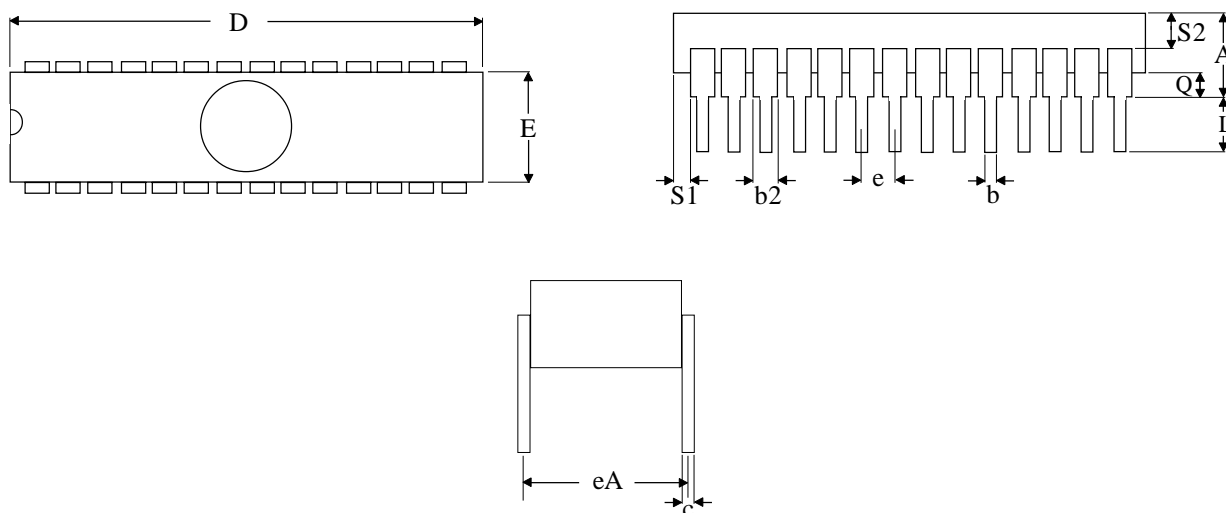


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**UVEPROM**  
**SMJ27C256**

**MECHANICAL DEFINITION\***

ASI Case #110 (Package Designator CW)  
SMD 5962-86063, Case Outline X



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.232
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---
S2	0.005	---

**NOTE:** These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.

\*All measurements are in inches.



## ORDERING INFORMATION

**EXAMPLE:** SMJ27C256-30JM

Device Number	Speed ns	Package Type	Operating Temp.
SMJ27C256	-15	J	*
SMJ27C256	-17	J	*
SMJ27C256	-20	J	*
SMJ27C256	-25	J	*
SMJ27C256	-30	J	*

### \*AVAILABLE PROCESSES

M = Extended Temperature Range

-55°C to +125°C



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**SMJ27C256**

## ASI TO DSCC PART NUMBER CROSS REFERENCE\*

### ASI Package Designator J

<u>TI Part #**</u>	<u>SMD Part #</u>
SMJ27C256-15JM	5962-8606305XA
SMJ27C256-17JM	5962-8606304XA
SMJ27C256-20JM	5962-8606301XA
SMJ27C256-25JM	5962-8606302XA
SMJ27C256-30JM	5962-8606303XA

\* ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.

\*\* Parts are listed on SMD under the old Texas Instruments part number. ASI purchased this product line in November of 1999.