

TEMIC

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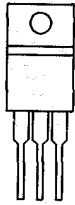
SMP40N10

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.040	40

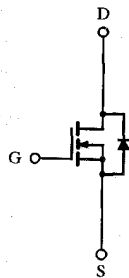
TO-220AB



G D S

Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	40
		$T_C = 100^\circ\text{C}$	25
Pulsed Drain Current	I_{DM}	160	A
Avalanche Current	I_{AR}	40	A
Avalanche Energy	E_A	240	mJ
Repetitive Avalanche Energy ^a	E_{AR}	40	mJ
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	125
		$T_C = 100^\circ\text{C}$	60
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature ($1/16''$ from case for 10 sec.)	T_L	300	$^\circ\text{C}$

6
 N-/P-Channel
 MOSFETS

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	$^\circ\text{C}/\text{W}$
Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	1.0		

Notes:

a. Duty cycle $\leq 1\%$

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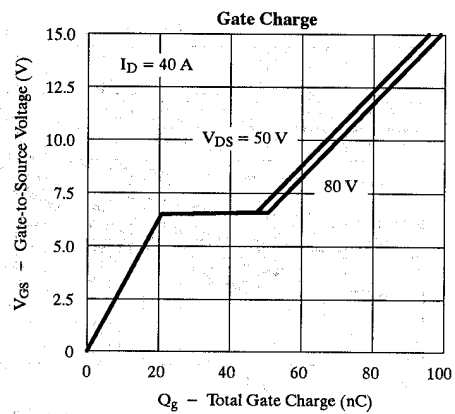
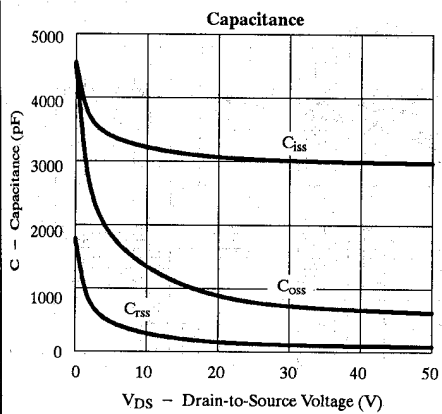
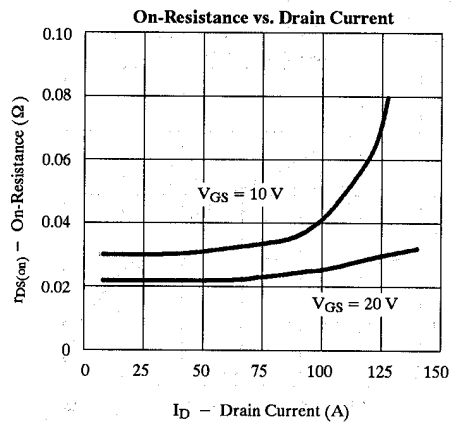
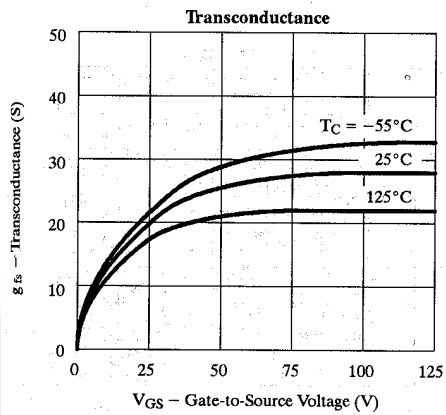
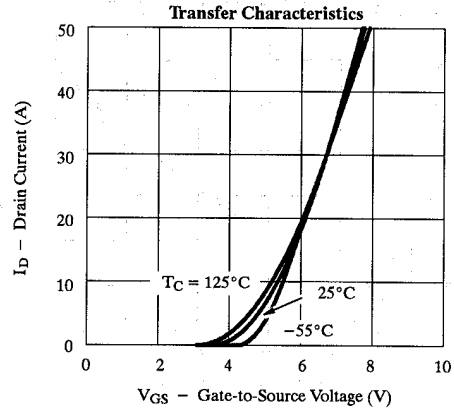
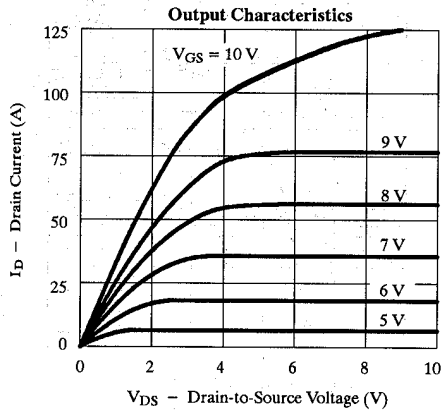
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0		4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			25	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		0.030	0.040	Ω
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}, T_J = 125^\circ\text{C}$		0.055	0.072	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$	15	20		S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		3000		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge ^c	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		62	80	nC
Gate-Source Charge ^c	Q_{gs}			20	30	
Gate-Drain Charge ^c	Q_{gd}			26	35	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 1.25\ \Omega$ $I_D = 40\text{ A}, V_{GEN} = 10\text{ V}, R_G = 5\ \Omega$		17	30	ns
Rise Time ^c	t_r			80	120	
Turn-Off Delay Time ^c	$t_{d(off)}$			40	60	
Fall Time ^c	t_f			20	40	
Source-Drain Diode Ratings and Characteristics ($T_C = 25^\circ\text{C}$)						
Continuous Current	I_S				40	A
Pulsed Current	I_{SM}				180	
Forward Voltage ^b	V_{SD}	$I_F = 40\text{ A}, V_{GS} = 0\text{ V}$			1.8	V
Reverse Recovery Time	t_{rr}			120	250	ns
Reverse Recovery Charge	Q_{rr}			0.3		μC

Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Independent of operating temperature.

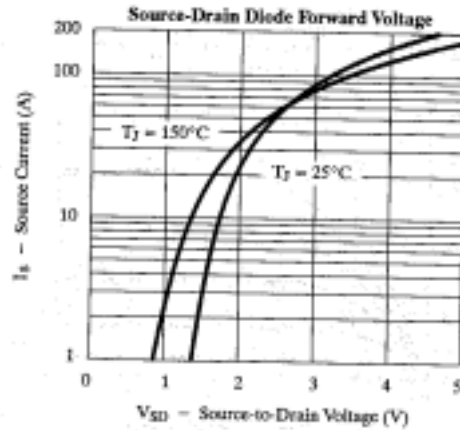
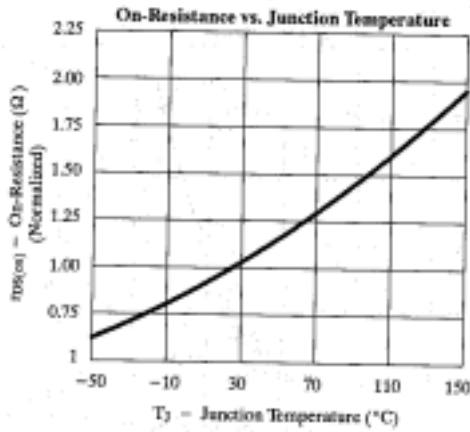
Typical Characteristics (25°C Unless Otherwise Noted)



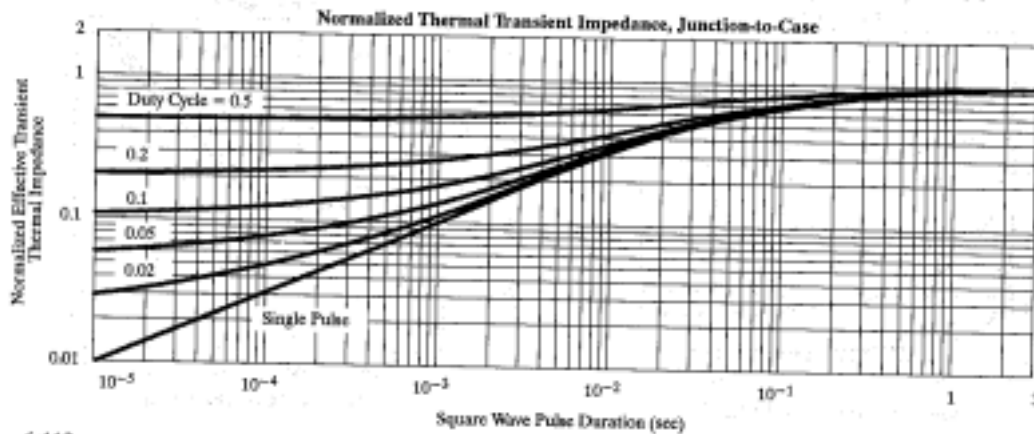
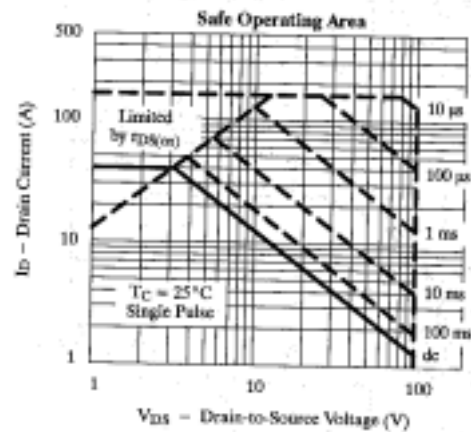
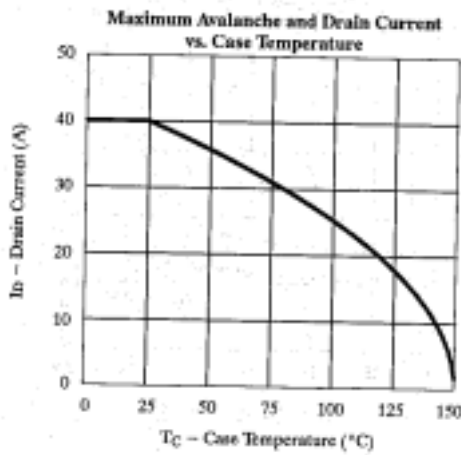
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Typical Characteristics (25°C Unless Otherwise Noted)



Thermal Ratings



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