

- **TTL-Compatible Inputs**
- **CCD-Compatible Outputs**
- **Full-Frame Operation**
- **Frame-Transfer Operation**
- **Solid-State Reliability**
- **Adjustable Clock Levels**

### description

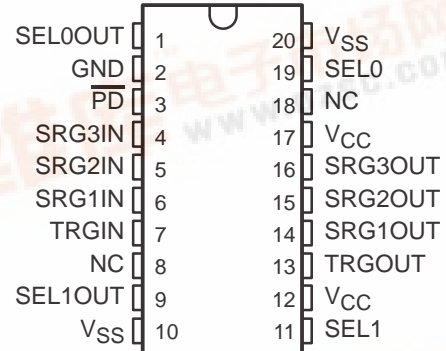
The SN28846 serial driver is a monolithic CMOS integrated circuit designed to drive the serial-register gate (SRGn) and transfer-gate (TRG) inputs of the Texas Instruments (TI™) virtual-phase CCD image sensors. The SN28846 interfaces a user-defined timing generator to the CCD image sensor; it receives TTL signals from the timing generator and outputs level-shifted signals to the image sensor. The SN28846 contains three noninverting serial-gate drivers and one noninverting transfer-gate driver.

The voltage levels on SRG1OUT, SRG2OUT, SRG3OUT, and TRGOUT are controlled by the levels on  $V_{SS}$  and  $V_{CC}$ . The propagation delays for these outputs are controlled by SEL0 and SEL1. The  $\overline{PD}$ , SRG1IN, SRG2IN, SRG3IN, and TRGIN are TTL compatible.

A high level on  $\overline{PD}$  allows the SN28846 to operate normally with the level-shifted outputs following the inputs. When  $\overline{PD}$  is low, the device is in a low power-consumption mode and all outputs are at  $V_{CC}$ .

The SN28846 is available in a 20-pin surface-mount package and is characterized for operation from  $-20^{\circ}\text{C}$  to  $45^{\circ}\text{C}$ .

**DW PACKAGE**  
**(TOP VIEW)**



NC – No internal connection



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either  $V_{CC}$  or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

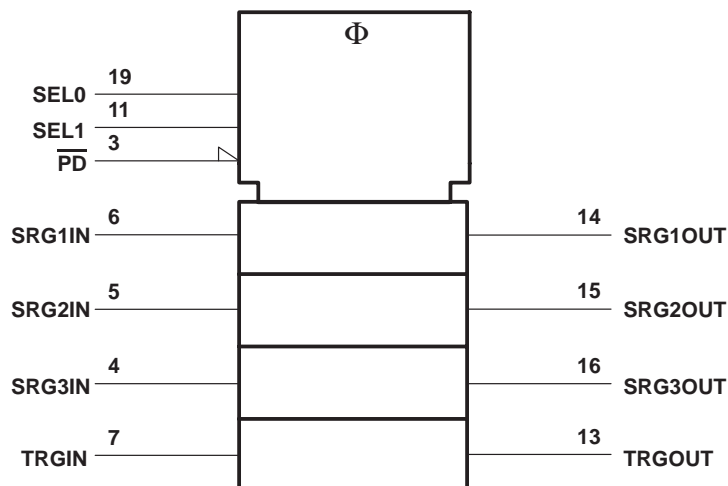
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# SN28846 SERIAL DRIVER

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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	2		Ground
NC‡	8		No connect
NC‡	18		No connect
PD	3	I	Power down
SEL0	19	I	Propagation delay mode select
SEL1	11	I	Propagation delay mode select
SEL0OUT	1	O	Test pin (factory use only)
SEL1OUT	9	O	Test pin (factory use only)
SRG1IN	6	I	Serial-register gate 1 in
SRG2IN	5	I	Serial-register gate 2 in
SRG3IN	4	I	Serial-register gate 3 in
SRG1OUT	14	O	Serial-register gate 1 out
SRG2OUT	15	O	Serial-register gate 2 out
SRG3OUT	16	O	Serial-register gate 3 out
TRGIN	7	I	Transfer gate in
TRGOUT	13	O	Transfer gate out
VCC‡	12	I	Positive supply voltage
VCC‡	17	I	Positive supply voltage
VSS‡	10	I	Negative supply voltage
VSS‡	20	I	Negative supply voltage

‡ All terminals of the same name should be connected together externally.

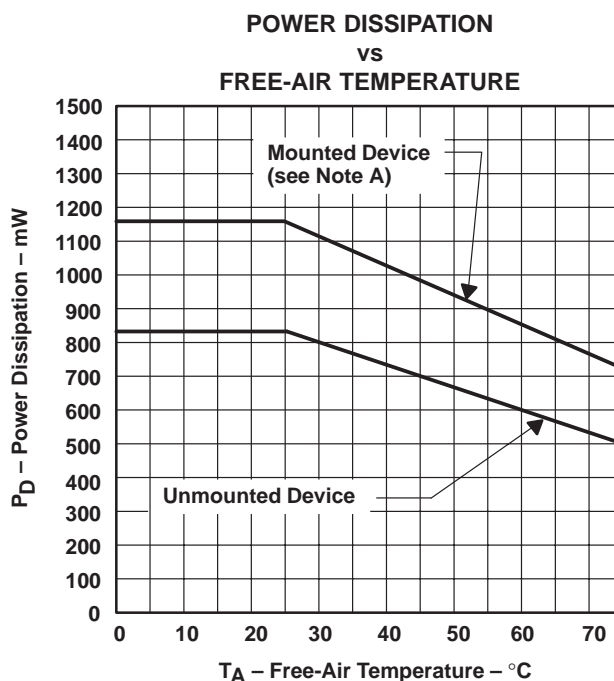
**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Positive supply voltage, $V_{CC}$ (see Note 1)	4 V
Negative supply voltage, $V_{SS}$ (see Note 2)	-11.1 V
Input voltage range: SEL0 and SEL1	$V_{SS}$ to $V_{CC}$
Other inputs	0 to 5.5 V
Continuous total power dissipation at (or below) $T_A \leq 25^\circ\text{C}$ : Unmounted device (see Figure 1)	825 mW
Mounted device (see Figure 1)	1150 mW
Operating free-air temperature range, $T_A$	-20°C to 45°C
Storage temperature range, $T_{STG}$	-55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminal.

2. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.



**Figure 1**

NOTE A: The mounted-device derating curve of Figure 1 is obtained under the following conditions:

The board is 50 mm by 50 mm by 1.6 mm thick.

The board material is glass epoxy.

The copper thickness of all the etch runs is 35 microns.

Etch run dimensions – All 20 etch runs are 0.4 mm by 22 mm.

Each chip is soldered to the board.

An aluminum cooling fin 10 mm by 10 mm by 1 mm thick is coupled to the chip with thermal paste.

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### recommended operating conditions

		MIN	NOM	MAX	UNIT
Positive supply voltage, $V_{CC}$		0	1.5	3	V
Negative supply voltage, $V_{SS}$ (see Note 2)		−11.1	−10.4	−9.7	
High-level input voltage, $V_{IH}$	SRG1IN, SRG2IN, SRG3IN, TRGIN	2	5	V	
	SEL0, SEL1	$V_{CC}$			
	$\overline{PD}$	4	5		
Low-level input voltage, $V_{IL}$	SRG1IN, SRG2IN, SRG3IN, TRGIN	0	0.8	V	
	SEL0, SEL1	$V_{SS}$			
	$\overline{PD}$	0	0.4		
Capacitance load	SRG1OUT, SRG2OUT, SRG3OUT	200		pF	
	TRGOUT	350			
Operating free-air temperature, $T_A$		−20	45	°C	

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels only.

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{OH}$ High-level output voltage	SRG1OUT, SRG2OUT, SRG3OUT	$f = 4.8 \text{ MHz}$ , $t_W = 70 \text{ ns}$ , See Figure 2	$V_{CC} - 0.5$	$V_{CC} + 0.5$	V
	TRGOUT	$f = 3.6 \text{ MHz}$ , $t_W = 140 \text{ ns}$ , See Figure 2			
$V_{OL}$ Low-level output voltage	SRG1OUT, SRG2OUT, SRG3OUT	$f = 4.8 \text{ MHz}$ , $t_W = 70 \text{ ns}$ , See Figure 2	$V_{SS} - 0.8$	$V_{SS} + 0.8$	V
	TRGOUT	$f = 3.6 \text{ MHz}$ , $t_W = 140 \text{ ns}$ , See Figure 2			
$V_{N(PP)}$ Peak-to-peak output noise voltage	SRG1OUT, SRG2OUT, SRG3OUT	See Figure 2		300	mV
$I_{IH}$ High-level input current	SRG1IN, SRG2IN, SRG3IN, TRGIN, SEL0, SEL1	$V_I = 5.5 \text{ V}$		50	$\mu\text{A}$
$I_{IL}$ Low-level input current		$V_I = 0$		$\pm 10$	$\mu\text{A}$
$I_{SS}$ Supply current		No load, $\overline{PD}$ at 0 V, $T_A = 25^\circ\text{C}$		-0.5	mA
		See Note 3		-25	
$f_{max}$ Maximum frequency of oscillation	SRG1OUT, SRG2OUT, SRG3OUT	$C_L = 200 \text{ pF}$	10		MHz
	TRGOUT	$C_L = 350 \text{ pF}$	1		

NOTE 3: SRG1OUT, SRG2OUT, and SRG3OUT are loaded with 80-pF capacitive loads; TRGOUT is loaded with a 180-pF load. The SN28846 driver is clocked by the SN28835 timer. SEL0 and SEL1 are both held at -11.1 V.

switching characteristics for SRG1OUT, SRG2OUT, and SRG3OUT,  $V_{CC} = 2.3\text{ V}$ ,  $V_{SS} = -10.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted) (see Figure 2)<sup>†</sup>

PARAMETER	SELECT MODE‡	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH Propagation delay time, low-to-high-level output	0	tW = 70 ns,      f = 4.8 MHz	28			ns
	1		36			
	2		42			
	3		48			
tPHL Propagation delay time, high-to-low-level output	0	tW = 70 ns,      f = 4.8 MHz	25			ns
	1		24			
	2		23			
	3		23			
ΔtPLH      (see Note 4)	Any	TA = −20°C to 55°C	±5			ns
ΔtPHL      (see Note 4)			±5			
tsk(o)      Skew time (see Note 5)			5			
			5			
tW Pulse duration	0	tW = 70 ns,      f = 4.8 MHz	63	68	73	ns
	1		54	59	64	
	2		47	52	57	
	3		40	45	50	
tW(n) − tW(m)       Pulse duration differential (see Note 6)	Any	tW = 70 ns,      f = 4.8 MHz	5			ns
tR Rise time	Any	tW = 70 ns,      f = 4.8 MHz	10	14	18	ns
tF Fall time			6	10	13	

<sup>†</sup> The load is a Texas Instruments CCD image sensor.

<sup>‡</sup> The select mode is determined by the voltage levels applied to the SEL1 and SEL0 inputs as follows:

SELECT MODE	SEL1	SEL0
0	V <sub>SS</sub>	V <sub>SS</sub>
1	V <sub>SS</sub>	V <sub>CC</sub>
2	V <sub>CC</sub>	V <sub>SS</sub>
3	V <sub>CC</sub>	V <sub>CC</sub>

- NOTES: 4. For a given channel,  $\Delta t_{PLH}$  and  $\Delta t_{PHL}$  are the changes in  $t_{PLH}$  and  $t_{PHL}$ , respectively, when the device is operated over the temperature range  $-20^\circ\text{C}$  to  $55^\circ\text{C}$  rather than at  $25^\circ\text{C}$ .
5. This is the maximum absolute difference in propagation delay time, either  $t_{PLH}$  or  $t_{PHL}$ , through the three channels at any given temperature within the specified range.
6. This is the maximum difference in the pulse duration through the three channels.

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switching characteristics for TRGOUT,  $V_{CC} = 2.3\text{ V}$ ,  $V_{SS} = -10.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)  
(see Figure 2)<sup>†</sup>

PARAMETER	SELECT MODE <sup>‡</sup>	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	0	$t_W = 140\text{ ns}$ , $f = 3.6\text{ MHz}$		24		ns
	1			33		
	2			39		
	3			47		
$t_{PHL}$ Propagation delay time, high-to-low-level output	0	$t_W = 140\text{ ns}$ , $f = 3.6\text{ MHz}$		24		ns
	1			23		
	2			22		
	3			22		
$\Delta t_{PLH}$ (see Note 7)	Any	$T_A = -20^\circ\text{C}$ to $55^\circ\text{C}$			20	ns
$\Delta t_{PHL}$ (see Note 7)					20	
$t_W$ Pulse duration	Any	$t_W = 140\text{ ns}$ , $f = 3.6\text{ MHz}$	100	140	180	ns
$t_r$ Rise time				17		
$t_f$ Fall time				10		

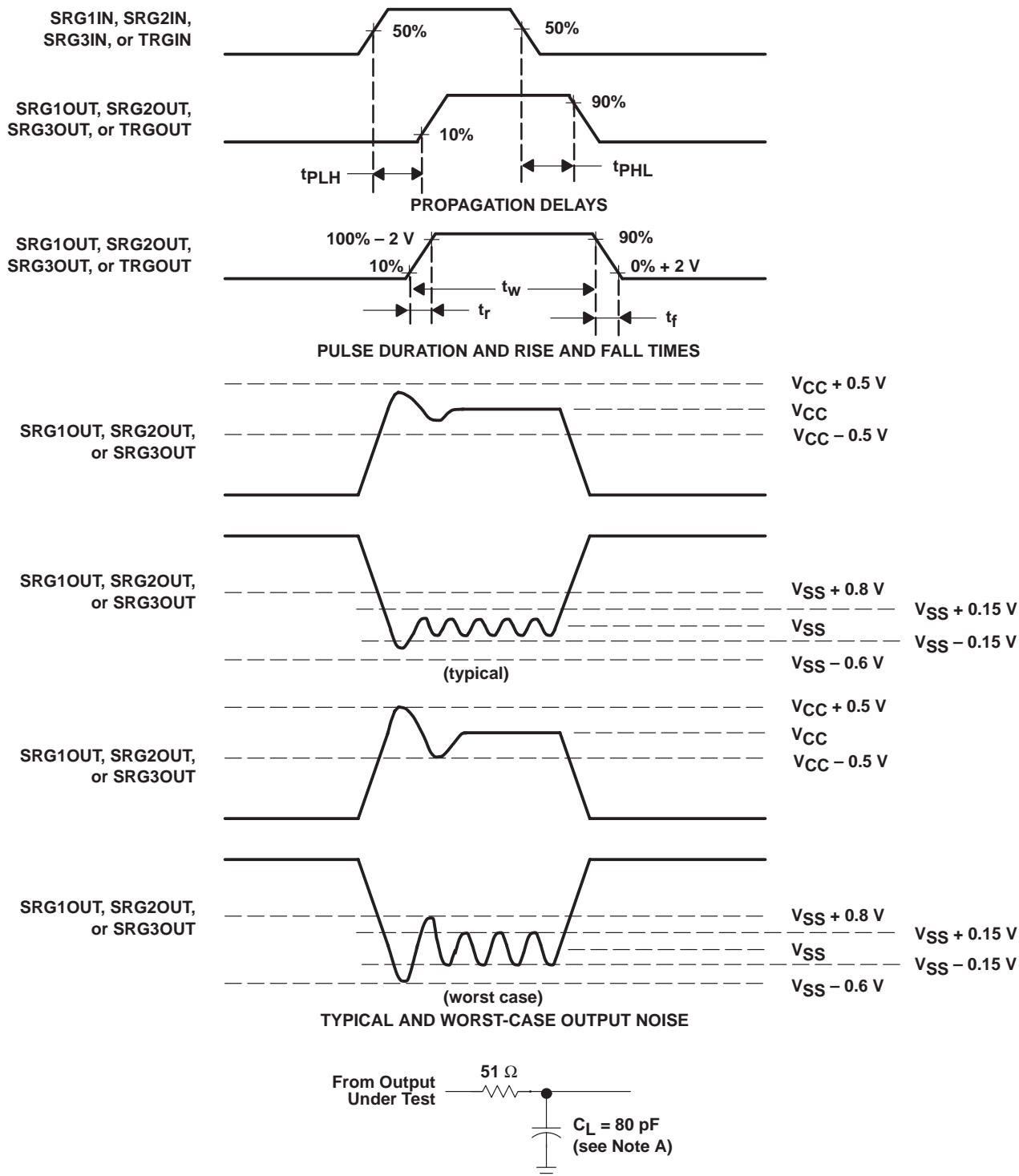
<sup>†</sup> The load is a Texas Instruments CCD image sensor.

<sup>‡</sup> The select mode is determined by the voltage levels applied to SEL1 and SEL0 as follows:

SELECT MODE	SEL1	SEL0
0	$V_{SS}$	$V_{SS}$
1	$V_{SS}$	$V_{CC}$
2	$V_{CC}$	$V_{SS}$
3	$V_{CC}$	$V_{CC}$

NOTE 7:  $\Delta t_{PLH}$  and  $\Delta t_{PHL}$  are the changes in  $t_{PLH}$  and  $t_{PHL}$ , respectively, when the device is operated over the temperature range  $-20^\circ\text{C}$  to  $55^\circ\text{C}$  rather than at  $25^\circ\text{C}$ .

## PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  Includes probe and jig capacitance.

Figure 2. Load Circuit and Voltage Waveforms

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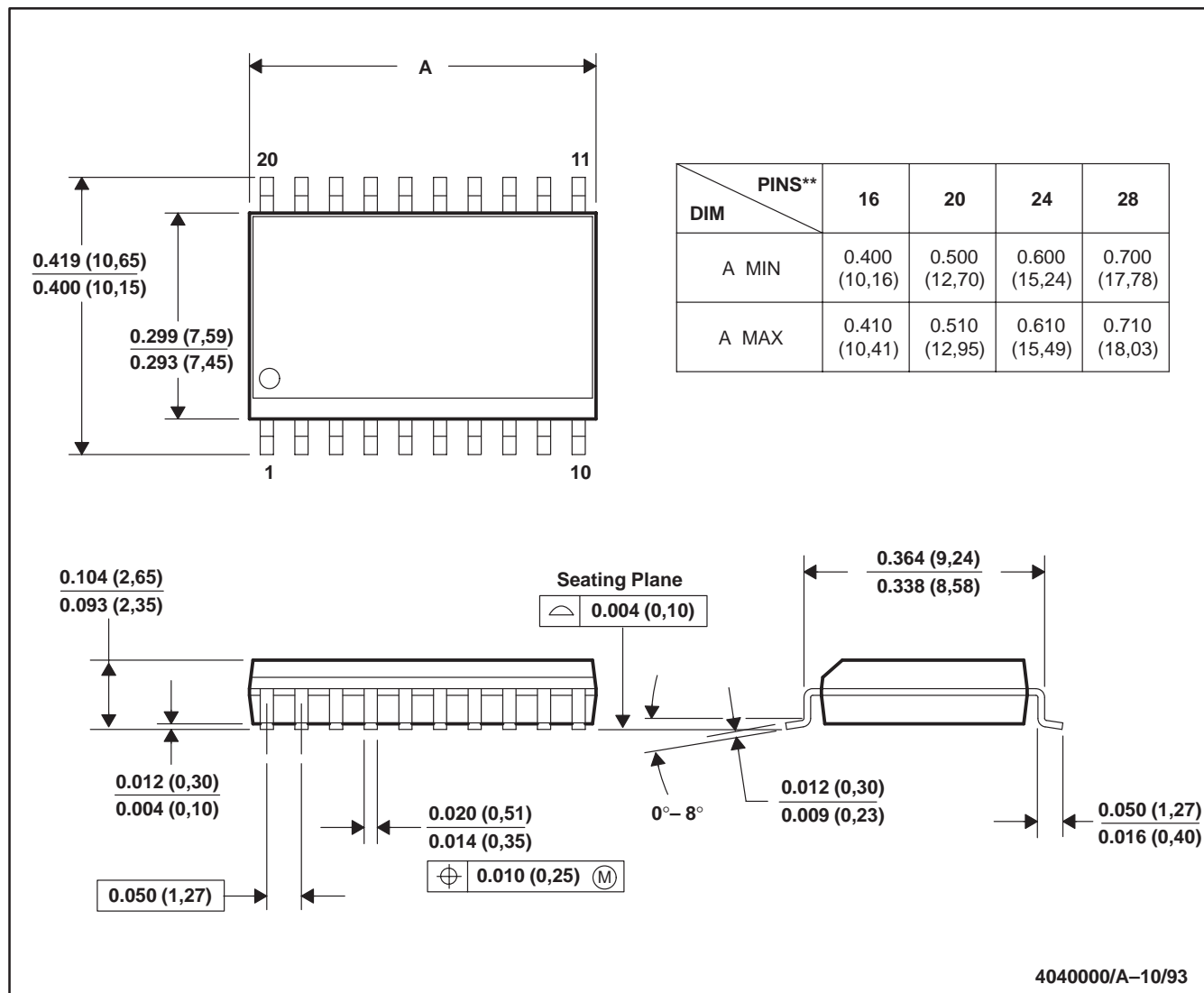
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## MECHANICAL DATA

DW/R-PDSO-G\*\*

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE

20 PIN SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).



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