# 3-V TO 5.5-V MULTICHANNEL RS-232 COMPATIBLE LINE DRIVER/RECEIVER

SLLS534B - MAY 2002 - REVISED OCTOBER 2004

- Operates With 3-V to 5.5-V V<sub>CC</sub> Supply
- Operates Up To 1 Mbit/s
- Low Standby Current . . . 1 μA Typ
- External Capacitors . . . 4 × 0.1 μF
- Accepts 5-V Logic Input With 3.3-V Supply
- RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)
- Applications
  - Battery-Powered Systems, PDAs,
    Notebooks, Laptops, Palmtop PCs, and
    Hand-Held Equipment

# DB, DW, OR PW PACKAGE (TOP VIEW)

EN[	1	20	PWRDOWN
C1+[	2	19	V <sub>CC</sub>
V+[	3	18	] GND
C1-[	4	17	DOUT1
C2+[	5	16	] RIN1
C2-[	6	15	] ROUT1
V-[	7	14	] NC
DOUT2[	8	13	DIN1
RIN2[	9	12	DIN2
ROUT2[	10	11	] NC

NC - No internal connection

### description/ordering information

The SN65C3222 and SN75C3222 consist of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). The devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ $\mu$ s to 150 V/ $\mu$ s.

The SN65C3222 and SN75C3222 can be placed in the power-down mode by setting  $\overline{PWRDOWN}$  low, which draws only 1  $\mu A$  from the power supply. When the devices are powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled, V+ is lowered to V<sub>CC</sub>, and V- is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting  $\overline{EN}$  high.

#### **ORDERING INFORMATION**

TA	PACKAG	PACKAGE <sup>†</sup>		TOP-SIDE MARKING
	0010 (D)40	Tube of 25	SN75C3222DW	7500000
	SOIC (DW)	Reel of 2000	SN75C3222DWR	75C3222
−0°C to 70°C	SSOP (DB)	Reel of 2000	SN75C3222DBR	CA3222
THE BE	TOOOD (DIA)	Tube of 70	SN75C3222PW	040000
FILE W	TSSOP (PW)	Reel of 2000	SN75C3222PWR	CA3222
Z 1	0010 (D)40	Tube of 25	SN65C3222DW	0500000
	SOIC (DW)	Reel of 2000	SN65C3222DWR	65C3222
–40°C to 85°C	SSOP (DB)	Reel of 2000	SN65C3222DBR	CB3222
	TCCOD (DW)	Tube of 70	SN65C3222PW	CD2222
	TSSOP (PW)	Reel of 2000	SN65C3222PWR	CB3222

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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#### **Function Tables**

#### **EACH DRIVER**

IN	OUTPUT	
DIN	PWRDOWN	DOUT
Х	L	Z
L	Н	Н
Н	Н	L

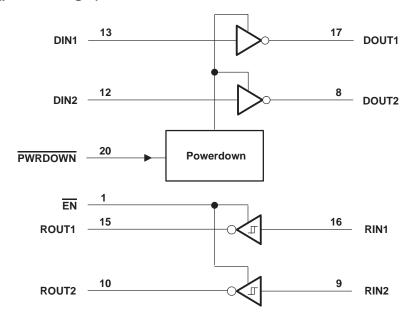
H = high level, L = low level, X = irrelevant, Z = high impedance

#### **EACH RECEIVER**

INPU	OUTPUT	
RIN	EN	ROUT
L	L	Н
Н	L	L
Х	Н	Z
Open	L	Н

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

# logic diagram (positive logic)





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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub> (see Note 1)		-0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1)		
Negative output supply voltage range, V- (see Note 1)		0.3 V to -7 V
Supply voltage difference, V+ - V- (see Note 1)		13 V
Input voltage range, V <sub>I</sub> : Drivers, EN, PWRDOWN		-0.3 V to 6 V
Receivers		-25 V to 25 V
Output voltage range, VO: Drivers		
Receivers	0.3 V to	$V_{CC} + 0.3 V$
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3):	DB package	70°C/W
	DW package	58°C/W
	PW package	83°C/W
Operating virtual junction temperature, T <sub>J</sub>		150°C
Storage temperature range, T <sub>stq</sub>		5°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

- 2. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions (see Note 4 and Figure 5)

				MIN	NOM	MAX	UNIT
	Oursels well and	V <sub>CC</sub> = 3.3 V		3	3.3	3.6	.,
	Supply voltage	V <sub>CC</sub> = 5 V		4.5	5	5.5	V
V	Driver and control bink level input voltage		V <sub>CC</sub> = 3.3 V	2			V
VIH	Driver and control high-level input voltage	DIN, EN, PWRDOWN	V <sub>CC</sub> = 5 V	2.4			V
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, EN, PWRDOWN				0.8	V
٧ <sub>I</sub>	Driver and control input voltage	DIN, EN, PWRDOWN		0		5.5	V
٧ <sub>I</sub>	Receiver input voltage			-25		25	V
т.		SN65C3222		-40		85	°C
TA	Operating free-air temperature	SN75C3222		0		70	°C

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
II	Input leakage current (EN, PWRDOWN)			±0.01	±1	μΑ
	Supply current	No load, PWRDOWN at VCC		0.3	1	mA
ICC	Supply current (powered off)	No load, PWRDOWN at GND		1	10	μΑ

‡ All typical values are at  $V_{CC}$  = 3.3 V or  $V_{CC}$  = 5 V, and  $T_A$  = 25°C. NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC}$  = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC}$  = 5 V  $\pm$  0.5 V.



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#### **DRIVER SECTION**

# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

	PARAMETER TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
VOH	High-level output voltage	DOUT at R <sub>L</sub> = $3 \text{ k}\Omega$ to GND,	DIN = GND	5	5.4		V
VOL	Low-level output voltage	DOUT at $R_L = 3 \text{ k}\Omega$ to GND,	DIN = V <sub>CC</sub>	-5	-5.4		V
lιΗ	High-level input current	$V_I = V_{CC}$			±0.01	±1	μΑ
IլL	Low-level input current	V <sub>I</sub> at GND			±0.01	±1	μΑ
	Object along the standard access of	V <sub>CC</sub> = 3.6 V,	VO = 0 V		±35	±60	A
los	Short-circuit output current‡	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0 V		±35	±90	mA
r <sub>O</sub>	Output resistance	$V_{CC}$ , V+, and V- = 0 V,	$V_O = \pm 2 V$	300	10M		Ω
1	Output lookage ourrent	PWRDOWN = GND	$V_O = \pm 12 \text{ V},  V_{CC} = 3 \text{ V to } 3.6 \text{ V}$			±25	^
loff	Output leakage current	Output leakage current PWRDOWN = GND	$V_O = \pm 10 \text{ V},  V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			±25	μΑ

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

	PARAMETER	-	TEST CONDITIONS		TYP <sup>†</sup>	MAX	UNIT
Maximum data rate (see Figure 1)			C <sub>L</sub> = 1000 pF	250			
		$R_L = 3 k\Omega$ , One DOUT switching	$C_L = 250 \text{ pF}, \qquad V_{CC} = 3 \text{ V to } 4.5 \text{ V}$	1000			kbit/s
		One Boot switching	$C_L = 1000 \text{ pF}, \qquad V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1000			
t <sub>sk(p)</sub>	Pulse skew§	C <sub>L</sub> = 150 pF to 2500 pF	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$ See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	$R_L$ = 3 kΩ to 7 kΩ, $V_{CC}$ = 3.3 V	C <sub>L</sub> = 150 pF to 1000 pF	18		150	V/μs

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.



<sup>\$</sup> Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

<sup>§</sup> Pulse skew is defined as |tpLH - tpHL| of each channel of the same device.

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#### RECEIVER SECTION

#### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	I <sub>OH</sub> = −1 mA	V <sub>C</sub> C – 0.6 V	V <sub>CC</sub> – 0.1 V		V
VOL	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
\/-	Desitive main a input three held valte as	V <sub>CC</sub> = 3.3 V		1.5	2.4	.,
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5 V		1.8	2.4	V
.,	No well-resident format three should contract	V <sub>CC</sub> = 3.3 V	0.6	1.2		
V <sub>IT</sub> _	Negative-going input threshold voltage	V <sub>CC</sub> = 5 V	0.8	1.5		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.3		V
l <sub>off</sub>	Output leakage current	EN = V <sub>CC</sub>		±0.05	±10	μΑ
rį	Input resistance	$V_I = \pm 3 \text{ V to } \pm 25 \text{ V}$	3	5	7	kΩ

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V ± 0.5 V.

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

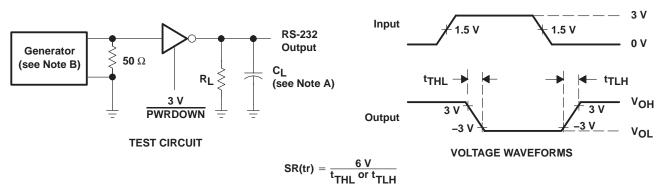
	PARAMETER	TEST CONDITIONS	MIN TYP <sup>†</sup> MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	$C_{L} = 150 \text{ pF}$ , See Figure 3	300	ns
tPHL	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See Figure 3	300	ns
t <sub>en</sub>	Output enable time	$C_L$ = 150 pF, $R_L$ = 3 kΩ, See Figure 4	200	ns
<sup>t</sup> dis	Output disable time	$C_L$ = 150 pF, $R_L$ = 3 kΩ, See Figure 4	200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>‡</sup>	See Figure 3	300	ns

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

‡ Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device. NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC}$  = 3.3 V ± 0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at  $V_{CC}$  = 5 V ± 0.5 V.



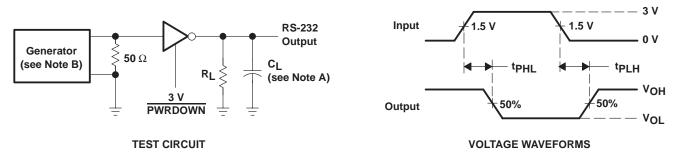
#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \le 10$  ns.  $t_f \le 10$  ns.

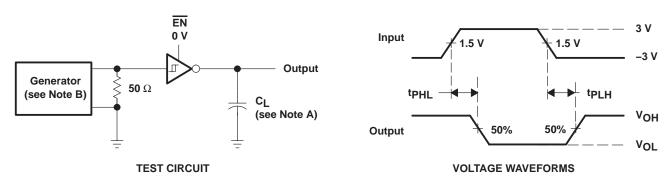
Figure 1. Driver Slew Rate



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_f \le 10$  ns.  $t_f \le 10$  ns.

Figure 2. Driver Pulse Skew



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

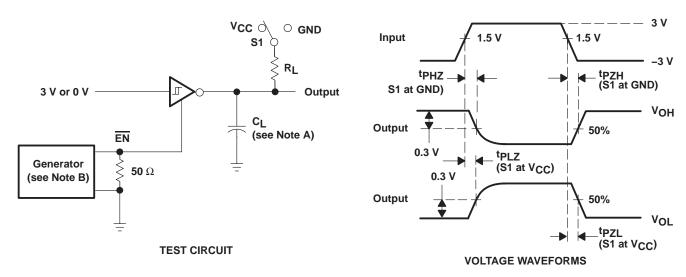
B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \le 10$  ns,  $t_f \le 10$  ns.

Figure 3. Receiver Propagation-Delay Times



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#### PARAMETER MEASUREMENT INFORMATION



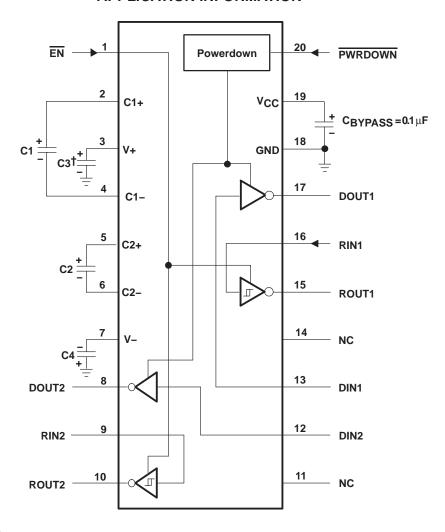
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50 \ \Omega$ , 50% duty cycle,  $t_\Gamma \le 10 \ ns$ ,  $t_f \le 10 \ ns$ .

Figure 4. Receiver Enable and Disable Times



#### **APPLICATION INFORMATION**



†C3 can be connected to VCC or GND.

NOTES: A. Resistor values shown are nominal.

B. NC - No internal connection

#### V<sub>CC</sub> vs CAPACITOR VALUES

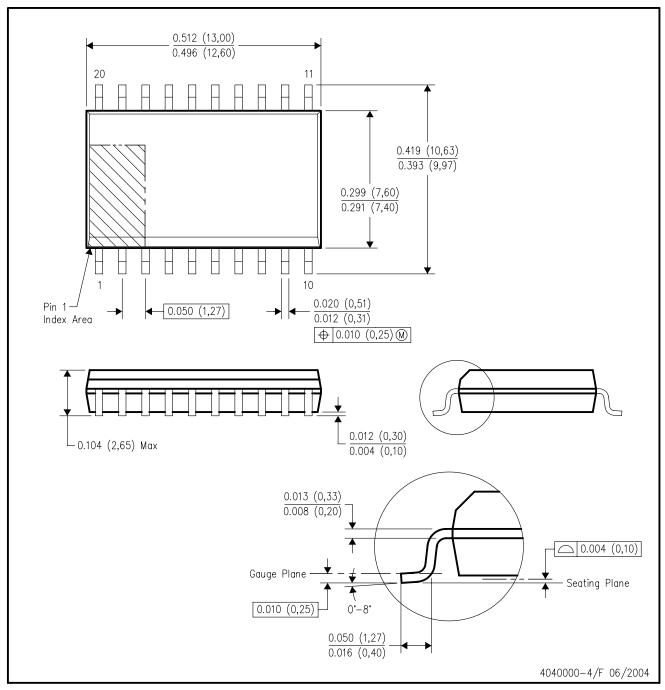
VCC	C1	C2, C3, and C4
3.3 V $\pm$ 0.3 V	<b>0.1</b> μ <b>F</b>	<b>0.1</b> μ <b>F</b>
5 V ± 0.5 V	<b>0.047</b> μ <b>F</b>	<b>0.33</b> μF
3 V to 5.5 V	<b>0.1</b> μ <b>F</b>	<b>0.47</b> μ <b>F</b>

Figure 5. Typical Operating Circuit and Capacitor Values



# DW (R-PDSO-G20)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

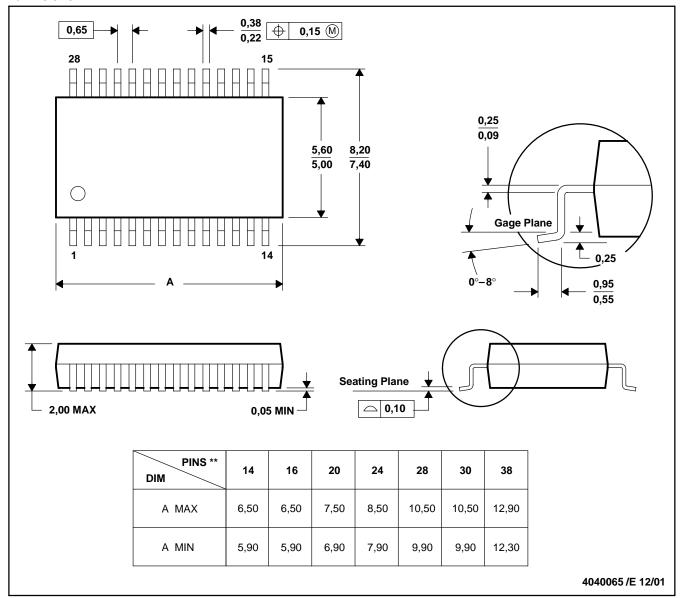
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



## DB (R-PDSO-G\*\*)

#### **PLASTIC SMALL-OUTLINE**

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



## PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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