# 5-V FULL-DUPLEX RS-485/RS-422 DRIVER AND BALANCED RECEIVER

## FEATURES

- **Designed for INTERBUS Applications**
- **Balanced Receiver Thresholds**
- **1/2 Unit-Load (up to 64 nodes on the bus)**
- **Bus-Pin ESD Protection 15 kV HBM**
- **Bus-Fault Protection of –7V to 12V**
- **Thermal Shutdown Protection**
- **Power-Up/Down Glitch-free Bus Inputs and Outputs**

## APPLICATIONS

- **Digital Motor Control**
- **Utility Meters**
- **Chassis-to-Chassis Interconnections**
- **Electronic Security Stations**
- **Industrial, Process, and Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**
- **DTE/DCE Interfaces**

## DESCRIPTION

The SN65HVD179 is a differential line driver and differential-input line receiver that operates with a 5-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

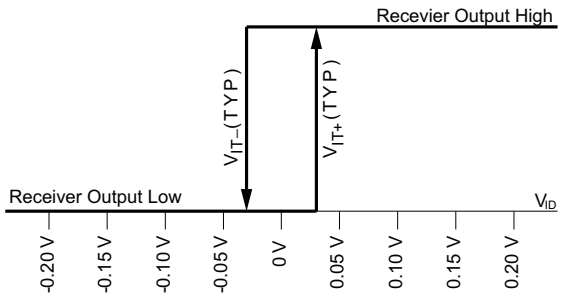
The differential bus driver and receiver are monolithic, integrated circuits designed for full-duplex bi-directional data communication on multipoint bus-transmission lines at signaling rates(1) up to 25 Mbps. The SN65HVD179 is fully enabled with no external enabling pins.

The 1/2 unit load receiver has a high receiver input resistance. This results in lower bus leakage currents over the common-mode voltage range, and reduces the total amount of current that a 485 driver is forced to source or sink when transmitting.

The balanced differential receiver input threshold makes the SN65HVD179 fully compatible with fieldbus requirements that define an external failsafe structure.

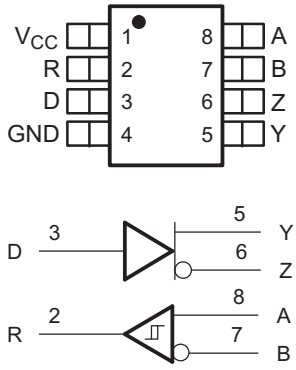
(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

**BALANCED RECEIVER INPUT THRESHOLDS**




**SN65HVD179**

D PACKAGE (TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| SIGNALING RATE | UNIT LOADS | BASE PART NUMBER | SOIC MARKING |
|---|---|---|---|
| 25 Mbps | 1/2 | SN65HVD179 | SN65HVD179 |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | UNIT |
|---|---|---|
| $V_{CC}$ | Supply voltage range | –0.3 V to 6 V |
| $V_A$, $V_B$, $V_Y$, $V_Z$ | Voltage range at any bus terminal (A, B, Y, Z) | –9 V to 14 V |
| $V_{TRANS}$ | Voltage input, transient pulse through 100 Ω. See Figure 8 (A, B, Y, Z)(3) | –50 to 50 V |
| $V_I$ | Voltage input range (D, DE, $\overline{RE}$) | –0.5 V to 7 V |
| $P_{CONT}$ | Continuous total power dissipation | Internally limited(4) |
| $I_O$ | Output current (receiver output only, R) | 11 mA |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) This tests survivability only and the output state of the receiver is not specified.
(4) The Thermal shutdown of this device internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | | 5.5 | V |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common mode) | | –7(1) | | 12 | |
| $1/t_{UI}$ | Signaling rate | | | | 25 | Mbps |
| $R_L$ | Differential load resistance | | 54 | 60 | | Ω |
| $V_{IH}$ | High-level input voltage | D | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | D | 0 | | 0.8 | |
| $V_{ID}$ | Differential input voltage | | –12 | | 12 | |
| $I_{OH}$ | High-level output current | Driver | –60 | | | mA |
| | | Receiver | –8 | | | |
| $I_{OL}$ | Low-level output current | Driver | | | 60 | mA |
| | | Receiver | | | 8 | |
| $T_J$ | Junction temperature(2) | | –40 | | 150 | °C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) See thermal characteristics table for information regarding this specification.

## ELECTROSTATIC DISCHARGE PROTECTION

| PARAMETER | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| Human body model | Bus terminals and GND | | ±16 | | kV |
| Human body model(2) | All pins | | ±4 | | |
| Charged-device-model(3) | All pins | | ±1 | | |

(1) All typical values at 25°C and with a 5-V supply.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{I(K)}$ | Input clamp voltage | | $I_I$ = –18 mA | | –1.5 | | | V |
| $\|V_{OD(SS)}\|$ | Steady-state differential output voltage | | $I_O$ = 0 | | 4 | | $V_{CC}$ | V |
| | | | $R_L$ = 54 Ω, See Figure 1 (RS-485) | | 1.7 | 2.6 | | V |
| | | | $R_L$ = 100 Ω, See Figure 1 (RS-422) | | 2.4 | 3.2 | | V |
| | | | $V_{test}$ = –7 V to 12 V, See Figure 2 | | 1.6 | | | V |
| $\Delta\|V_{OD(SS)}\|$ | Change in magnitude of steady-state differential output voltage between states | | $R_L$ = 54 Ω, See Figure 1 and Figure 2 | | –0.2 | | 0.2 | V |
| $V_{OD(RING)}$ | Differential Output Voltage overshoot and undershoot | | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 5 and Figure 3 for definition | | | | 10(2) | % |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | See Figure 4 | | | 0.5 | | V |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | | See Figure 4 | | 2.2 | | 3.3 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage | | See Figure 4 | | –0.1 | | 0.1 | V |
| $I_{Z(Z)}$ or $I_{Y(Z)}$ | High-impedance state output current | | $V_{CC}$ = 0 V, $V_Z$ or $V_Y$ = 12 V, Other input at 0 V | | | | 90 | µA |
| | | | $V_{CC}$ = 0 V, $V_Z$ or $V_Y$ = –7 V, Other input at 0 V | | –10 | | | µA |
| $I_{Z(S)}$ or $I_{Y(S)}$ | Short Circuit output Current | | $V_Z$ or $V_Y$ = –7 V | Other input at 0 V | –250 | | 250 | mA |
| | | | $V_Z$ or $V_Y$ = 12 V | Other input at 0 V | –250 | | 250 | mA |
| $I_I$ | Input current | $V_I$ = 0, $V_I$ = 2.0 | | | 0 | | 100 | µA |
| $C_{(OD)}$ | Differential output capacitance | | | | | 16 | | pF |

(1) All typical values are at 25°C and with a 5-V supply.
(2) 10% of the peak-to-peak Differential Output voltage swing, per TIA/EIA-485.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 5 | 4 | 8 | 12 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 5 | 4 | 8 | 12 | ns |
| $t_r$ | Differential output signal rise time | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 5 | 3 | 6 | 12 | ns |
| $t_f$ | Differential output signal fall time | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 5 | 3 | 6 | 12 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} - t_{PLH}\|$) | | | 1.4 | | ns |
| $t_{sk(pp)}$(2) | Part-to-part skew | | | 1 | | ns |

(1) All typical values are at 25°C and with a 5-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input threshold voltage | $I_O$ = –8 mA | | | | 0.2 | V |
| $V_{IT–}$ | Negative-going differential input threshold voltage | $I_O$ = 8 mA | | –0.2 | | | |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+}$– $V_{IT–}$) | | | | 50 | | mV |
| $V_O$ | Output voltage | $V_{ID}$ = 200 mV, $I_O$ = –8 mA, See Figure 6 | | 4.0 | | | V |
| | | $V_{ID}$ = –200 mV, $I_O$ = 8 mA, See Figure 6 | | | | 0.3 | |
| $I_A$ or $I_B$ | Bus input current | $V_A$ or $V_B$ = 12 V | Other input at 0 V | | 0.20 | 0.3 | mA |
| | | $V_A$ or $V_B$ = 12 V, $V_{CC}$ = 0 V | | | 0.24 | 0.4 | |
| | | $V_A$ or $V_B$ = –7 V | | –0.35 | –0.19 | | |
| | | $V_A$ or $V_B$ = –7 V, $V_{CC}$ = 0 V | | –0.25 | –0.14 | | |
| $I_{CC}$ | Supply current | D at 0 V or $V_{CC}$ and No Load | | | | 2.7 | mA |

(1) All typical values are at 25°C and with a 5-V supply.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $V_I$ = 0 V to 3 V, $C_L$ = 15 pF, See Figure 7 | | 24 | 40 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | | |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} - t_{PLH}\|$) | | | | 5 | |
| $t_{sk(pp)}$(2) | Part-to-part skew | | | 5 | | ns |
| $t_r$ | Output signal rise time | $C_L$ = 15 pF, See Figure 7 | | 2 | 4 | ns |
| $t_f$ | Output signal fall time | | | 2 | 4 | ns |

(1) All typical values are at 25°C and with a 5-V supply

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## THERMAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | Low-K board(3), No airflow | | 230.8 | | °C/W |
| | | High-K board(4), No airflow | | 135.1 | | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | High-K board | | 44.4 | | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance | No board | | 43.5 | | °C/W |
| $P_D$ | Device power dissipation | $R_L$= 60 Ω, $C_L$ = 50 pF, Input to D a 50% duty cycle square wave at indicated signaling rate | | | 420 | mW |
| $T_A$ | Ambient air temperature | Low-K board, No airflow | –40 | | 55 | °C |
| | | High-K board, No airflow | –40 | | 85 | |
| $T_{JSD}$ | Thermal shutdown junction temperature | | | 165 | | °C |

(1) See *Application Information* section for an explanation of these parameters.
(2) The intent of $\theta_{JA}$ specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(3) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(4) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

## PARAMETER MEASUREMENT INFORMATION

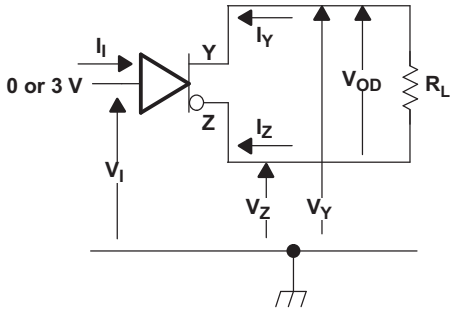



**Figure 1. Driver $V_{OD}$ Test Circuit: Voltage and Current Definitions**

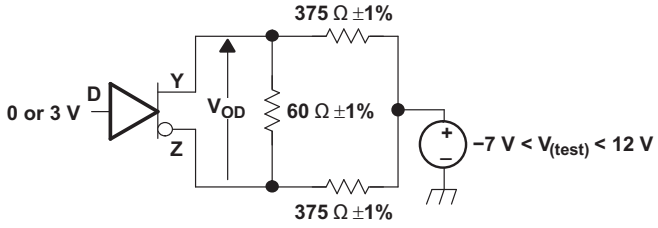



**Figure 2. Driver $V_{OD}$ With Common-Mode Loading Test Circuit**

VOD(RING) is measured at four points on the output waveform, corresponding to overshoot and undershoot from theVOD(H) and VOD(L) steady state values.

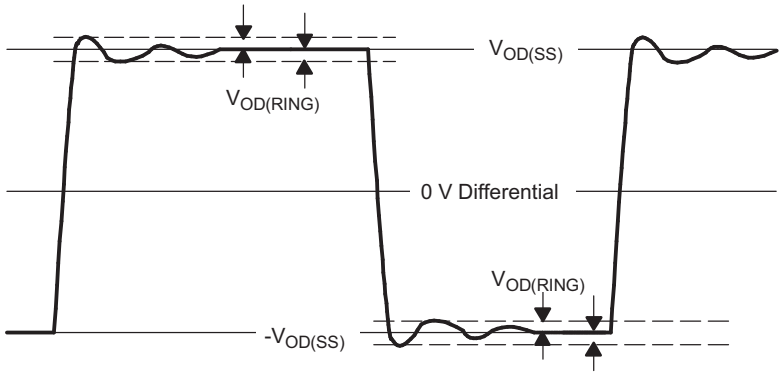
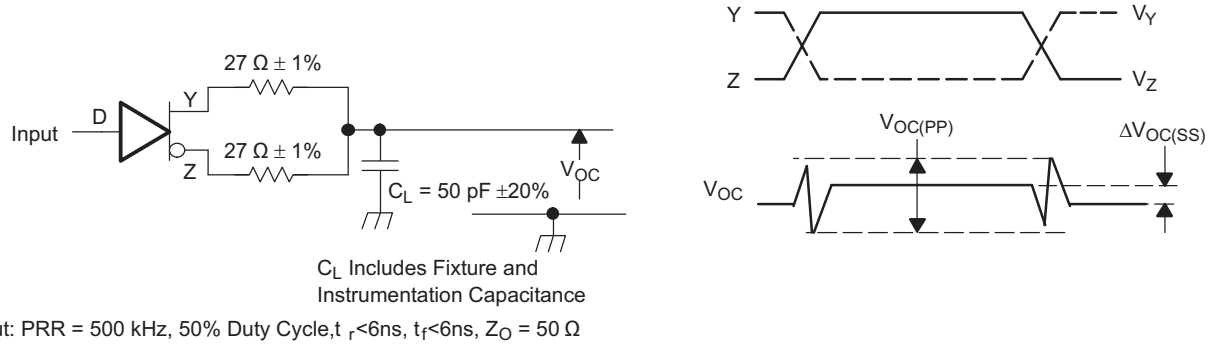


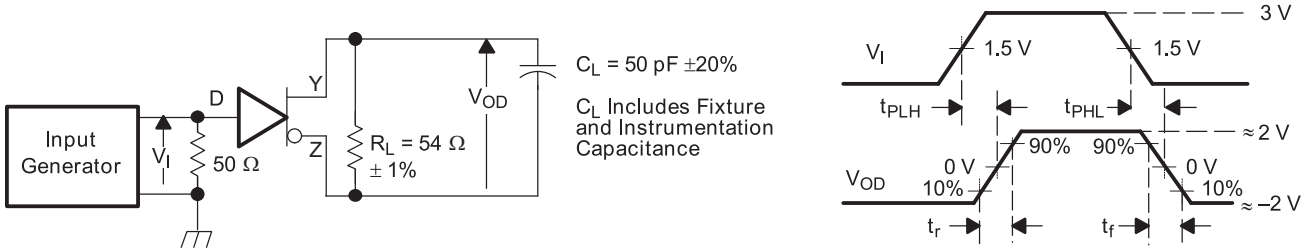

**Figure 3. $V_{OD(RING)}$ Waveform and Definitions**

## PARAMETER MEASUREMENT INFORMATION (continued)




Input: PRR = 500 kHz, 50% Duty Cycle,$t_r$<6ns, $t_f$<6ns, $Z_O$ = 50 Ω

**Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**




Generator: PRR = 500 kHz, 50% Duty Cycle, $t_r$ <6 ns, $t_f$ <6 ns, $Z_o$ = 50 Ω

**Figure 5. Driver Switching Test Circuit and Voltage Waveforms**

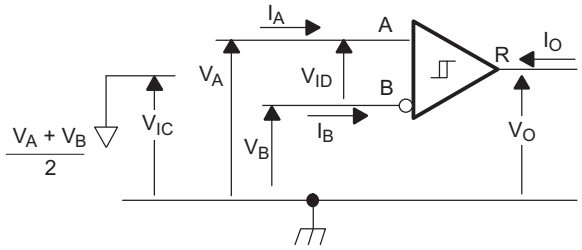



**Figure 6. Receiver Voltage and Current Definitions**

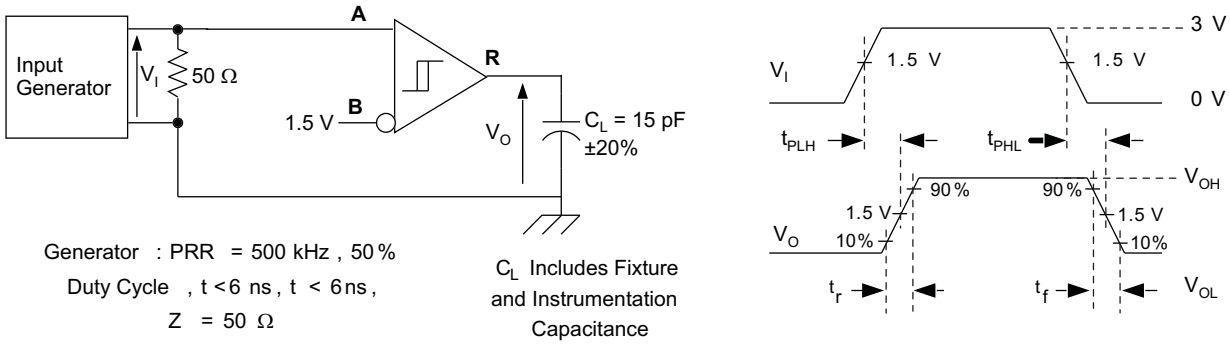



**Figure 7. Receiver Switching Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)

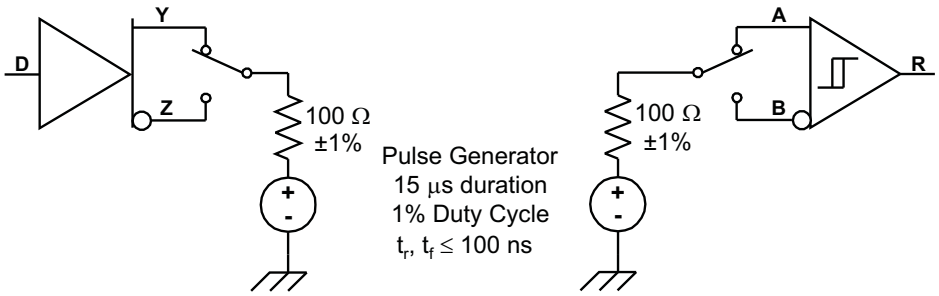
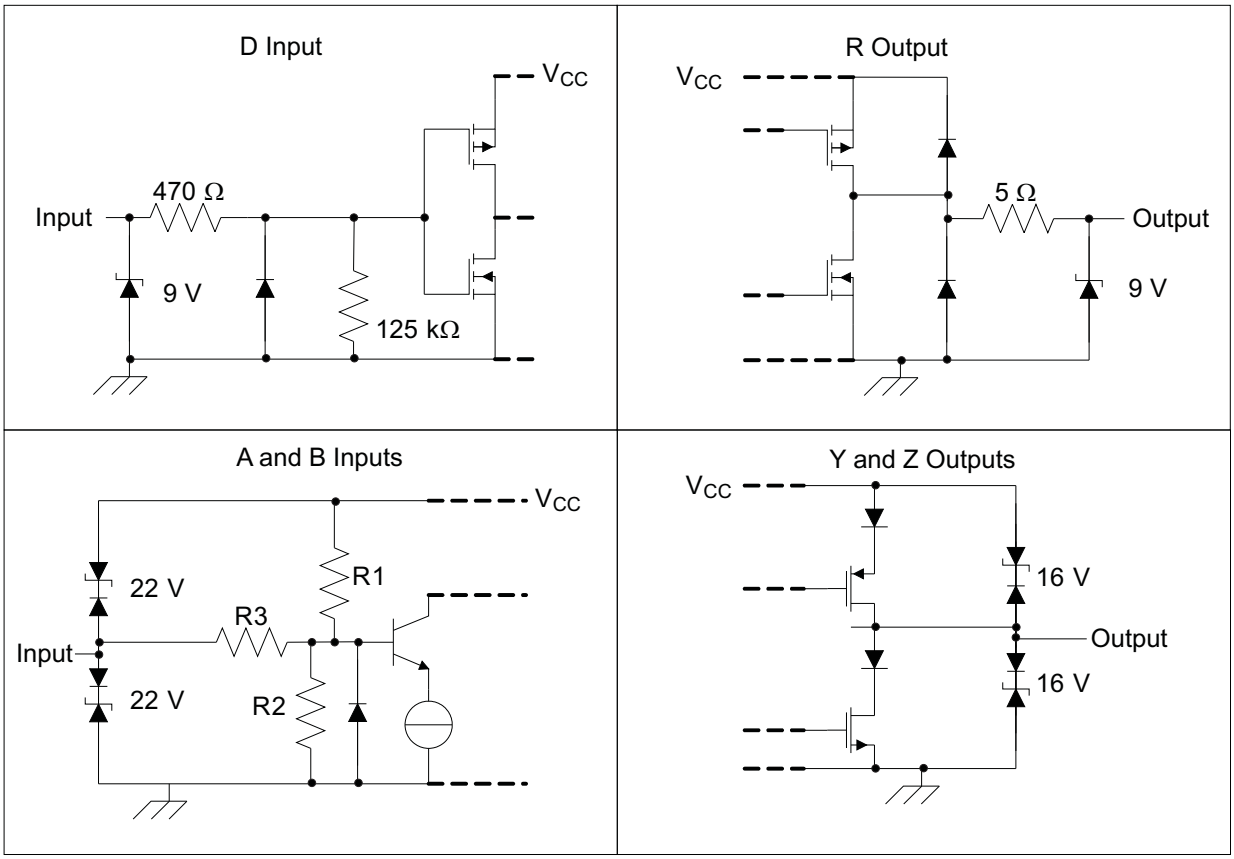



**Figure 8. Test Circuit, Transient Overvoltage Test**

## FUNCTION TABLES

| DRIVER | | | RECEIVER | |
|---|---|---|---|---|
| **INPUT** | **OUTPUTS** | | **DIFFERENTIAL INPUTS** | **OUTPUTS** |
| **D** | **Y** | **Z** | **$V_{ID} = V_A - V_B$** | **R** |
| H | H | L | $V_{ID} \leq -0.2$ V | L |
| L | L | H | $-0.2$ V < $V_{ID}$ < 0.2 V | ? |
| Open | L | H | 0.2 V ≤ $V_{ID}$ | H |

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS




| | R1/R2 | R3 |
|---|---|---|
| SN65HVD179 | 9 kΩ | 45 kΩ |

## TYPICAL CHARACTERISTICS

**RMS SUPPLY CURRENT vs SIGNALING RATE**

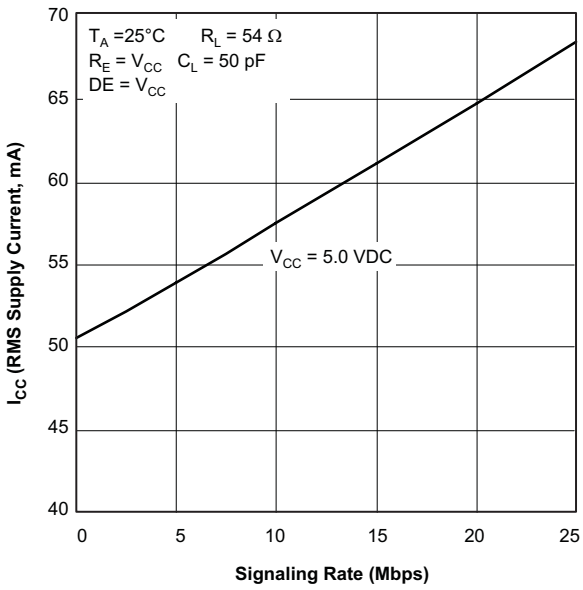



**Figure 9.**

**BUS INPUT CURRENT vs INPUT VOLTAGE**

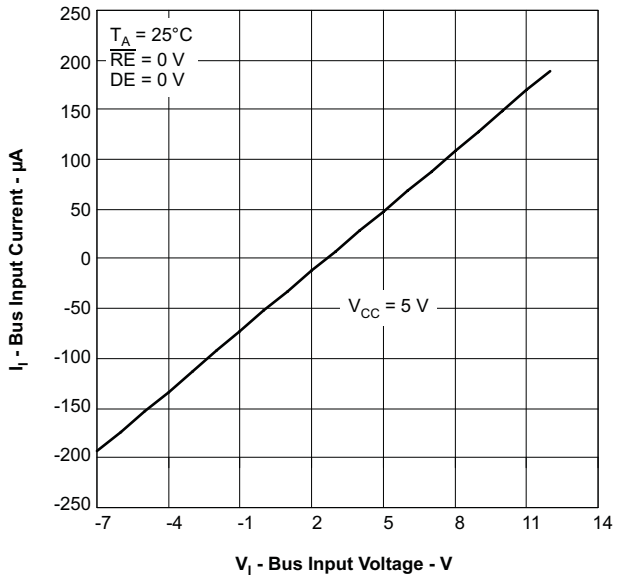



**Figure 10.**

**DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

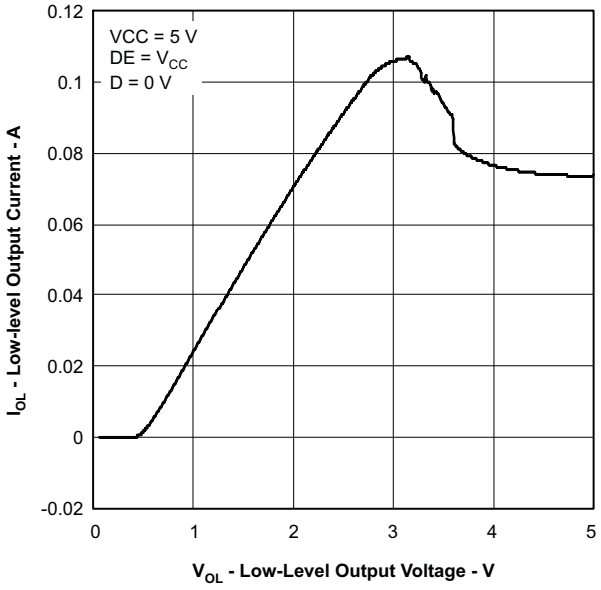



**Figure 11.**

## TYPICAL CHARACTERISTICS (continued)

**DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

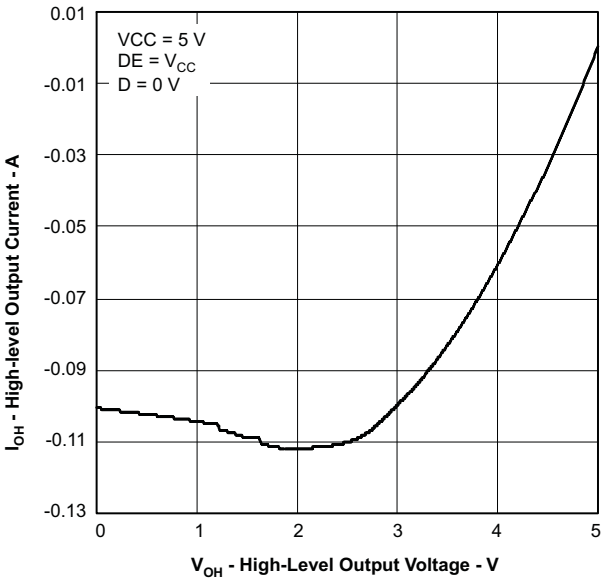



**Figure 12.**

**DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

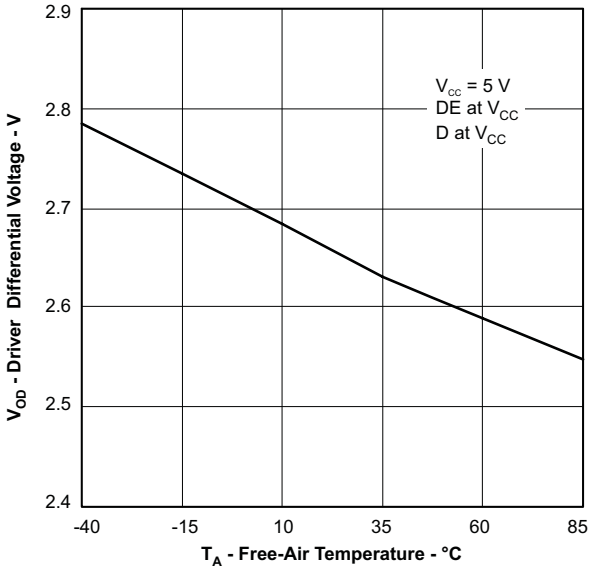



**Figure 13.**

**DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE**

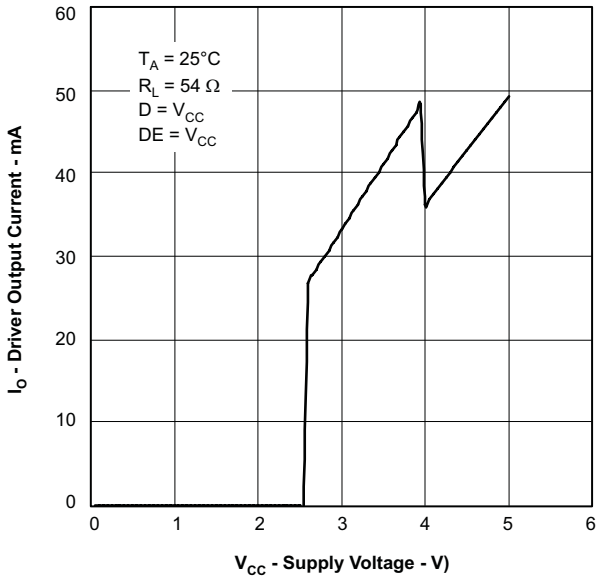



**Figure 14.**

## APPLICATION INFORMATION

### THERMAL CHARACTERISTICS OF IC PACKAGES

$\theta_{JA}$ **(Junction-to-Ambient Thermal Resistance)** is defined as the difference in junction temperature to ambient temperature divided by the operating power.

$\theta_{JA}$ is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$\theta_{JA}$ can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. $\theta_{JA}$ is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-K board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-K board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in $\theta_{JA}$ can be measured between these two test cards

$\theta_{JC}$ **(Junction-to-Case Thermal Resistance)** is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$\theta_{JC}$ is a useful thermal characteristic when a heatsink applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with $\theta_{JB}$ in 1-dimensional thermal simulation of a package system.

$\theta_{JB}$ **(Junction-to-Board Thermal Resistance)** is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. $\theta_{JB}$ is only defined for the high-K test card.

$\theta_{JB}$ provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see Figure 15.

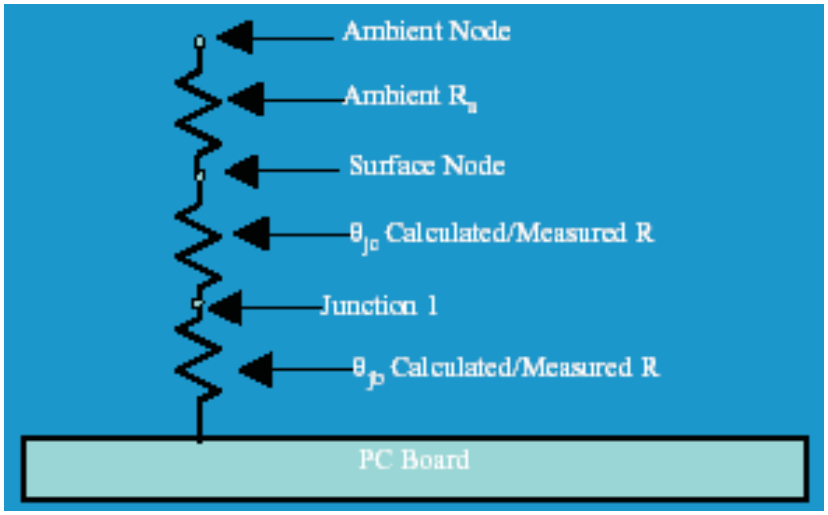



**Figure 15. Thermal Resistance**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN65HVD179D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65HVD179DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65HVD179DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65HVD179DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

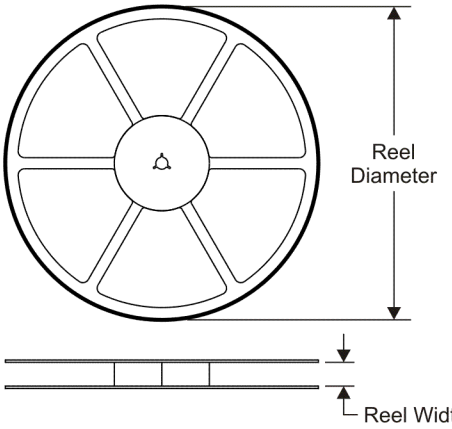
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

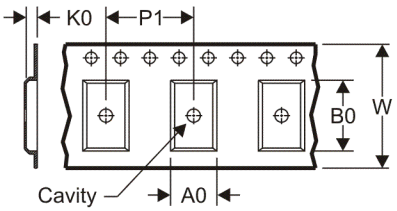
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

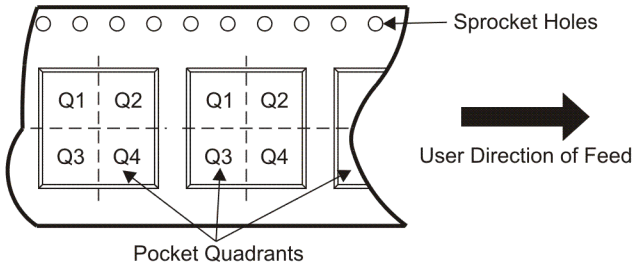



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

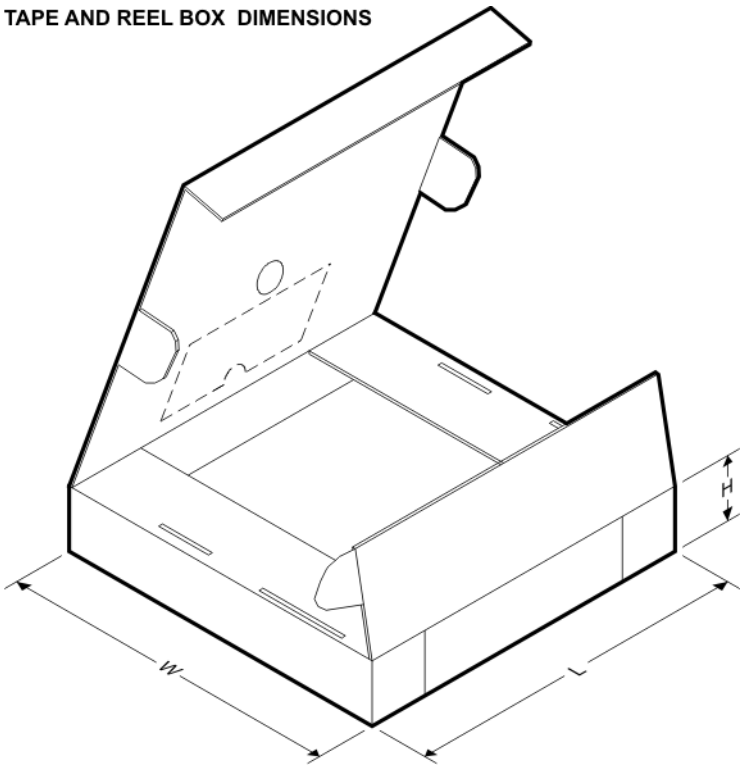
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD179DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

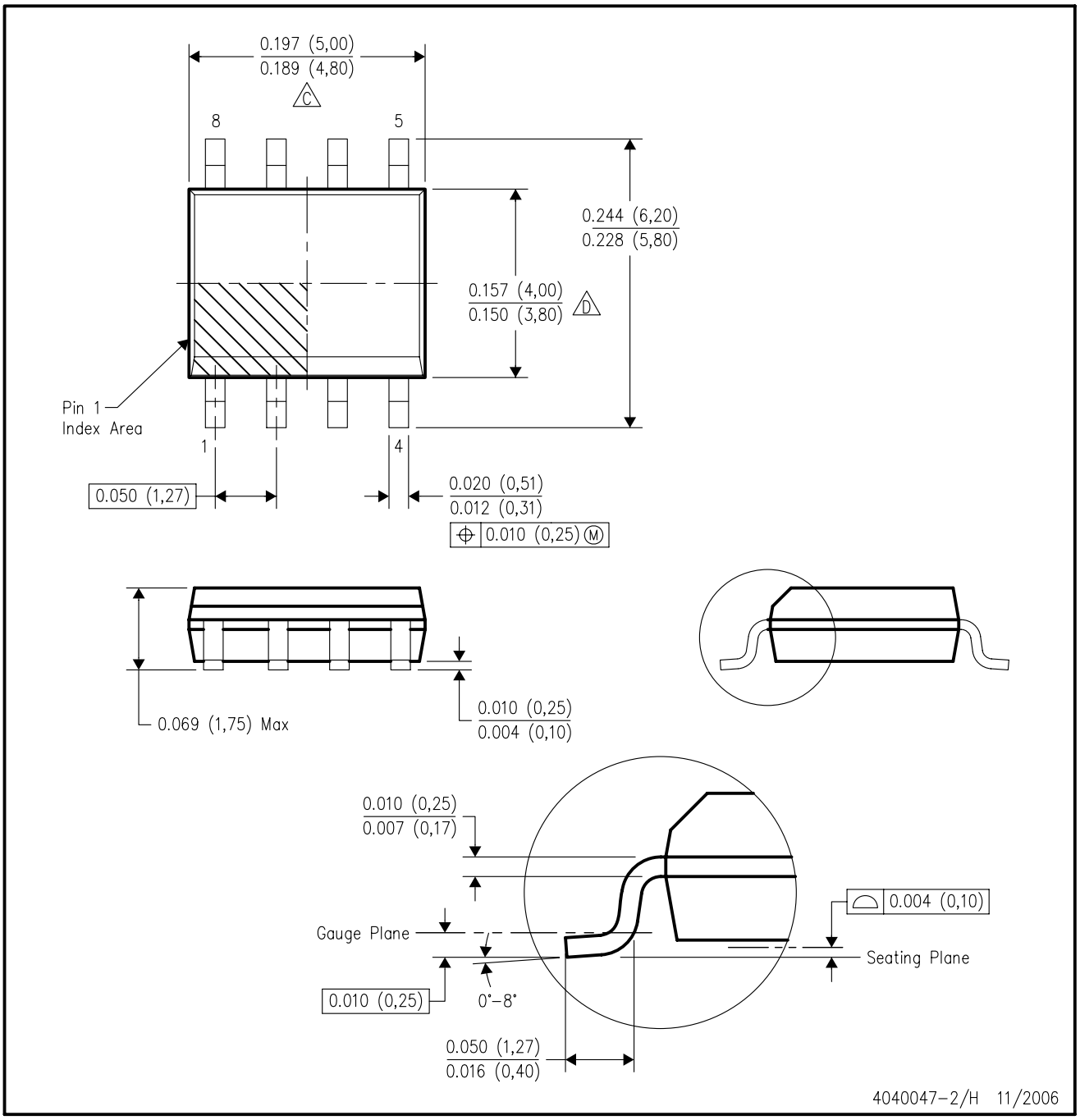
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVD179DR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

## D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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