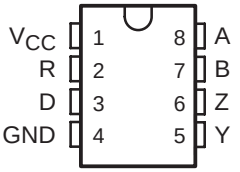
- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Operates With Pulse Widths as Low as 30 ns**
- **Low Supply Current . . . 5 mA Max**
- **Meets or Exceeds the Standard Requirements of ANSI RS-485 and ISO 8482:1987(E)**
- **Common-Mode Voltage Range of −7 V to 12 V**
- **Positive- and Negative-Output Current Limiting**
- **Driver Thermal Shutdown Protection**
- **Pin Compatible With the SN75179B**

description

The SN65LBC179, SN65LBC179Q, and SN75LBC179 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). Both devices are designed using TI's proprietary LinBiCMOS™ with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

The SN65LBC179, SN65LBC179Q, and SN75LBC179 combine a differential line driver and differential line receiver and operate from a single 5-V supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off (V_{CC} = 0). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

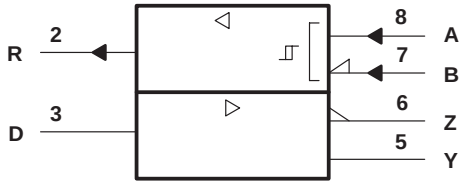
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A−B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V < V_{ID} < 0.2 V	?
$V_{ID} \leq -0.2$ V	L
Open circuit	H

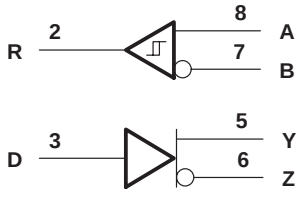
H = high level, L = low level,
? = indeterminate

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

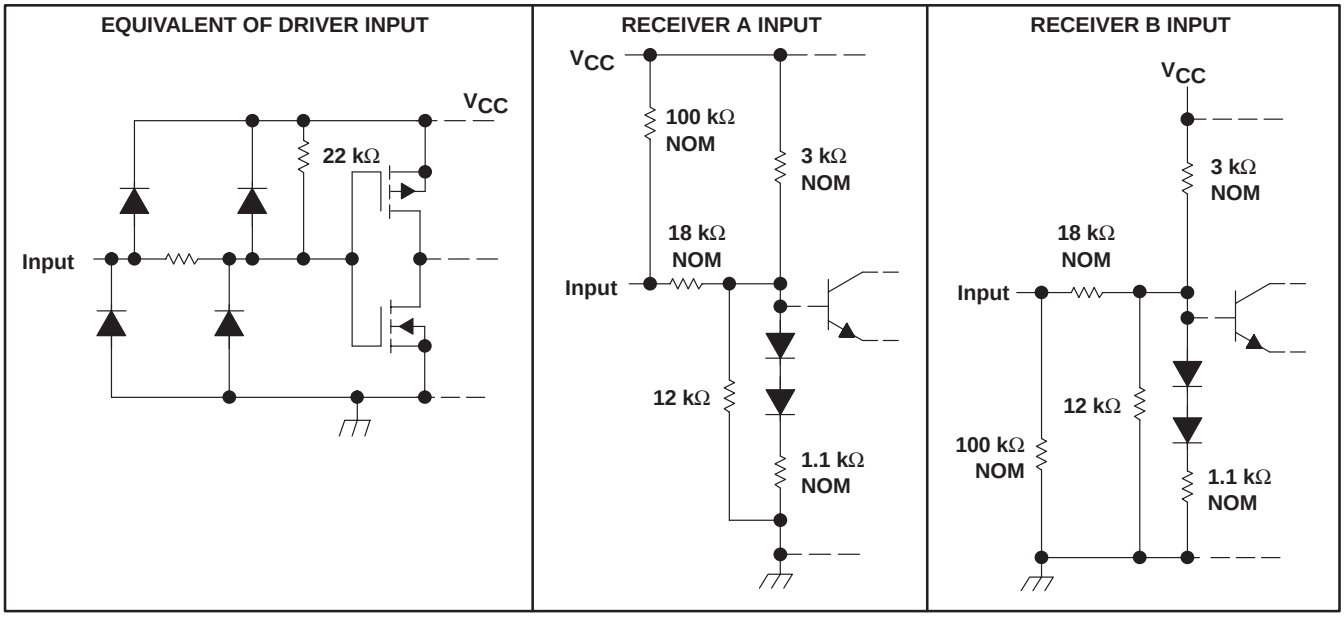
logic diagram (positive logic)

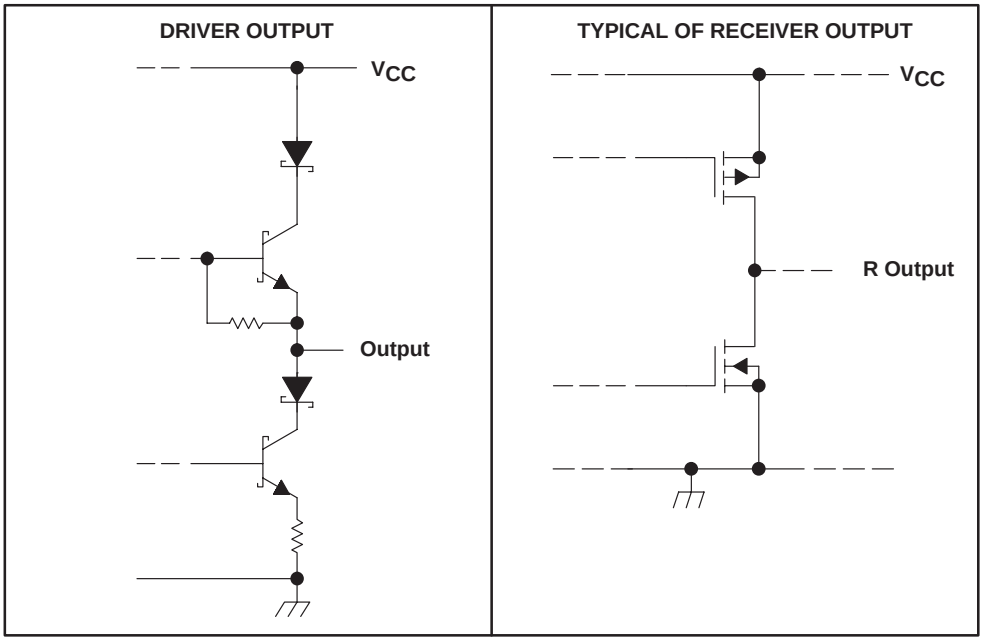


description (continued)

The SN65LBC179, SN65LBC179Q, and SN75LBC179 are available in the 8-pin dual-in-line and small-outline packages. The SN75LBC179 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC179 is characterized over the industrial temperature range of −40°C to 85°C. The SN65LBC179Q is characterized over the extended industrial or automotive temperature range of −40°C to 125°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.3 V to 7 V
Voltage range at A, B, Y, or Z (see Note 1) . . . . . −10 V to 15 V
Voltage range at D or R (see Note 1) . . . . . −0.3 V to V_{CC} + 0.5 V
Receiver output current, I_O . . . . . ±10 mA
Continuous total power dissipation (see Note 2) . . . . . Internally limited
Total power dissipation . . . . . See Dissipation Rating Table

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1100 mW	8.8 mW/°C	704 mW	572 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D	2			V
Low-level input voltage, V_{IL}	D			0.8	V
Differential input voltage, V_{ID}		−6‡		6	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	A, B, Y, or Z	−7		12	V
High-level output current, I_{OH}	Y or Z			−60	mA
	R			−8	
Low-level output current, I_{OL}	Y or Z			60	mA
	R			8	
Operating free-air temperature, T_A	SN65LBC179	−40		85	°C
	SN65LBC179Q	−40		125	
	SN75LBC179	0		70	

‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for differential input voltage, voltage at any bus terminal (separately or common mode), operating temperature, input threshold voltage, and common-mode output voltage.

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\|V_{OD}\|$	Differential output voltage (see Note 3)	R_L = 54 Ω, See Figure 1	SN65LBC179, SN65LBC179Q	1.1	2.2	5	V
			SN75LBC179	1.5	2.2	5	
		R_L = 60 Ω, See Figure 2	SN65LBC179, SN65LBC179Q	1.1	2.2	5	
			SN75LBC179	1.5	2.2	5	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 4)	See Figures 1 and 2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω, See Figure 1		1	2.5	3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	No load	SN65LBC179, SN75LBC179		4.2	5	mA
			SN65LBC179Q		4.2	7	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 3. The minimum V_{OD} specification of the SN65179 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, See Figure 3		7	18	ns
$t_{t(OD)}$	Differential transition time			5	20	ns

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = −8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OL} = 8 mA			0.3	0.5	V
I_I	Bus input current	V_I = 12 V, Other inputs at 0 V, V_{CC} = 5 V	SN65LBC179, SN75LBC179		0.7	1	mA
			SN65LBC179Q		0.7	1.2	mA
		V_I = 12 V, Other inputs at 0 V, V_{CC} = 0 V	SN65LBC179, SN75LBC179		0.8	1	mA
			SN65LBC179Q		0.8	1.2	mA
		V_I = −7 V, Other inputs at 0 V, V_{CC} = 5 V	SN65LBC179, SN75LBC179		−0.5	−0.8	mA
			SN65LBC179Q		−0.5	−1.0	mA
		V_I = −7 V, Other inputs at 0 V, V_{CC} = 0 V	SN65LBC179, SN75LBC179		−0.5	−0.8	mA
			SN65LBC179Q		−0.5	−1.0	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 4	15		30	ns
t_{PLH}	Propagation delay time, low- to high-level output		15		30	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	See Figure 4		3	6	ns
t_t	Transition time			3	5	ns

PARAMETER MEASUREMENT INFORMATION

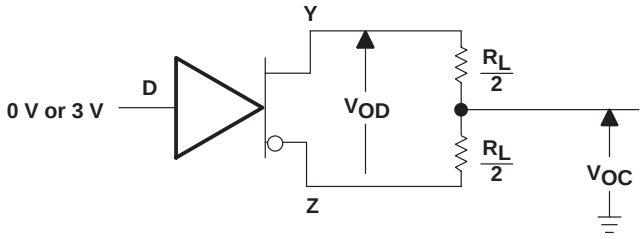


Figure 1. Differential and Common-Mode Output Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION

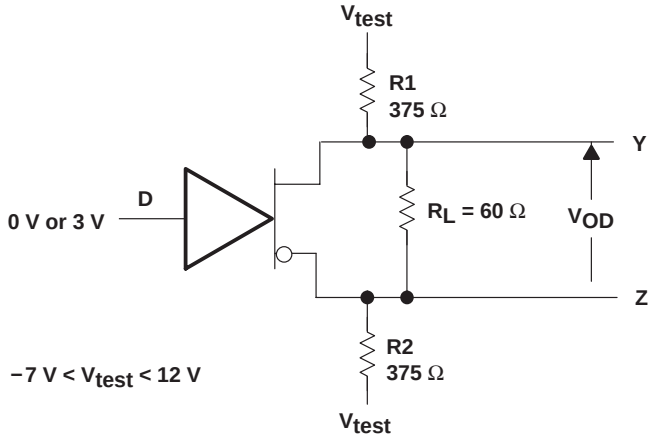
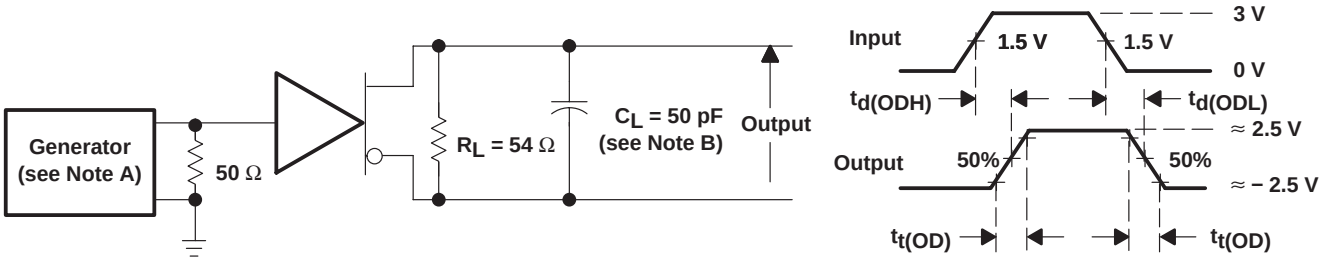
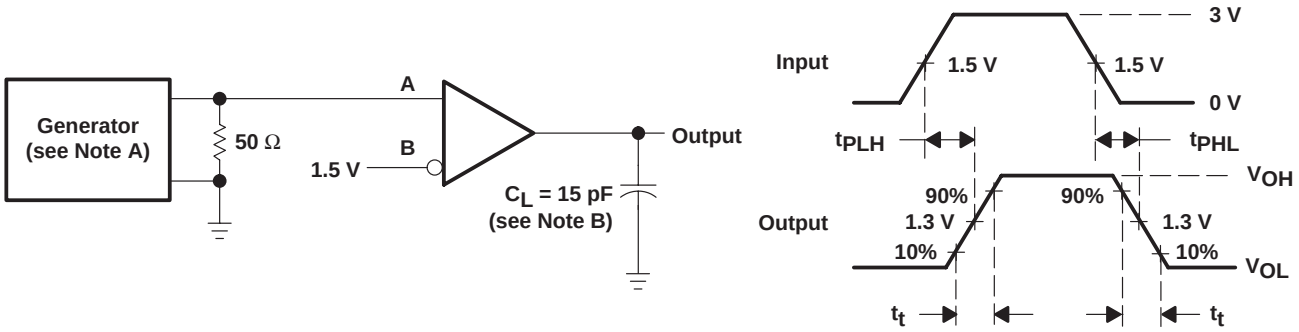


Figure 2. Differential Output Voltage Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuits and Differential Output Delay and Transition Time Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Receiver Test Circuit and Propagation Delay and Transition Time Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

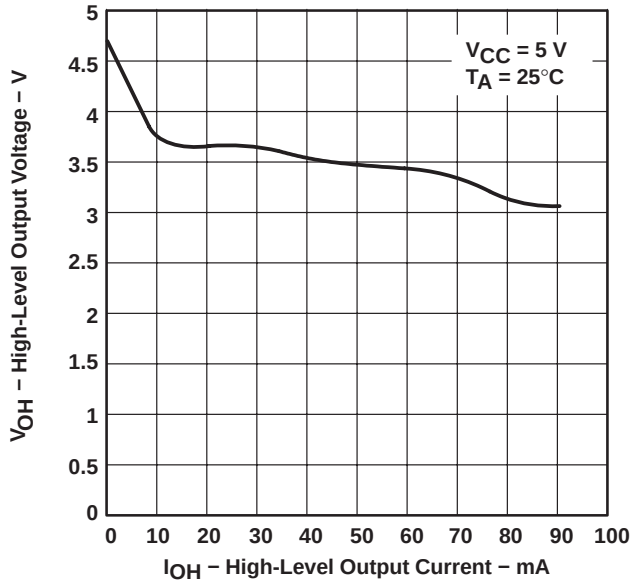


Figure 5

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

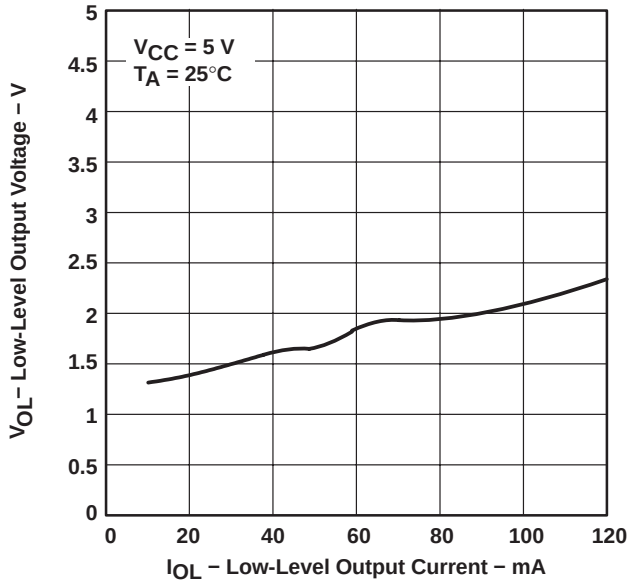


Figure 6

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

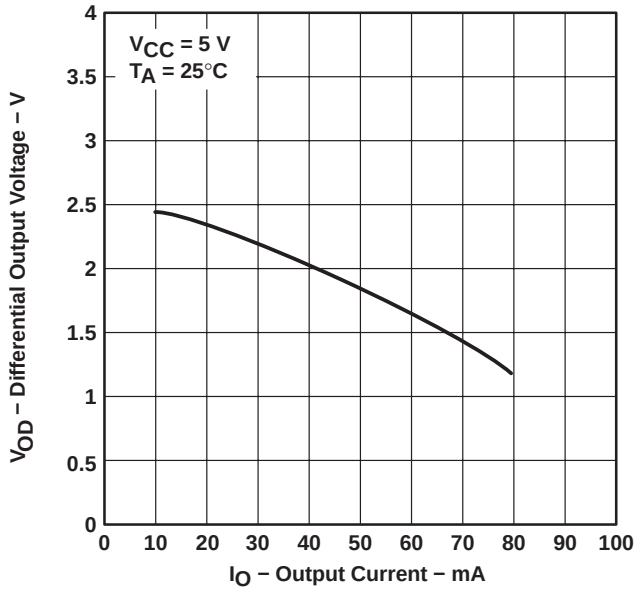


Figure 7

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

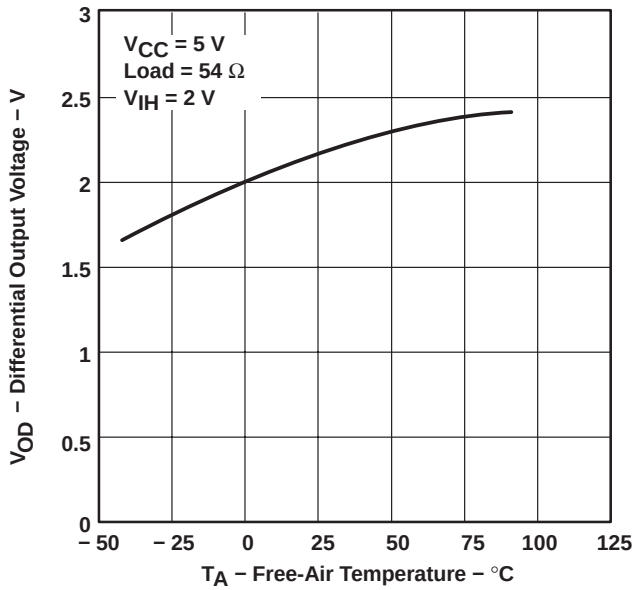


Figure 8

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL DELAY TIME
vs
FREE-AIR TEMPERATURE

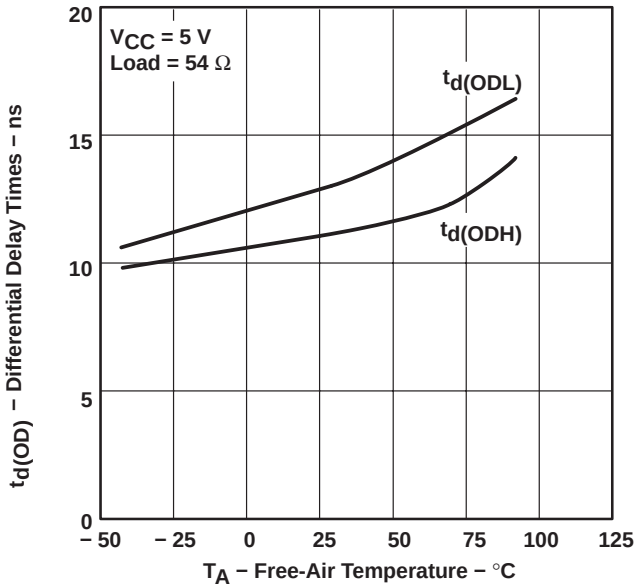


Figure 9

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

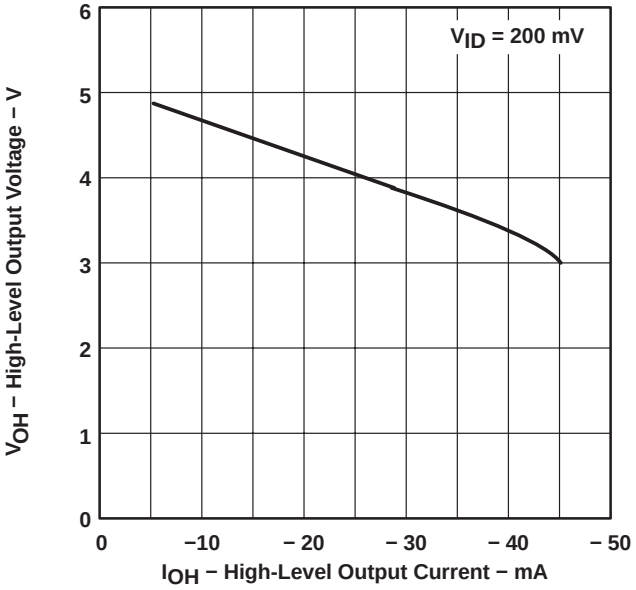


Figure 10

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

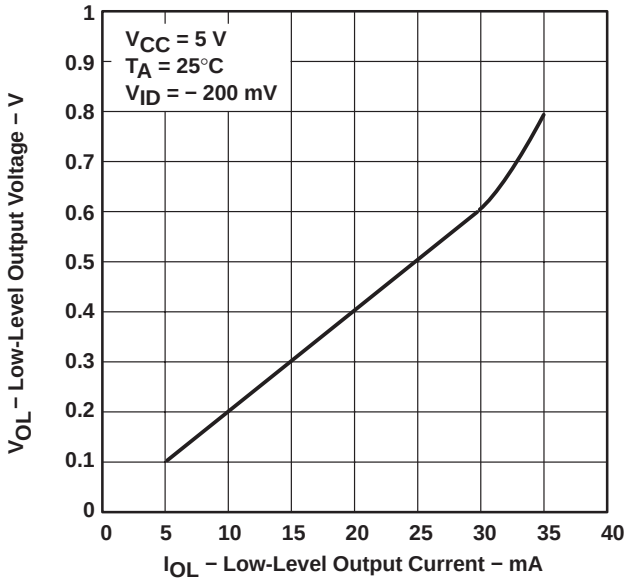


Figure 11

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

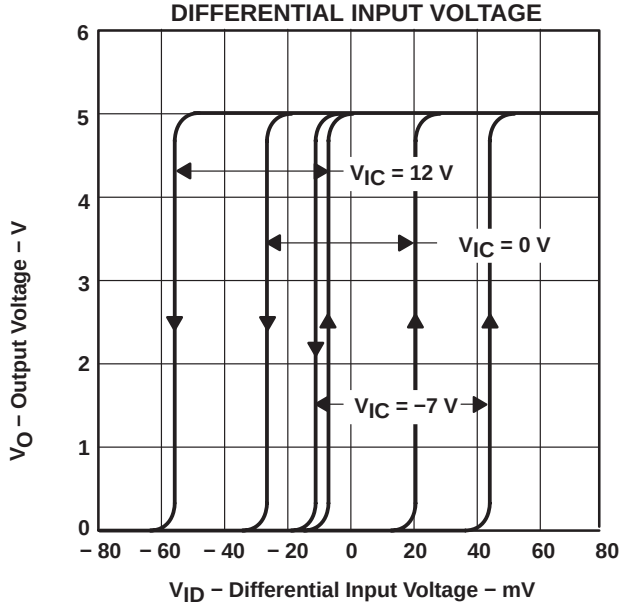


Figure 12

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT vs FREQUENCY

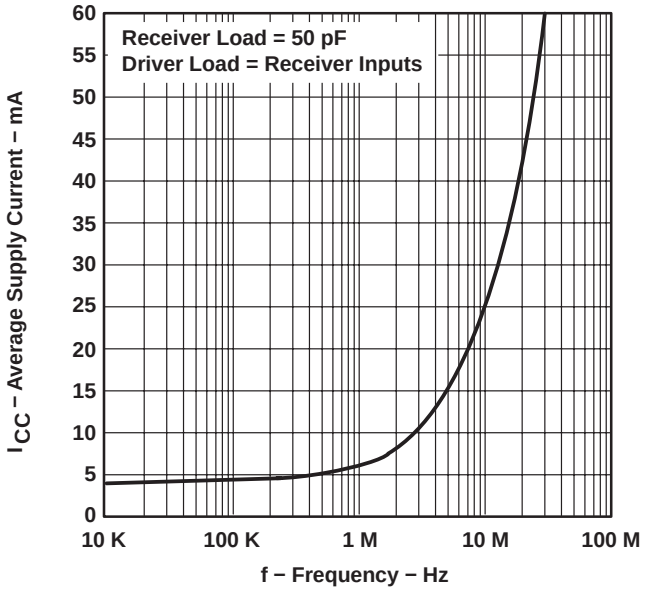


Figure 13

RECEIVER INPUT CURRENT vs INPUT VOLTAGE (COMPLEMENTARY INPUT AT 0 V)

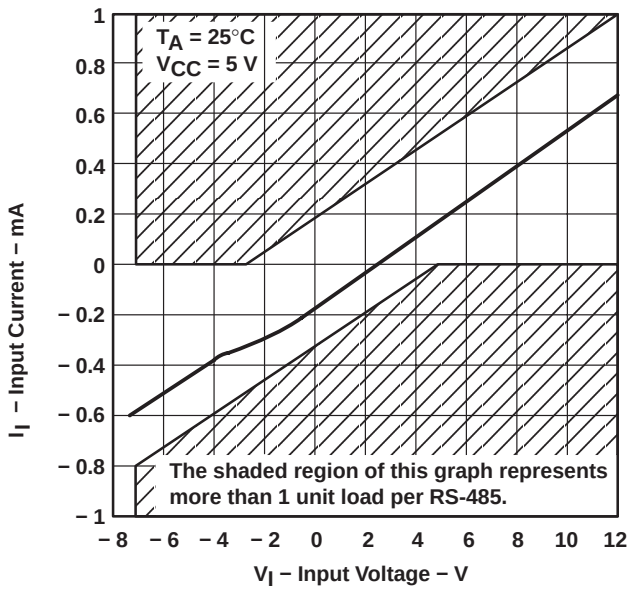


Figure 14

RECEIVER PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

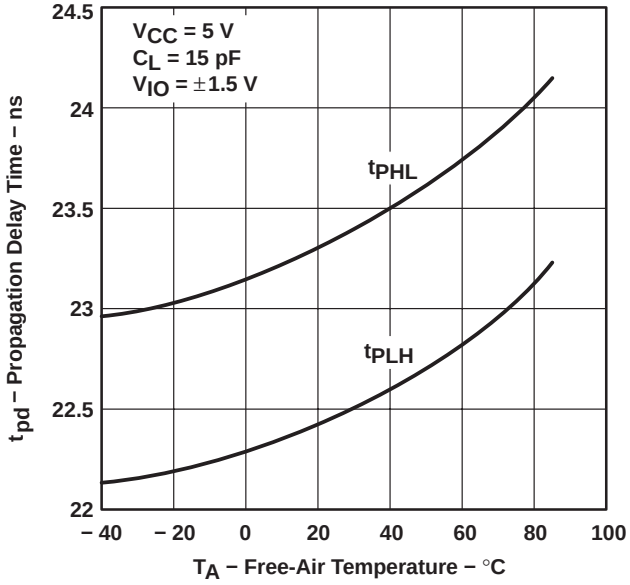


Figure 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LBC179D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC179DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC179DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC179DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC179P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC179PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC179QD	NRND	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN65LBC179QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC179QDR	NRND	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN65LBC179QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC179D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC179DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC179DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC179DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC179P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC179PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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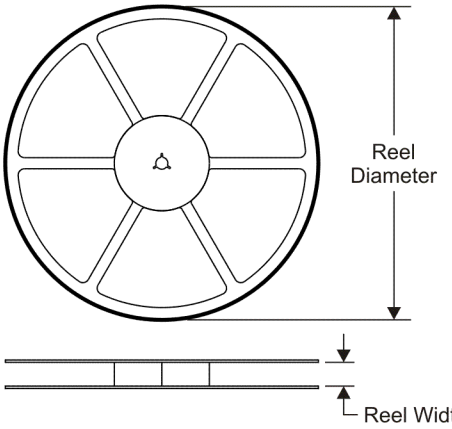
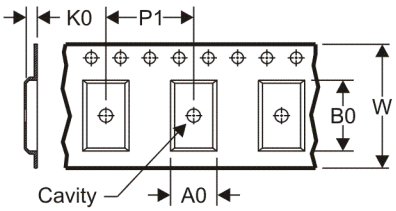
TAPE AND REEL INFORMATION

REEL DIMENSIONS

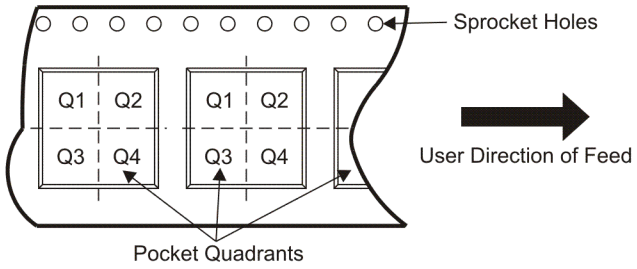


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

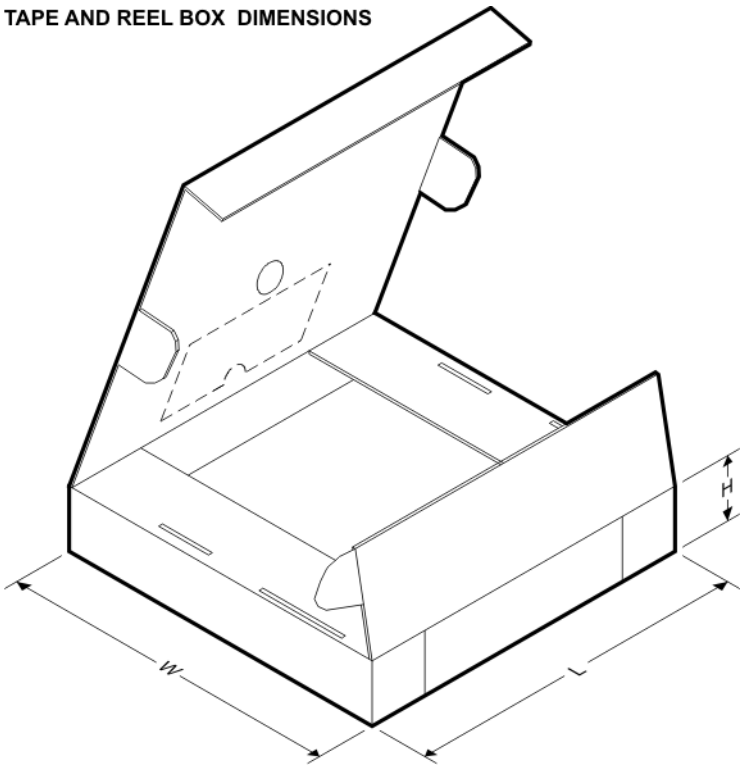
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

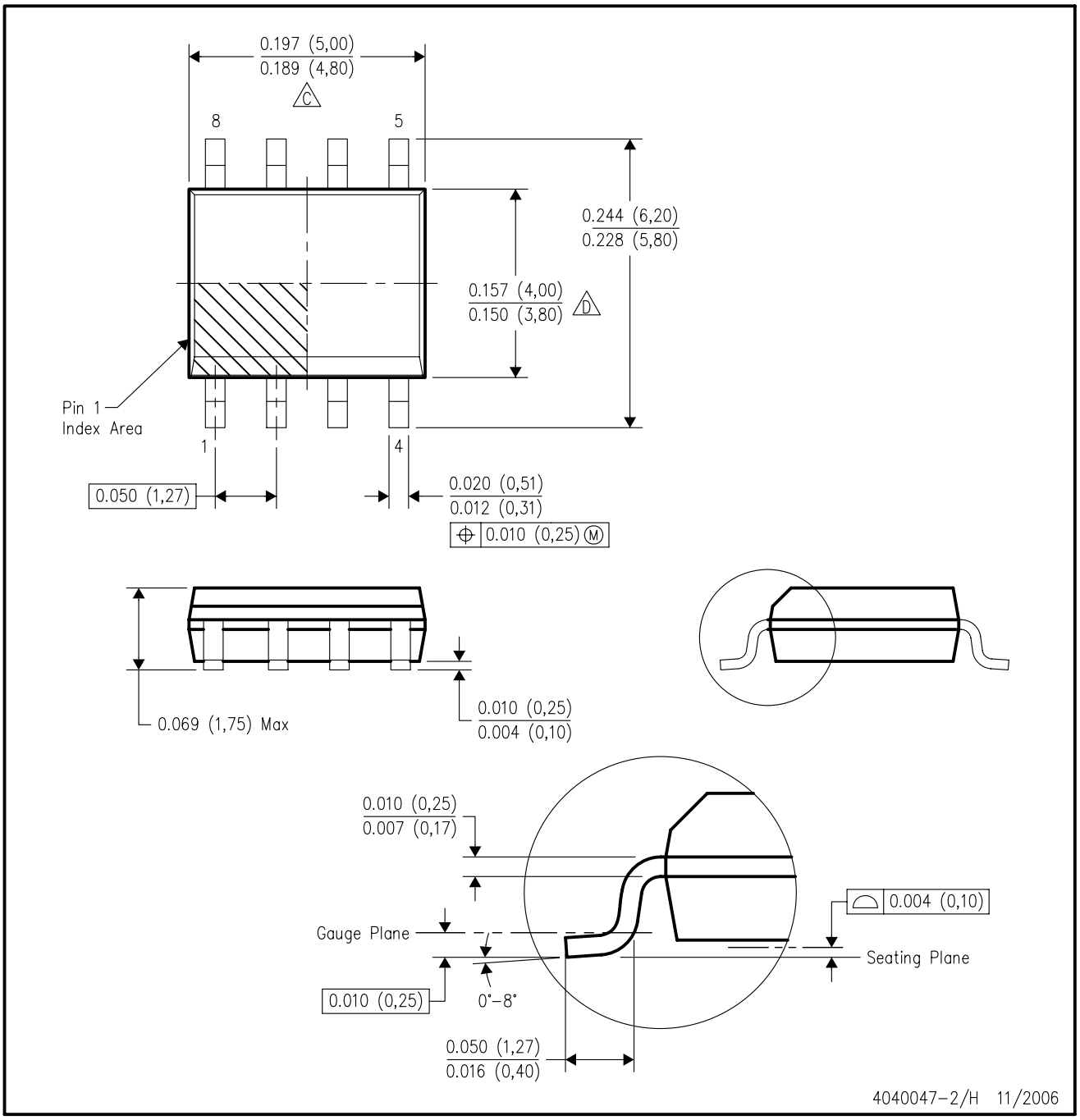
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179DR	SOIC	D	8	2500	342.9	338.1	20.6
SN75LBC179DR	SOIC	D	8	2500	342.9	338.1	20.6

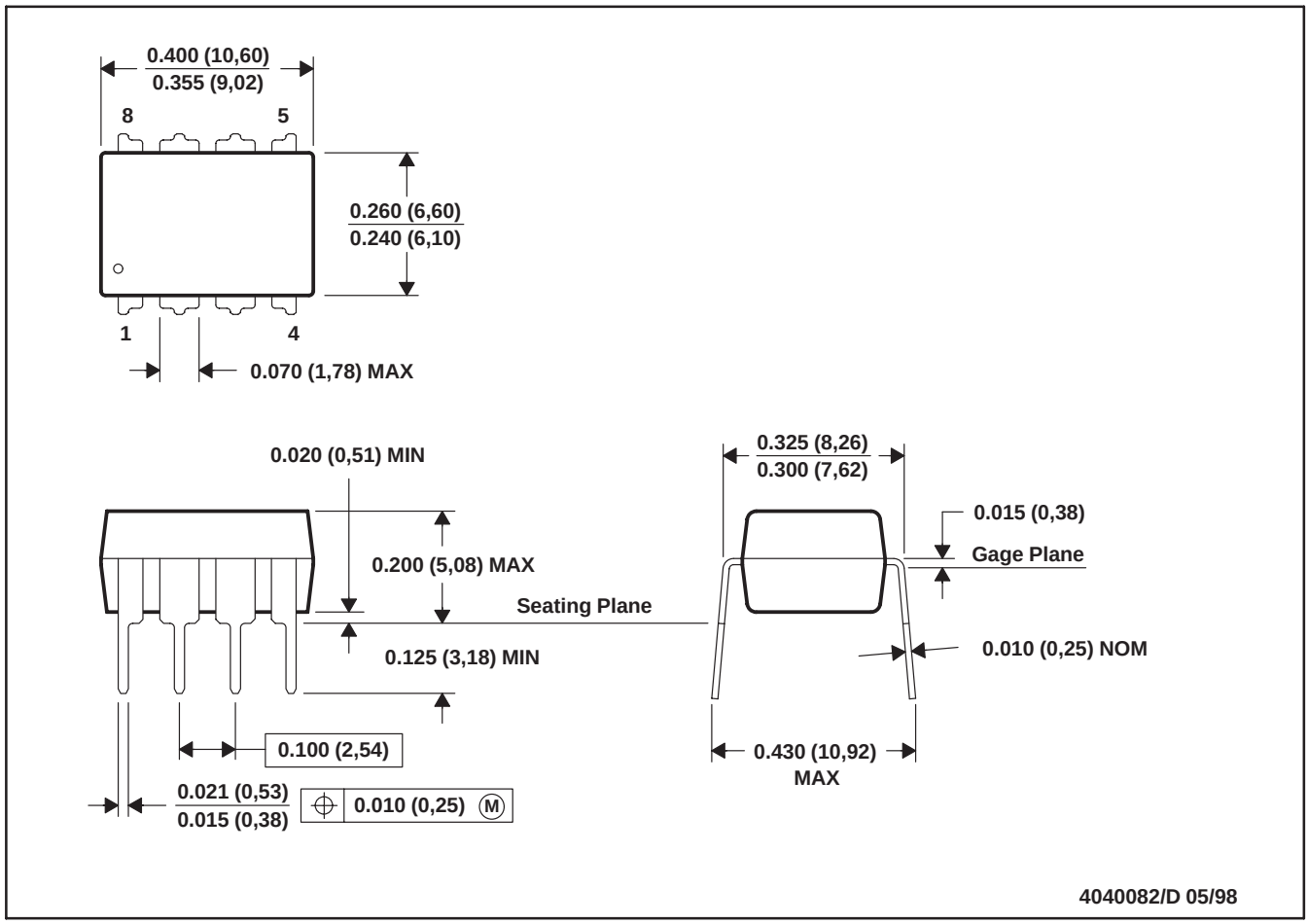
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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