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- Four ('391), Eight ('389) or Sixteen ('387) Line Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
- Designed for Signaling Rates<sup>†</sup> up to 630 Mbps With Very Low Radiation (EMI)
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Propagation Delay Times Less Than 2.9 ns
- Output Skew Is Less Than 150 ps
- Part-to-Part Skew Is Less Than 1.5 ns
- 35-mW Total Power Dissipation in Each Driver Operating at 200 MHz
- Driver Is High Impedance When Disabled or With V<sub>CC</sub> < 1.5 V</li>
- SN65' Version Bus-Pin ESD Protection Exceeds 15 kV
- Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch
- Low-Voltage TTL (LVTTL) Logic Inputs Are 5-V Tolerant

### description

This family of four, eight, and sixteen differential line drivers implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the sixteen current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100- $\Omega$  load when enabled.

LVDS389 DBT PACKA (TOP VIEW)	GE	<sup>?</sup> LVDS387 DGG PACKAGE (TOP VIEW)			
GND [ 1 <sup>0</sup> 38 V <sub>CC</sub> [ 2 37 GND [ 3 36 ENA [ 4 35 A1A [ 5 34 A2A [ 6 33 A3A [ 7 32 A4A [ 8 31 GND [ 9 30 V <sub>CC</sub> [ 10 29 GND [ 11 28 B1A [ 12 27 B2A [ 13 26 B3A [ 14 25 B4A [ 15 24 ENB [ 16 23	, A1Y A2Y A2Z A2Z A3Y A3Z A4Y A4Z NC NC B1Y B1Z B2Y B2Z B3Y B3Z	GND [ 1 V <sub>CC</sub> [ 2 V <sub>CC</sub> [ 3 GND [ 4 ENA [ 5 A1A [ 6 A2A [ 7 A3A [ 8 A4A [ 9 ENB [ 10 B1A [ 11 B2A [ 12 B3A [ 13 B4A [ 14 GND [ 15 V <sub>CC</sub> [ 16 V <sub>CC</sub> [ 17	64 A1Y 63 A1Z 62 A2Y 61 A2Z 60 A3Y 59 A3Z 58 A4Y 57 A4Z 56 B1Y 55 B1Z 54 B2Y 53 B2Z 52 B3Y 51 B3Z 50 B4Y 49 B4Z 48 C1Y		
GND [] 17 22 V <sub>CC</sub> [] 18 21 GND [] 19 20	B4Y B4Z	GND [ 18 C1A [ 19 C2A [ 20 C3A [ 21	47 C1Z 46 C2Y 45 C2Z 44 C3Y		
LVDS391 D OR PW PACK (TOP VIEW		C4A [ 22 ENC [ 23 D1A [ 24	43 C3Z 42 C4Y 41 C4Z		
V <sub>CC</sub> 4 13 GND 5 12 3A 6 11	] 1Z ] 2Y ] 2Z ] 3Y ] 3Z ] 4Y	D2A [ 25 D3A [ 26 D4A [ 27 END [ 28 GND [ 29 V <sub>CC</sub> [ 30 V <sub>CC</sub> [ 31 GND [ 32	40 D1Y 39 D1Z 38 D2Y 37 D2Z 36 D3Y 35 D3Z 34 D4Y 33 D4Z		

The intended application of this device and signaling technique is for point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100  $\Omega$ . The transmission media can be printed-circuit board traces, backplanes, or cables. The large number of drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with the companion 16- or 8-channel receivers, the SN65LVDS386 or SN65LVDS388, over 300 million data transfers per second in single-edge clocked systems are possible with very little power. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

<sup>†</sup> Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



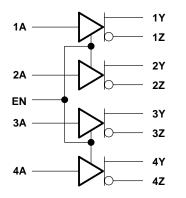
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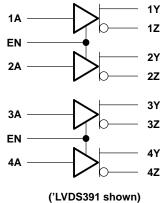
### description (continued)

When disabled, the driver outputs are high impedance. Each driver input (A) and enable (EN) have an internal pulldown that will drive the input to a low level when open circuited.

The SN65LVDS387, SN65LVDS389, and SN65LVDS391 are characterized for operation from -40°C to 85°C. The SN75LVDS387, SN75LVDS389, and SN75LVDS391 are characterized for operation from 0°C to 70°C.

### logic diagram (positive logic)





(1/4 of 'LVDS387 or 1/2 of 'LVDS389 shown)

('LVDS391 s	howr
-------------	------

AVAILABLE OPTIONS								
PART NUMBER <sup>†</sup>	TEMPERATURE RANGE	NO. OF DRIVERS	BUS-PIN ESD					
SN65LVDS387DGG	–40°C to 85°C	16	15 kV					
SN75LVDS387DGG	0°C to 70°C	16	4 kV					
SN65LVDS389DBT	–40°C to 85°C	8	15 kV					
SN75LVDS389DBT	0°C to 70°C	8	4 kV					
SN65LVDS391D	–40°C to 85°C	4	15 kV					
SN75LVDS391D	0°C to 70°C	4	4 kV					
SN65LVDS391PW	–40°C to 85°C	4	15 kV					
SN75LVDS391PW	0°C to 70°C	4	4 kV					

### AVAILABLE OPTIONS

<sup>†</sup> This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., SN65LVDS387DGGR).

#### **DRIVER FUNCTION TABLE**

INPUT	ENABLE	OUTPUTS			
Α	EN	Y	Z		
Н	Н	Н	L		
L	Н	L	н		
х	L	Z	Z		
OPEN	Н	L	Н		

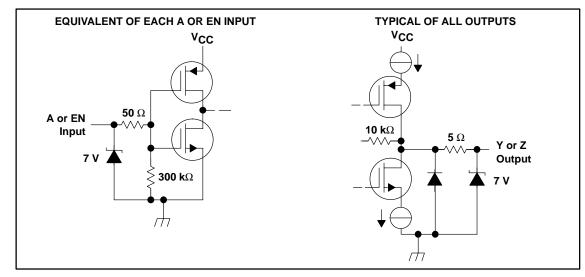
H = high-level, L = low-level, X = irrelevant,

Z = high-impedance (off)



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### equivalent input and output schematic diagrams



## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub>	–0.5 V to 4 V
Input voltage range: Inputs	–0.5 V to 6 V
Y or Z	–0.5 V to 4 V
Electrostatic discharge: SN65' (Y, Z, and GND)	Class 3, A:15 kV, B: 500 V
SN75' (Y, Z, and GND)	Class 3, A:4 kV, B: 400 V
Continuous power dissipation	(see Dissipation Rating Table)
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

2. Tested in accordance with MIL-STD-883C Method 3015.7.

#### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C	DERATING FACTOR <sup>‡</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DBT	1071 mW	8.5 mW/°C	688 mW	556 mW
DGG	2094 mW	16.7 mW/°C	1342 mW	1089 mW
PW	774 mW	6.2 mW/°C	496 mW	402 mW

<sup>‡</sup>This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>				3.6	V
High-level input voltage, VIH		2			V
Low-level input voltage, VIL				0.8	V
Operating free-air temperature, T <sub>A</sub>	SN75'	0		70	°C
	SN65'	-40		85	°C



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### electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CC	TEST CONDITIONS			MAX	UNIT	
Vod	Differential output voltage magnitude	P. 400.0		247	340	454		
$\Delta  V_{OD} $	Change in differential output voltage magnitude between logic states	$R_L = 100 \Omega$ , , See Figure 1 and Fig	-50		50	mV		
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage		1.125		1.375	V		
∆VOC(SS)	Change in steady-state common-mode output voltage between logic states	See Figure 3		-50		50	mV	
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage	1			50	150	mV	
	11VD0007		Enabled.		85	95		
ICC	Supply current	'LVDS389	$R_L = 100 \Omega$ ,		50	70	mA	
		'LVDS391	V <sub>IN</sub> = 0.8 V or 2 V		20	26		
		'LVDS387			0.5	1.5		
		'LVDS389	Disabled, V <sub>IN</sub> = 0 V or V <sub>CC</sub>		0.5	1.5		
		'LVDS391			0.5	1.3	l	
Iн	High-level input current	V <sub>IH</sub> = 2 V			3	20	μA	
Ι <sub>ΙL</sub>	Low-level input current	V <sub>IL</sub> = 0.8 V			2	10	μA	
		$V_{OY}$ or $V_{OZ} = 0 V$				±24	mA	
los	Short-circuit output current	V <sub>OD</sub> = 0 V				±12	mA	
IOZ	High-impedance output current	VO = 0 V or VCC				±1	μA	
lO(OFF)	Power-off output current	V <sub>CC</sub> = 1.5 V,	V <sub>O</sub> = 2.4 V			±1	μA	
CIN	Input capacitance	V <sub>I</sub> = 0.4 sin (4E6πt) + 0.5 V			5		pF	
с <sub>о</sub>	Output capacitance	$V_I = 0.4 \sin (4E6\pi t) + Disabled$		9.4		pF		

<sup>†</sup> All typical values are at 25°C and with a 3.3-V supply.

### switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	түр†	MAX	UNIT
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output		0.9	1.7	2.9	ns
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output		0.9	1.6	2.9	ns
t <sub>r</sub>	Differential output signal rise time	$R_{I} = 100 \Omega$ ,	0.4	0.8	1	ns
t <sub>f</sub>	Differential output signal fall time	$C_{L} = 100 \Omega_{2},$		0.8	1	ns
<sup>t</sup> sk(p)	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	See Figure 4		150	500	ps
<sup>t</sup> sk(o)	Output skew‡			80	150	ps
<sup>t</sup> sk(pp)	Part-to-part skew§				1.5	ns
<sup>t</sup> PZH	Propagation delay time, high-impedance-to-high-level output			6.4	15	ns
<sup>t</sup> PZL	Propagation delay time, high-impedance-to-low-level output			5.9	15	ns
<sup>t</sup> PHZ	Propagation delay time, high-level-to-high-impedance output	See Figure 5		3.5	15	ns
<sup>t</sup> PLZ	Propagation delay time, low-level-to-high-impedance output			4.5	15	ns

<sup>†</sup> All typical values are at 25°C and with a 3.3-V supply.

‡ t<sub>sk(0)</sub> is the magnitude of the time difference between the t<sub>PLH</sub> or t<sub>PHL</sub> of all drivers of a single device with all of their inputs connected together. § tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.



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### PARAMETER MEASUREMENT INFORMATION

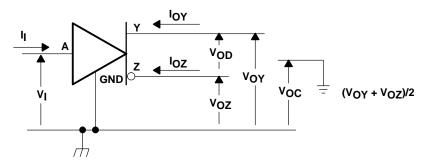
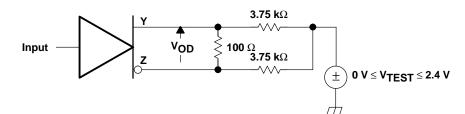
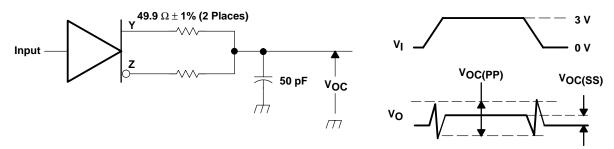


Figure 1. Voltage and Current Definitions

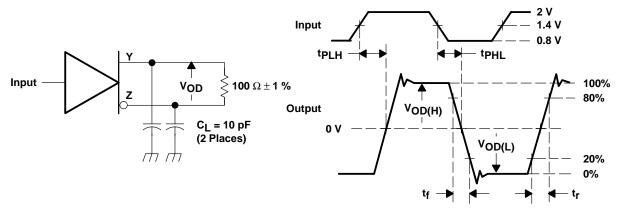


**Figure 2. VOD Test Circuit** 



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C1 includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of VOC(PP) is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

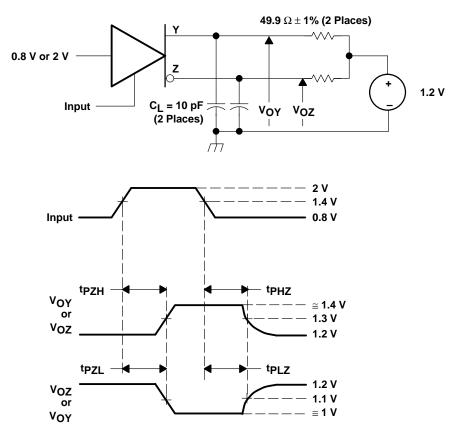


NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width =  $10 \pm 0.2$  ns. C<sub>1</sub> includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

#### Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



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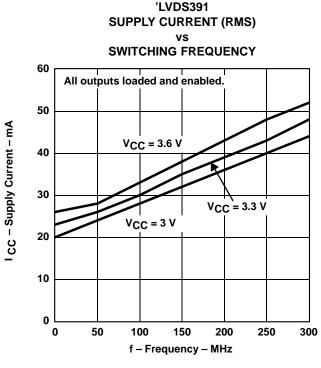


### PARAMETER MEASUREMENT INFORMATION

NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500  $\pm$  10 ns. CL includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

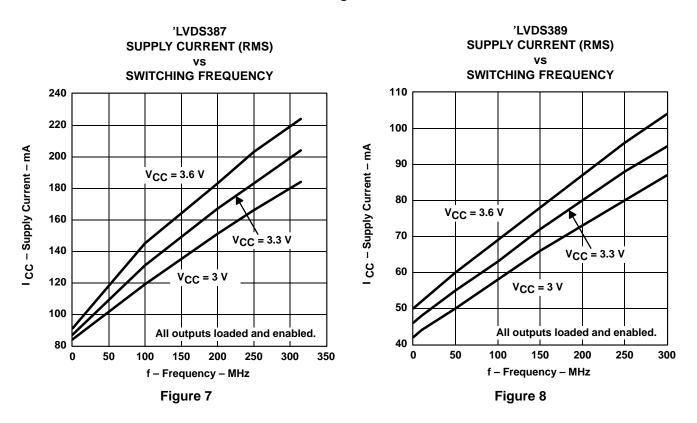
Figure 5. Enable and Disable Time Circuit and Definitions





### TYPICAL CHARACTERISTICS

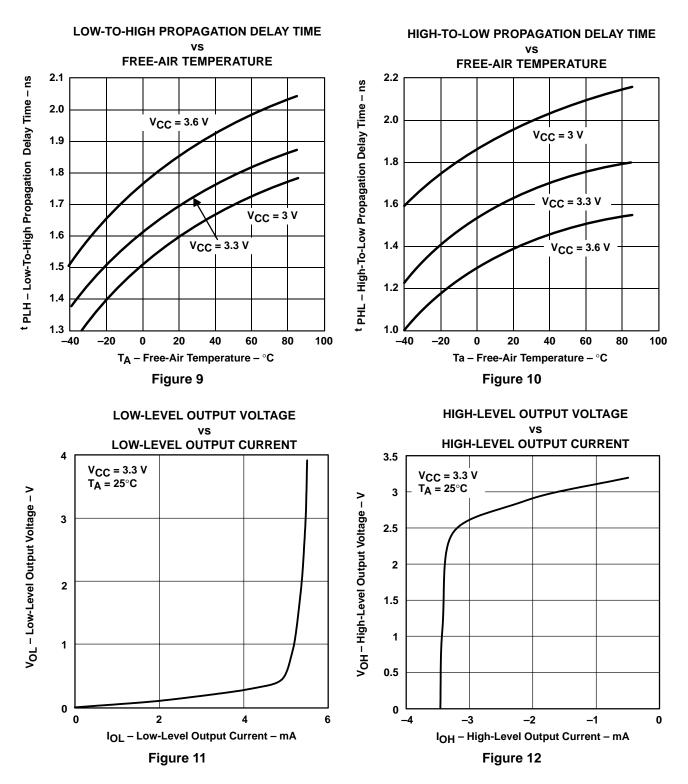






### SN65LVDS387, SN75LVDS387, SN65LVDS389 SN75LVDS389, SN65LVDS391, SN75LVDS391 HIGH-SPEED DIFFERENTIAL LINE DRIVERS SLLS362D – SEPTEMBER 1999 – REVISED MAY 2001

TYPICAL CHARACTERISTICS





## **TYPICAL CHARACTERISTICS**

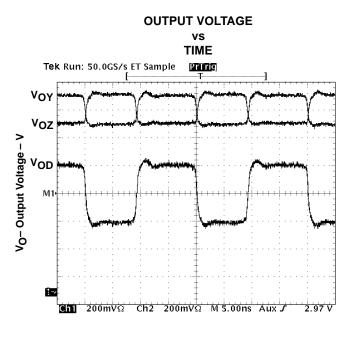
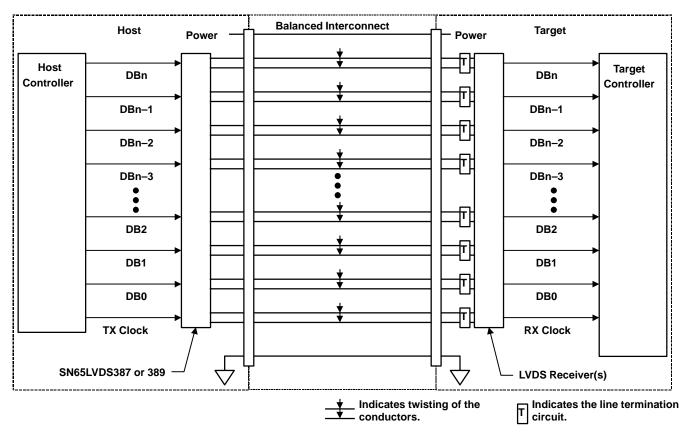




Figure 13



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### **APPLICATION INFORMATION**

Figure 14. Typical Application Schematic

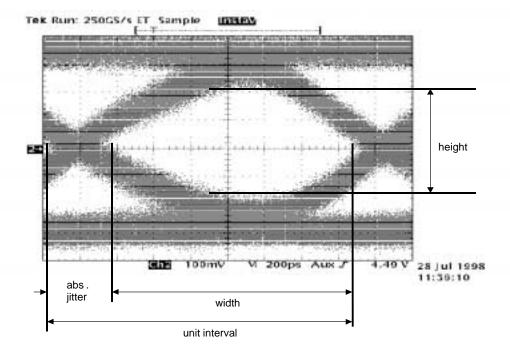
## **Signaling Rate vs Distance**

The ultimate data transfer rate over a given cable or trace length involves many variables. Starting with the capabilities of this LVDS driver to reproduce a data pulse as short as 1.6 ns (a 630 Mbps signaling rate) with less than 500 ps of pulse distortion, any degradation of this pulse by the transmission media will necessarily reduce the timing margin at the receiving end of the data link.

The timing uncertainty induced by the transmission media is commonly referred to as jitter and comes from numerous sources. The characteristics of a particular transmission media can be quantified by using an eyepattern measurement such as shown in Figure 12, which shows about 340 ps of jitter or 20% of the data pulse width.



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### **APPLICATION INFORMATION**

Figure 15. Typical LVDS Eyepattern

A generally accepted range of jitter at the receiver inputs that allows data recovery is 5% to 20% of the unit interval (data pulse width). Table 1 shows the signaling rate achieved on various cables and lengths at a 5% eyepattern jitter with a typical LVDS driver.

Table 1. Signaling Rates for Various Cables for 5% Eyepatter	n Jitter
--------------------------------------------------------------	----------

LENGTH	CABLE <sup>†</sup>							
(m)	A (Mbps)			D (Mbps)	E (Mbps)	F (Mbps)		
1	240	200	240	270	180	230		
5	205	210	230	250	215	230		
10	180	150	195	200	145	180		

<sup>†</sup>Cable A: CAT 3, specified up to 16 MHz, no shield, outside conductor diameter (Ø) 0.52 mm

Cable B: CAT 5, specified up to 100 MHz, no shield, Ø 0.52 mm

Cable C: CAT 5, specified up to 100 MHz, taped over all shield,  $\varnothing$  0.52 mm

Cable D: CAT 5 (exceeding CAT 5), specified up to 300 MHz, braided over all shield plus taped individual shield for any pair, Ø 0.64 mm (AWG22)

Cable E: CAT 5 (exceeding CAT 5), specified up to 350 MHz,  $\varnothing$  0.64 mm (AWG22), no shield

Cable F: CAT 5 (exceeding CAT 5), specified up to 350 MHz, "self-shielded", Ø 0.64 mm (AWG22)

During synchronous parallel transfers, skew between the data and clock lines will also reduce the timing margin. This must be accounted for in the system timing budget. Fortunately, the low output skew of this LVDS driver will generally be a small portion of this budget.

## other LVDS products

For other products and applications notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

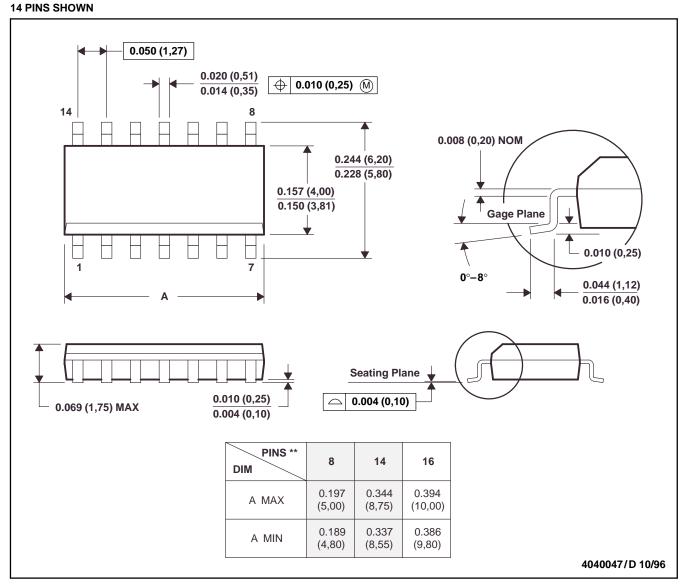


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**MECHANICAL DATA** 

### D (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

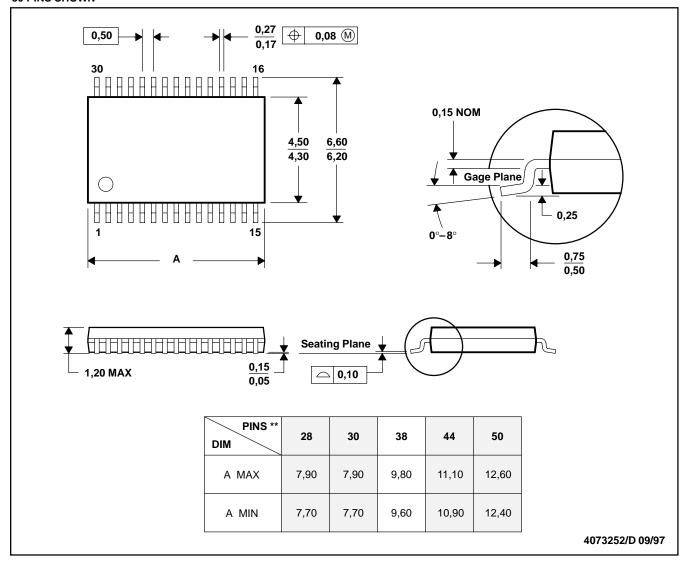


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### **MECHANICAL DATA**

#### PLASTIC SMALL-OUTLINE PACKAGE

DBT (R-PDSO-G\*\*) **30 PINS SHOWN** 



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

D. Falls within JEDEC MO-153



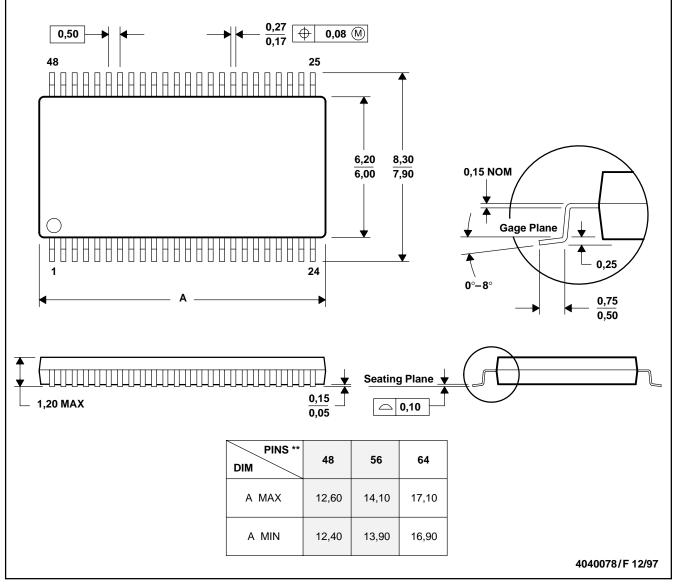
# SN65LVDS387, SN75LVDS387, SN65LVDS389 SN75LVDS389, SN65LVDS391, SN75LVDS391 HIGH-SPEED DIFFERENTIAL LINE DRIVERS SLLS362D - SEPTEMBER 1999 - REVISED MAY 2001

**MECHANICAL DATA** 

### DGG (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

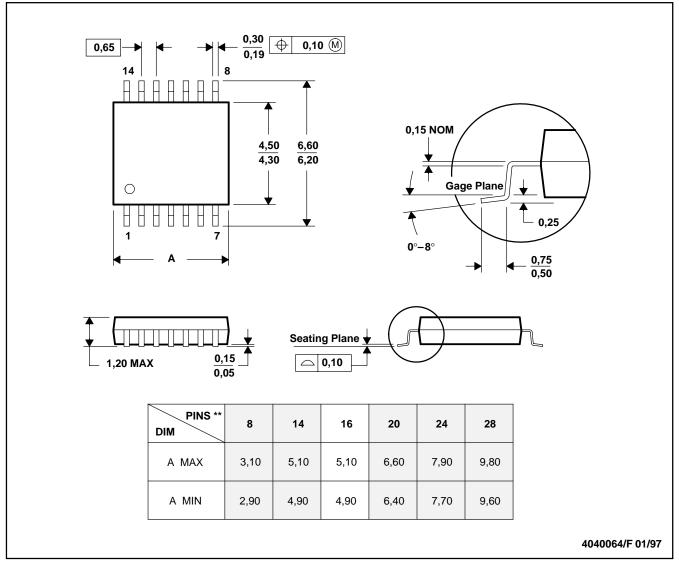


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### **MECHANICAL DATA**

### PLASTIC SMALL-OUTLINE PACKAGE

PW (R-PDSO-G\*\*) **14 PINS SHOWN** 



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



12-Feb-2008

### **PACKAGING INFORMATION**

TEXAS INSTRUMENTS www.ti.com

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS387DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS387DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS389DBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS389DBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS389DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS389DBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS391D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LVDS391PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS387DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS387DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS387DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS387DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS389DBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS389DBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS389DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS389DBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LVDS391D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75LVDS391DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS391DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS391DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS391PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS391PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS391PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS391PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

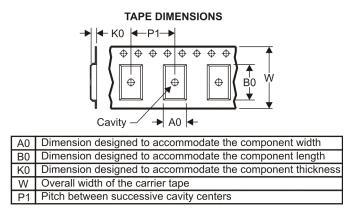
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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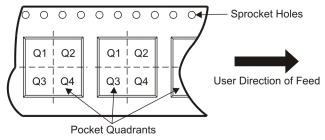
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## TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

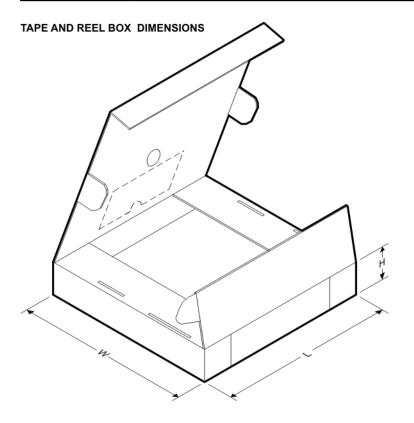


*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS387DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDS389DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDS391DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS391PWR	TSSOP	PW	16	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1
SN75LVDS387DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN75LVDS389DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75LVDS391DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LVDS391PWR	TSSOP	PW	16	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1



# PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS387DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0
SN65LVDS389DBTR	TSSOP	DBT	38	2000	346.0	346.0	33.0
SN65LVDS391DR	SOIC	D	16	2500	346.0	346.0	33.0
SN65LVDS391PWR	TSSOP	PW	16	2000	346.0	346.0	29.0
SN75LVDS387DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0
SN75LVDS389DBTR	TSSOP	DBT	38	2000	346.0	346.0	33.0
SN75LVDS391DR	SOIC	D	16	2500	346.0	346.0	33.0
SN75LVDS391PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

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