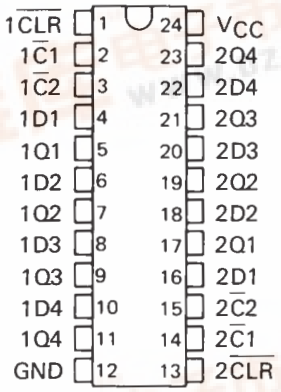
DECEMBER 1972—REVISED MARCH 1988

- Two Independent 4-Bit Latches in a Single Package
- Separate Clear Inputs Provide One-Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading Register Implementations
- Compatible for Use with TTL Circuits
- Input Clamping Diodes Simplify System Design

SN54116 . . . J OR W PACKAGE
SN74116 . . . N PACKAGE
(TOP VIEW)



description

These monolithic TTL circuits utlize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

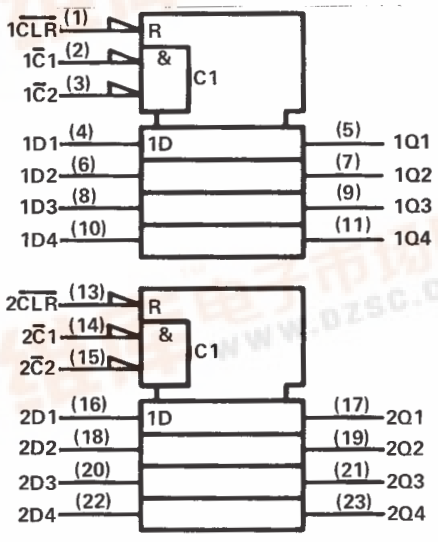
The SN54116 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74116 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS				OUTPUT
CLEAR	ENABLE $\overline{C1}$	ENABLE $\overline{C2}$	DATA	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

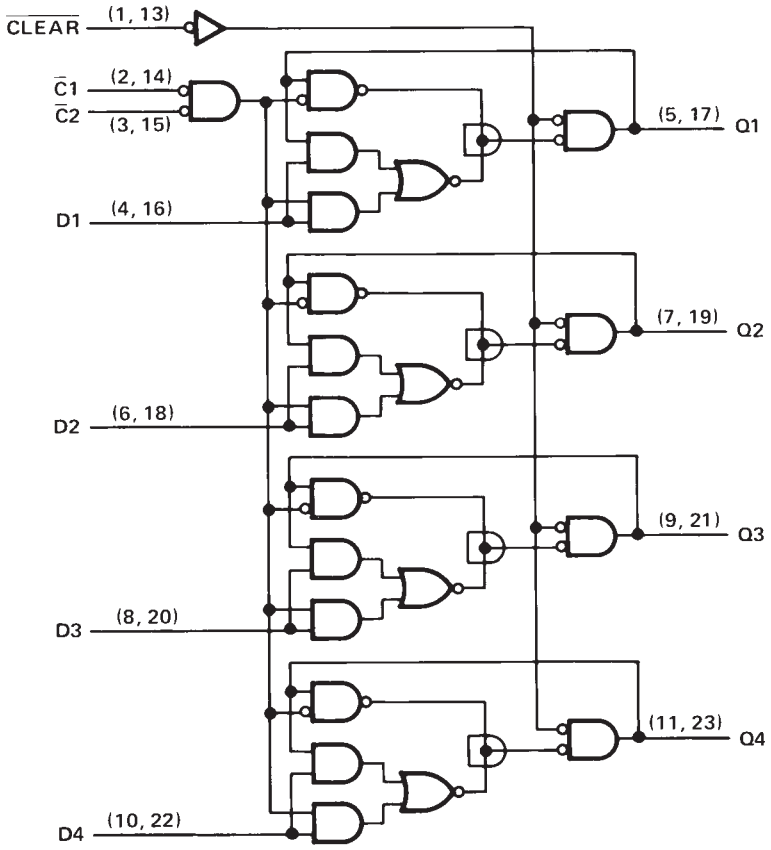
H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before these input conditions were established.

logic symbol†

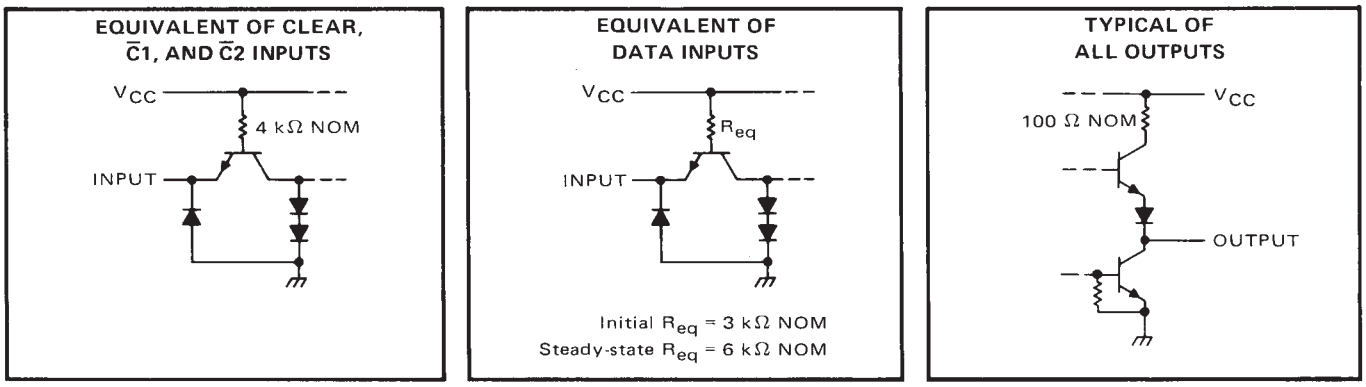


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Operating free-air temperature range:	SN54116 Circuits	−55°C to 125°C
	SN74116 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54116			SN74116			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Input pulse width, t_w	$\overline{C1}$, $\overline{C2}$	18			18			ns
	$\overline{CLR}$	18			18			
Data setup time, t_{su}	High logic level	8			8			ns
	Low logic level	14			14			
Clear inactive-state setup time, t_{su}		8			8			ns
Data release time, high-level data, $t_{release}$				2			2	ns
Data hold time, low-level data, t_h		8			8			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

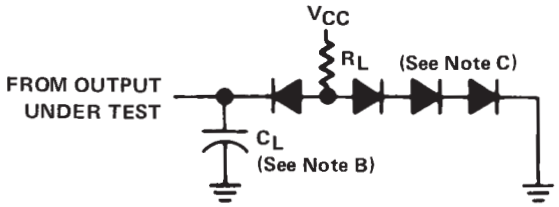
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	$\overline{C1}$, $\overline{C2}$, or clear	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Any D					60	
I_{IL}	Low-level input current	$\overline{C1}$, $\overline{C2}$, or clear	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Any D, initial peak					−2.4	
		Any D, steady-state					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54116	−20		−57	mA
				SN74116	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition A		60	100	mA
				Condition B		40	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With outputs open, I_{CC} is measured for the following conditions:
A. All inputs grounded.
B. All $\overline{C}$ inputs are grounded and all other inputs are at 4.5 V.

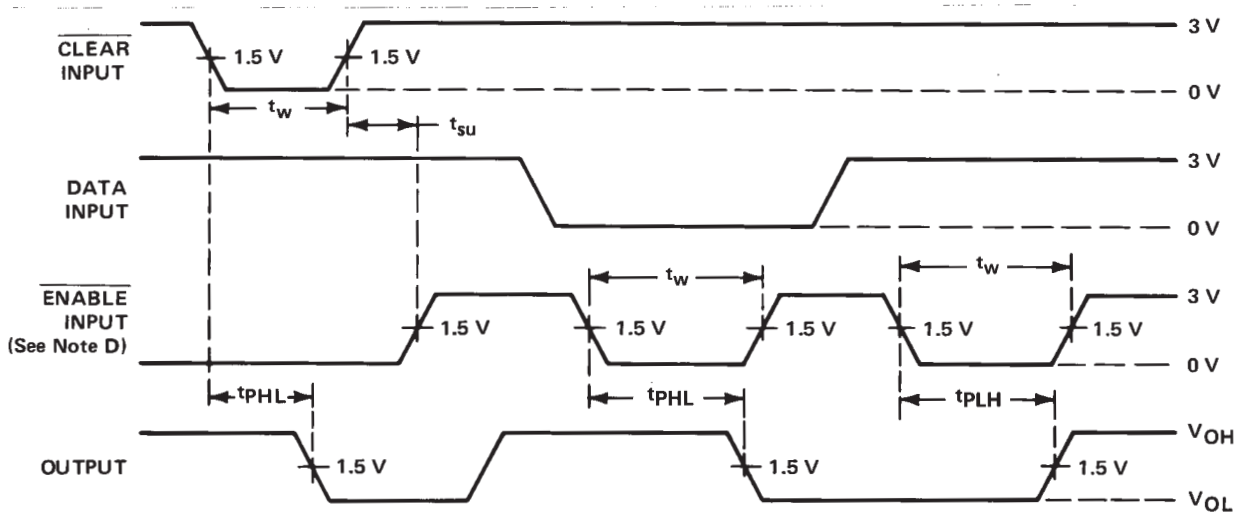
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$\overline{C1}$ or $\overline{C2}$	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		19	30	ns
t_{PHL}					15	22	
t_{PLH}	Data	Q			10	15	ns
t_{PHL}					12	18	
t_{PHL}	$\overline{CLR}$	Any Q			15	22	ns

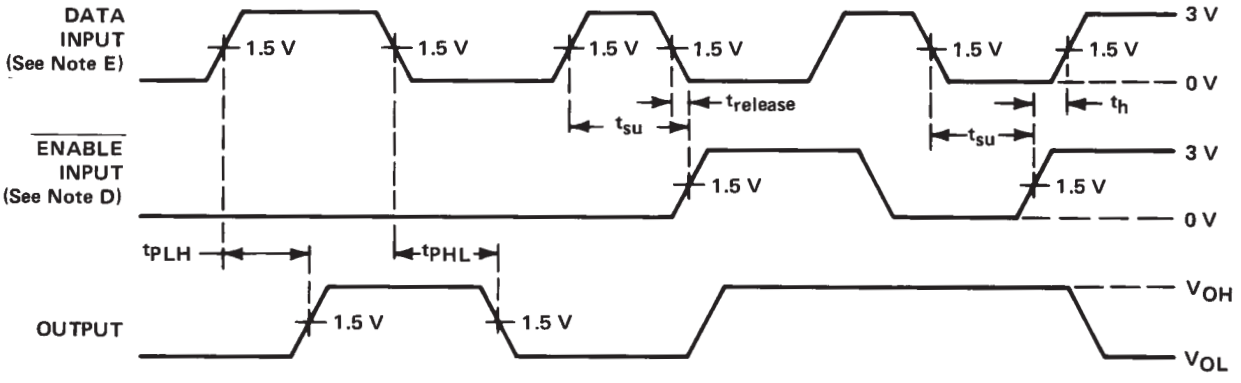
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



SWITCHING TIMES FROM CLEAR AND ENABLE INPUTS



SWITCHING TIMES FROM DATA INPUTS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. The other enable input is low.
E. Clear input is high.

FIGURE 1

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