

- Latched Data Inputs Serve as Buffer Register and Can also:
Synchronize Data Acquisition
“Debounce” Mechanical Switch Input
- Cascading Input P0 and Output P1
Provides “Busy” Signal Inhibiting All Lower-Order Bits
- Full TTL Compatibility
- Use for:
Priority Interrupt
Synchronous Priority Line Selection

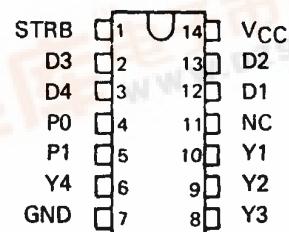
description

The SN54278 and SN74278 each consist of four data latches, full priority output gating, and a cascading gate. The highest-order data applied at a D latch input is transferred to the appropriate Y output while the strobe input is high, and when the strobe goes low all data is latched. The cascading input P0 is fully overriding and on the highest-order package this input must be held at a low logic level. The P1 output is intended for connection to the P0 input of the next lower-order package and will provide a “busy” (high-level) signal to inhibit all subsequent lower-order packages.

After the overriding P0 input, the order of priority is D1, D2, D3, and D4, respectively, within the package.

SN54278 . . . J OR W PACKAGE
SN74278 . . . N PACKAGE

(TOP VIEW)



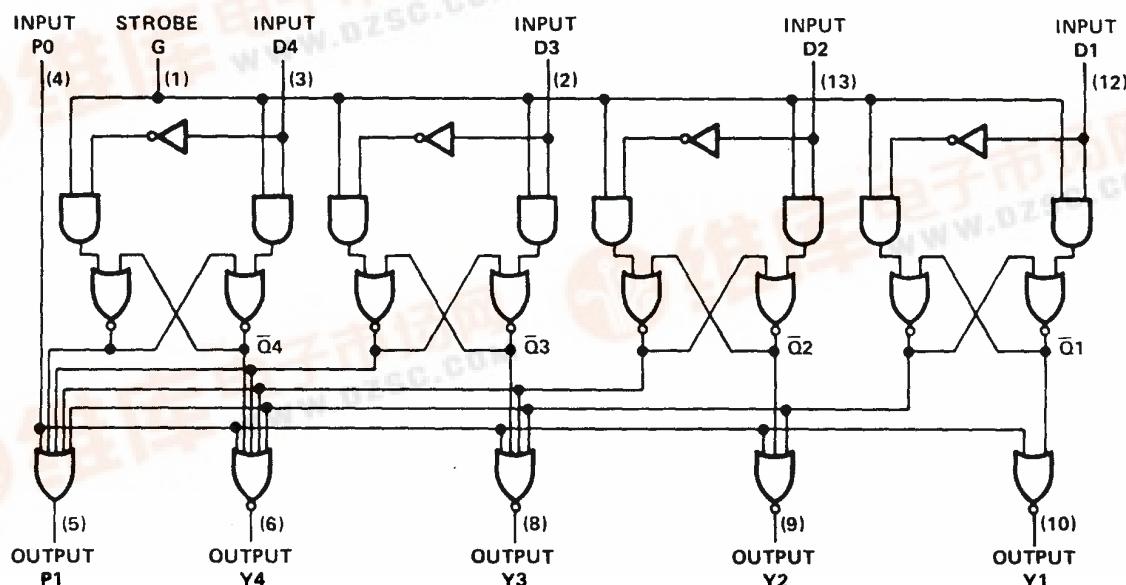
NC—No internal connection

FUNCTION TABLE

| | | INPUTS | | | | INTERNAL LATCH NODES | | | | OUTPUTS | | | | |
|----|---|-------------|----|----|----|---|-------------|-------------|-------------|-----------|----|----|----|----|
| P0 | G | D1 | D2 | D3 | D4 | \bar{Q}_1 | \bar{Q}_2 | \bar{Q}_3 | \bar{Q}_4 | Y1 | Y2 | Y3 | Y4 | P1 |
| L | H | H | X | X | X | L | X | X | X | H | L | L | L | H |
| L | H | L | H | X | X | H | L | X | X | L | H | L | L | H |
| L | H | L | L | H | X | H | H | L | X | L | L | H | L | H |
| L | H | L | L | L | H | H | H | H | L | L | L | H | H | H |
| L | H | L | L | L | L | H | H | H | H | L | L | L | L | L |
| | | | | | | Same function of \bar{Q} nodes as on 1st 5 lines | | | | | | | | |
| | | L L X X X X | | | | Latched when G goes low | | | | | | | | |
| | | | | | | | | | | L L L L H | | | | |
| | | H H | | | | Internal \bar{Q} levels are same function of D inputs as on first 5 lines | | | | L L L L H | | | | |

H = high level, L = low level, X = irrelevant

logic diagram (positive logic)



SN54278, SN74278

4-BIT CASCADEABLE PRIORITY REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Interemitter voltage (see Note 2) | 5.5 V |
| Operating free-air temperature range: SN54278 Circuits | -55°C to 125°C |
| SN74278 Circuits | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the strobe input and any of the four data inputs.

recommended operating conditions

| | SN54278 | | | SN74278 | | | UNIT |
|--|---------|-----|------|---------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} | | | -800 | | | -800 | μA |
| Low-level output current, I_{OL} | | | 16 | | | 16 | mA |
| Data setup time, t_{SU} (see Figure 1) | | | 20 | | | 20 | ns |
| Data hold time, t_h (see Figure 1) | | | 5 | | | 5 | ns |
| Strobe pulse width, t_w (see Figure 1) | | | 20 | | | 20 | ns |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS [†] | | MIN | TYP | MAX | UNIT |
|-----------|---|--|------------|-----|-------|------|------|
| V_{IH} | High-level input voltage | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | | | 0.8 | V |
| V_{IK} | Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$ | | | | -1.5 | V |
| V_{OH} | High-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$ | | 2.4 | 3.4 | | V |
| V_{OL} | Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$ | | | 0.2 | 0.4 | V |
| I_I | Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$ | | | 1 | | mA |
| I_{IH} | Any D input | | | | 80 | | |
| | P0 input | $V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$ | | | 200 | | μA |
| | G input | | | | 320 | | |
| I_{IL} | Any D input | | | | -3.2 | | |
| | P0 input | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -8 | | mA |
| | G input | | | | -12.8 | | |
| I_{OS} | Short-circuit output current [§] | $V_{CC} = \text{MAX}$ | SN54278 | -18 | -55 | | mA |
| | | | SN74278 | -18 | -57 | | |
| I_{CC} | Supply current | $V_{CC} = \text{MAX}$ | See Note 3 | | 55 | 80 | mA |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the P0 input grounded, all other inputs at 4.5 V, and outputs open.

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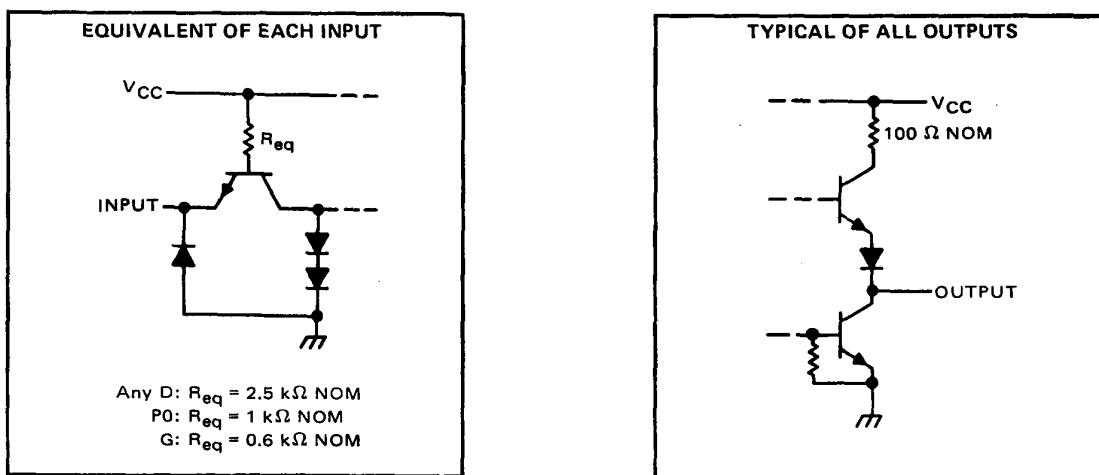
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER [†] | FROM (INPUT) | TO (OUTPUT) | WAVEFORMS | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|-----------------|----------------|-------------------------------|---|-----|-----|-----|------|
| t_{PLH} | Data | Y | A and C (with strobe high) | $C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1 | 30 | | | ns |
| t_{PHL} | | | A and D (with strobe high) | | 39 | | | |
| t_{PLH} | | Y | A and D (with strobe high) | | 38 | | | ns |
| t_{PHL} | | | A and E (with strobe high) | | 31 | | | |
| t_{PLH} | | P1 | A and E (with strobe high) | | 46 | | | ns |
| t_{PHL} | | | B and C or B and D | | 39 | | | |
| t_{PLH} | | Strobe | Any Y | | 30 | | | ns |
| t_{PHL} | | | P1 | | 31 | | | |
| t_{PLH} | | Strobe | B and E | | 38 | | | ns |
| t_{PHL} | | | P1 | | 42 | | | |
| t_{PLH} | | P0 | F and G | | 23 | | | ns |
| t_{PHL} | | | P1 | | 30 | | | |

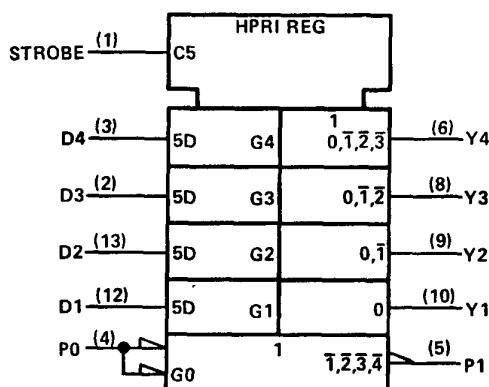
[†] t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

schematics of inputs and outputs



logic symbol[†]

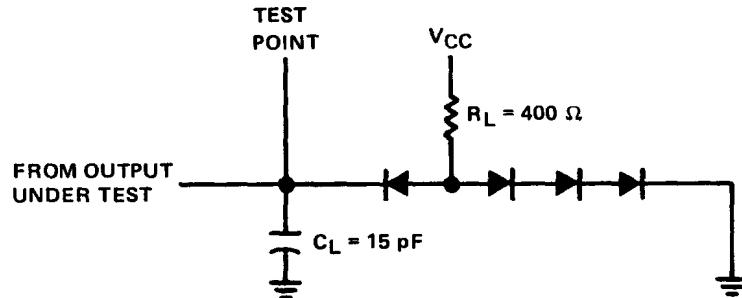


[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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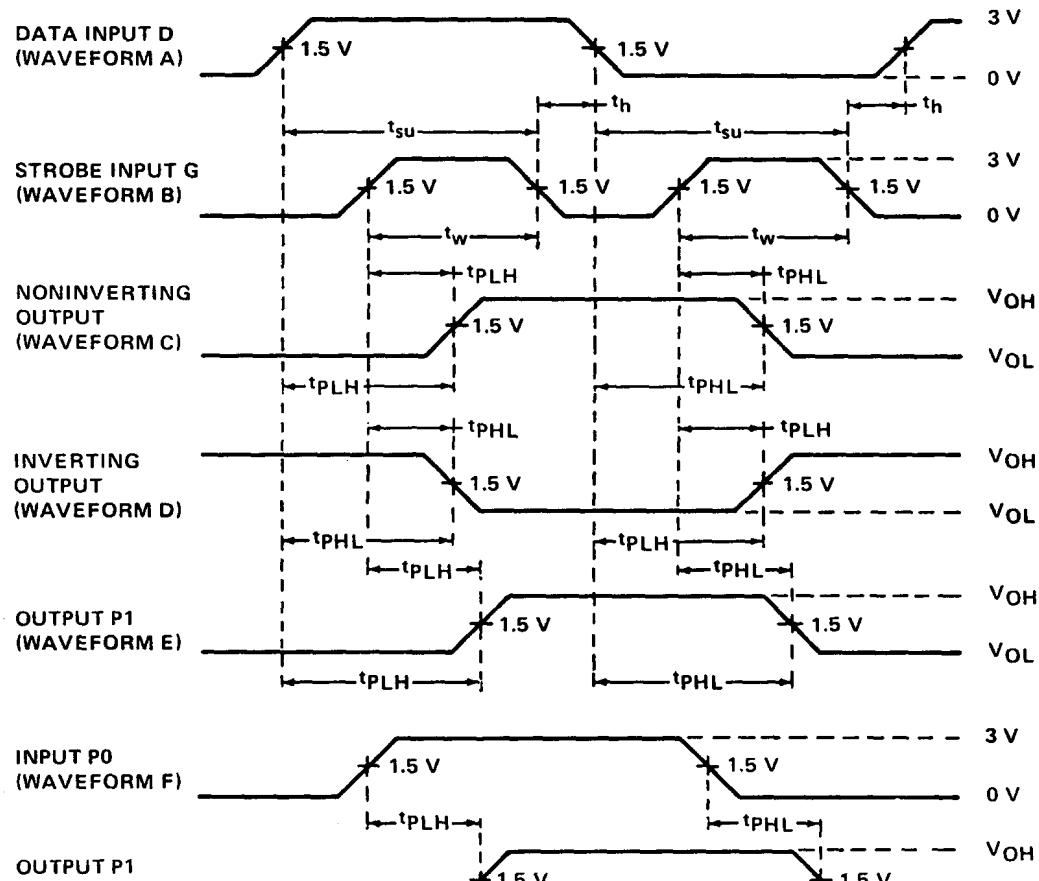
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PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTE: Input pulses are supplied by a generator having the following characteristics: $t_r \leq 7 \text{ ns}$, $t_f \leq 7 \text{ ns}$, $\text{PRR} \leq \text{MHz}$, $Z_{\text{out}} \approx 50\Omega$.

FIGURE 1—SWITCHING TIMES

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