

SN54ABT841, SN74ABT841A 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196D – FEBRUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

description

The SN54ABT841 and SN74ABT841A 10-bit latches are designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten transparent D-type latches provide true data at their outputs.

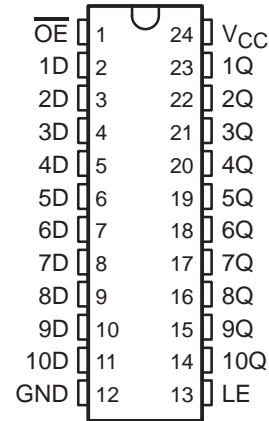
A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

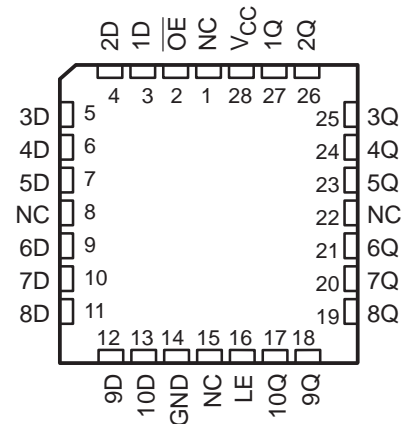
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT841 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT841A is characterized for operation from -40°C to 85°C .

SN54ABT841 . . . JT OR W PACKAGE
SN74ABT841A . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT841 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1997, Texas Instruments Incorporated

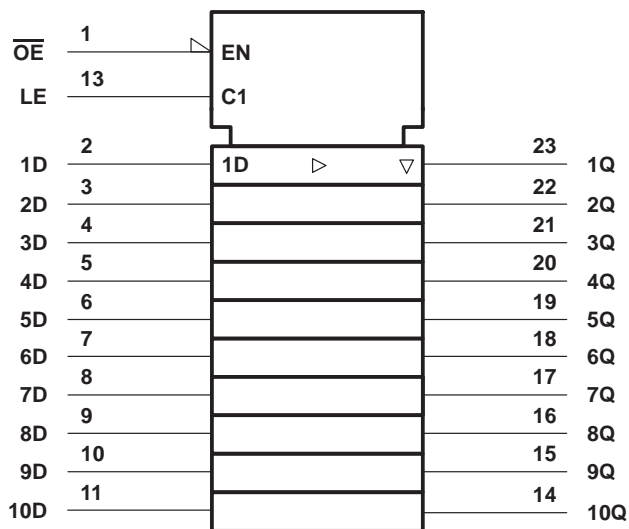
SN54ABT841, SN74ABT841A 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196D – FEBRUARY 1991 – REVISED MAY 1997

FUNCTION TABLE

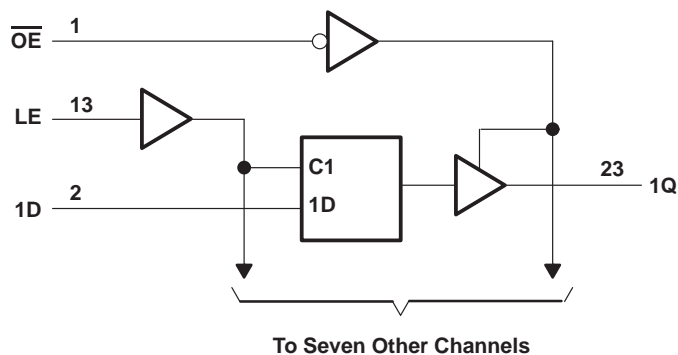
INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

SN54ABT841, SN74ABT841A

10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196D – FEBRUARY 1991 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT841	96 mA
SN74ABT841A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

	SN54ABT841		SN74ABT841A		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate		200		200	μs/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SN54ABT841, SN74ABT841A

10-BIT BUS-INTERFACE D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS196D – FEBRUARY 1991 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT841		SN74ABT841A		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5	V
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3	
	V _{CC} = 4.5 V			2		2		2	
V _{OL}	V _{CC} = 4.5 V					0.55		0.55	V
						0.55*		0.55	
V _{hys}				100					mV
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	µA
I _{OZPU} ‡	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	µA
I _{OZPD} ‡	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	µA
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	µA
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	µA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	µA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	µA
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V			-50 -140 -180		-50 -180		-50 -180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			1** 250**		280		250	µA
				24** 38††**		45††		38††	mA
				0.5** 250**		280		250	µA
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
				250**		280		250	µA
				1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			4					pF
C _o	V _O = 2.5 V or 0.5 V			7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** These limits apply only to the SN74ABT841A.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

†† This limit may vary among suppliers.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT841		SN74ABT841A		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
t _w	Pulse duration, LE high or low			3.3		3.3		3.3	ns
t _{su}	Setup time, data before LE↓		High	2.5		2.5		2.5	ns
			Low	1.5		1.5		1.5	
t _h	Hold time, data after LE↓		High	1.5		1.5		1.5	ns
			Low	1.5		2		1.5	



SN54ABT841, SN74ABT841A
10-BIT BUS-INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS196D – FEBRUARY 1991 – REVISED MAY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT841				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	D	Q	1†	4.1	5.5	1†	6.8	ns
t_{PHL}			1.5†	4	5.5	1.5†	6.8	
t_{PLH}	LE	Q	1.6†	4.1	6.6†	1.6†	7.4	ns
t_{PHL}			2†	4.6	6.2	2†	6.8	
t_{PZH}	\overline{OE}	Q	1	3	4.9†	1	5.8	ns
t_{PZL}			2.2	4.1	5.7†	2.2	6.5	
t_{PHZ}	\overline{OE}	Q	2†	4.7	6.2	2†	7.2	ns
t_{PLZ}			1.5†	4.6	6.1	1.5†	6.6	

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT841A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.4†	4.1	5.5	1.4†	6.2†	ns
t_{PHL}			1.5†	4	5.5	1.5†	6.2	
t_{PLH}	LE	Q	2.1†	4.1	5.9†	2.1†	6.5†	ns
t_{PHL}			2.4†	4.6	6.2	2.4†	6.7	
t_{PZH}	\overline{OE}	Q	1	3	4.7†	1	5.3†	ns
t_{PZL}			2.2	4.1	5.7†	2.2	6.3†	
t_{PHZ}	\overline{OE}	Q	2.6†	4.7	6.2	2.6†	7.1	ns
t_{PLZ}			1.9†	4.6	6.1	1.9†	6.5	

† This data sheet limit may vary among suppliers.

SN54ABT841, SN74ABT841A 10-BIT BUS-INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS196D – FEBRUARY 1991 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION

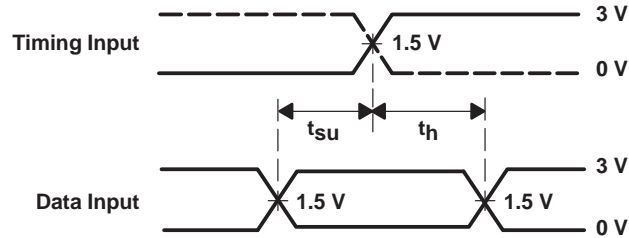


LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9676901Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9676901QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9676901QLA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74ABT841ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT841ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT841ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT841ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN74ABT841ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ANSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT841ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT841APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841APWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74ABT841APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT841APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT841FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ABT841JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ABT841W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT841ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT841ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT841ANSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1
SN74ABT841APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT841ADBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74ABT841ADWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74ABT841ANSR	SO	NS	24	2000	346.0	346.0	41.0
SN74ABT841APWR	TSSOP	PW	24	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

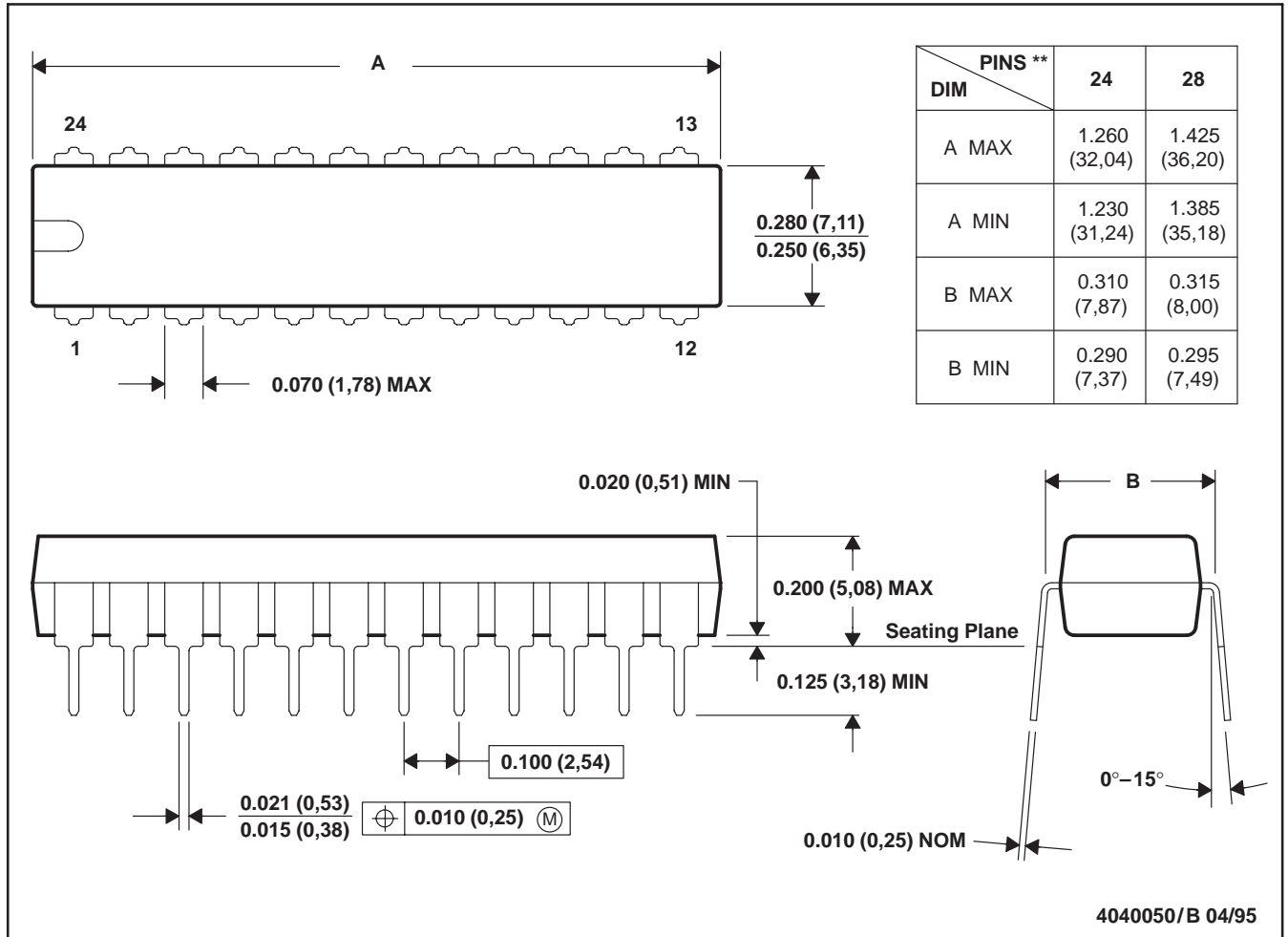


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

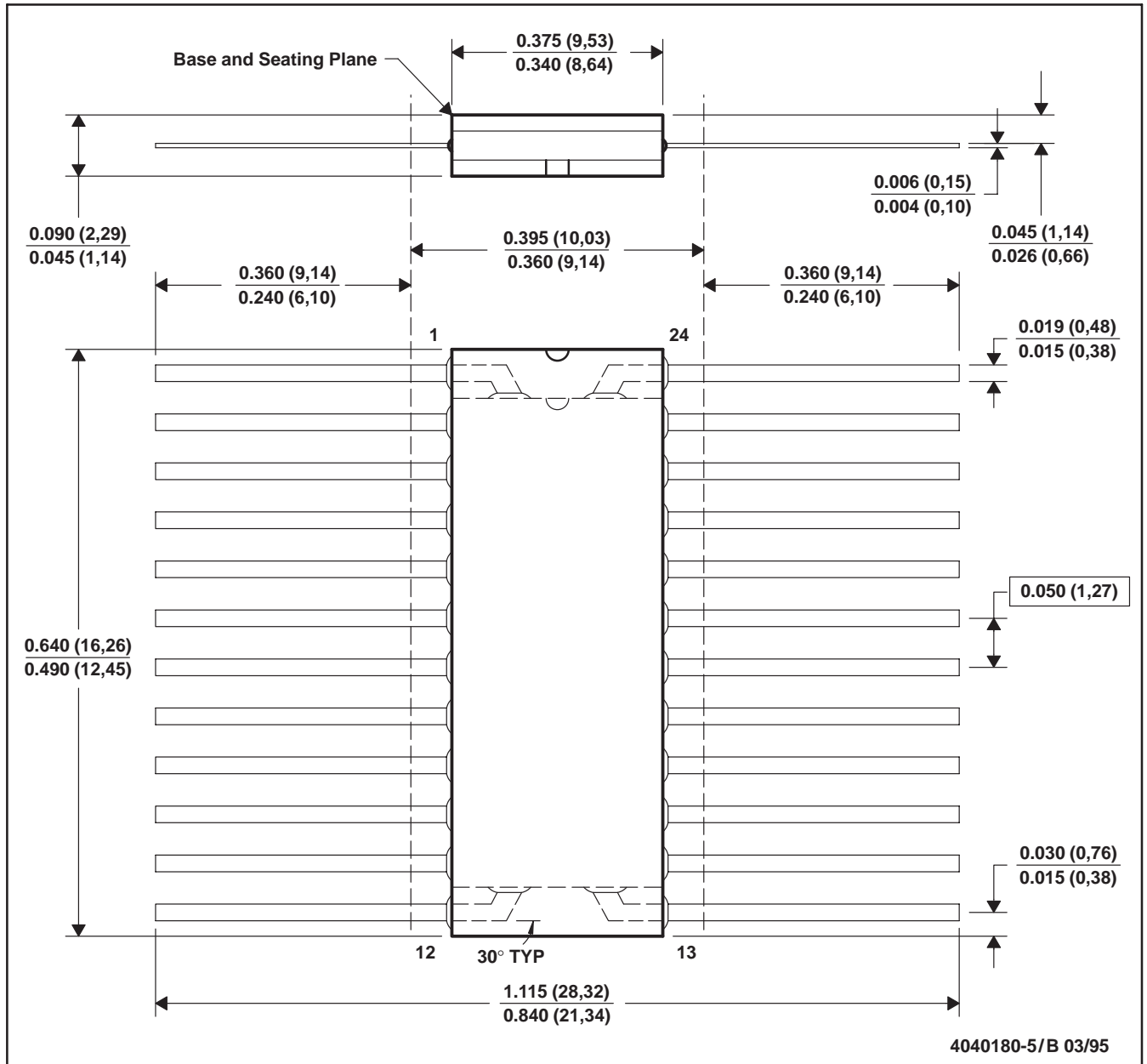
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

W (R-GDFP-F24)

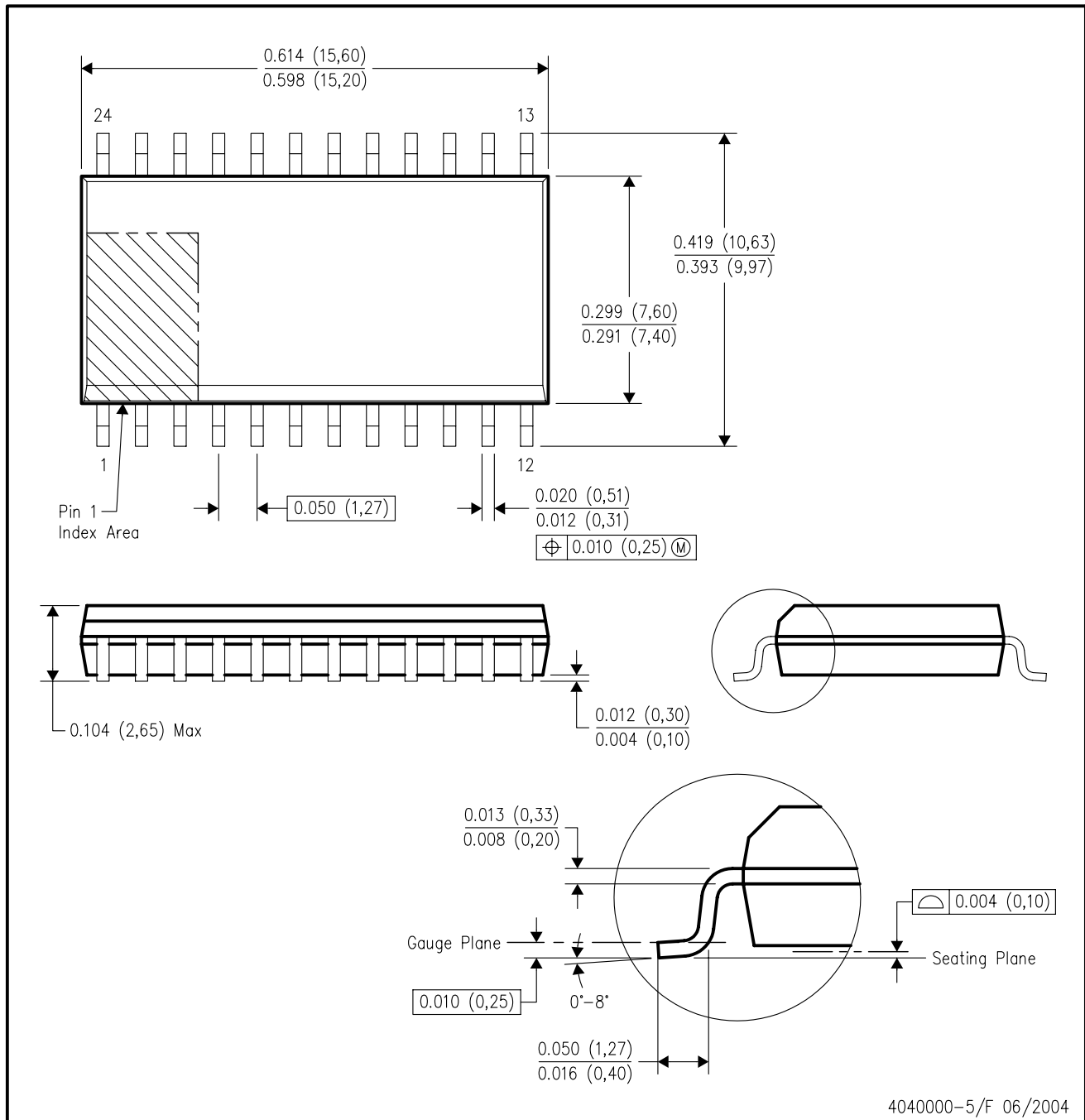
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - Index point is provided on cap for terminal identification only.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated