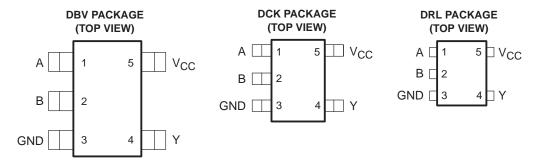
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- Operating Range of 2 V to 5.5 V
- Max t<sub>pd</sub> of 6.5 ns at 5 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±8-mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## description/ordering information

The SN74AHC1G00 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### **ORDERING INFORMATION**

TA	PACKAGE	<u></u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	00T (00T 00)	Reel of 3000	SN74AHC1G00DBVR	400
	SOT (SOT-23) – DBV	Reel of 250	SN74AHC1G00DBVT	A00_
	00T (00 70) DOV	Reel of 3000	SN74AHC1G00DCKR	Δ Δ
	SOT (SC-70) – DCK	Reel of 250	SN74AHC1G00DCKT	AA_
	SOT (SOT-553) – DRL	Reel of 4000	SN74AHC1G00DRLR	AA_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

	INP	UTS	OUTPUT
	Α	В	Υ
Γ	Н	Н	L
l	L	X	Н
	Χ	L	Н

### logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DBV package	206°C/W
DCK package	252°C/W
DRL package	142°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage VCC = 3 V			0.9	V
		V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
lOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	A
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA
		V <sub>CC</sub> = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A
		$V_{CC} = 5 V \pm 0.5 V$		8	mA
44/4		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$	20		ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

242445752	T-01 00UDITIOUS	.,	T,	ղ = 25°C	;			
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
		2 V	1.9	2		1.9		
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		
Voн		4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	$I_{OL} = 50 \mu A$	3 V			0.1		0.1	
V <sub>OL</sub>		4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
lį	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Ci	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T	չ = 25°C	;	MAINI	BA A V	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	A - :: D	V	0 455		5.5	7.9	1	9.5	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF		5.5	7.9	1	9.5	ns
<sup>t</sup> PLH	A or B	V	C: - 50 pF		8	11.4	1	13	20
t <sub>PHL</sub>	AUID	ſ	C <sub>L</sub> = 50 pF		8	11.4	1	13	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

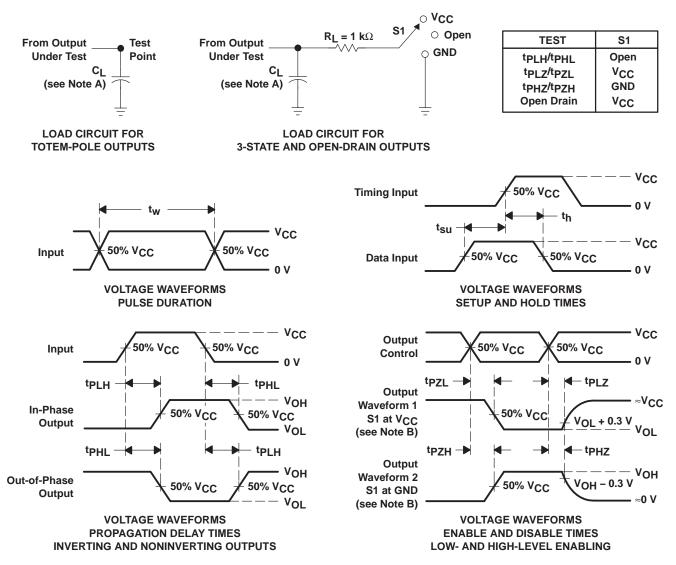
DADAMETED	FROM	то	LOAD	T,	գ = 25°C	С	BAINI	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	IVIAA	UNII
t <sub>PLH</sub>	A == D	V	0. 45.55		3.7	5.5	1	6.5	
t <sub>PHL</sub>	A or B	Y	C <sub>L</sub> = 15 pF		3.7	5.5	1	6.5	ns
tPLH	A or B	V	C: - 50 pF		5.2	7.5	1	8.5	20
<sup>t</sup> PHL	AUIB	r	C <sub>L</sub> = 50 pF		5.2	7.5	1	8.5	ns

## operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	9.5	pF



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHC1G00DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC1G00DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is



## **PACKAGE OPTION ADDENDUM**

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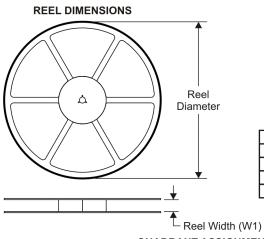
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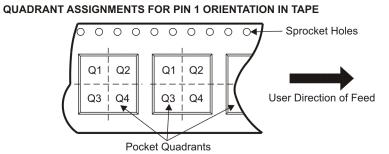
### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

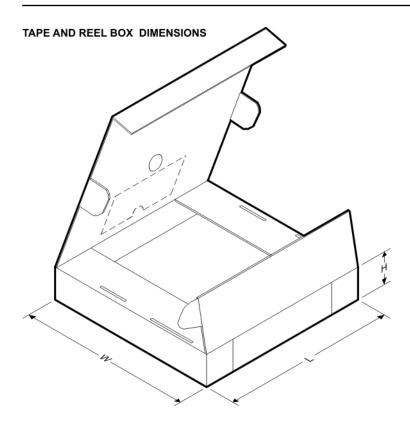
— Reel Width (WT)



\*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3



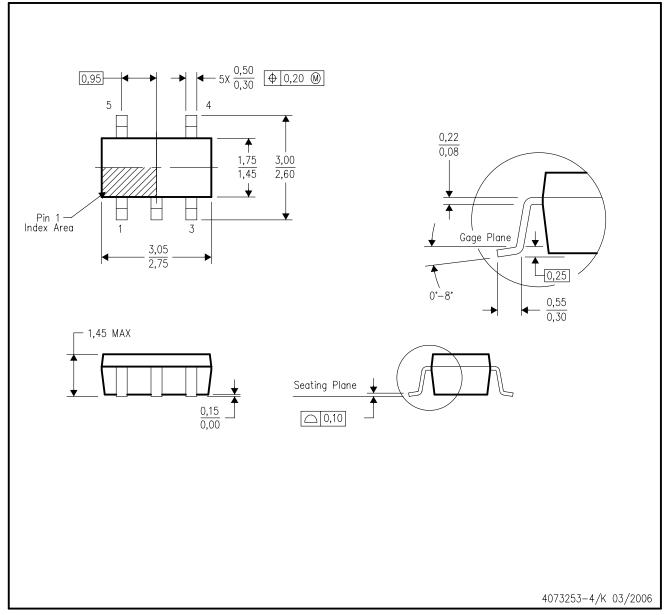


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74AHC1G00DBVT	SOT-23	DBV	5	250	201.0	192.0	26.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DCKT	SC70	DCK	5	250	201.0	192.0	26.0
SN74AHC1G00DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

## DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



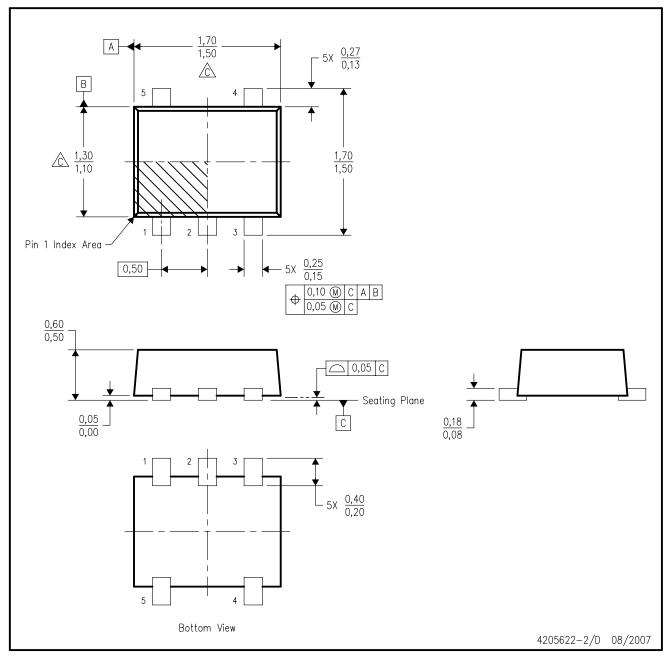
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



## DRL (R-PDSO-N5)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

  Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



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