

# SN74ALB16244

## 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS647D – AUGUST 1995 – REVISED JANUARY 2001

- Member of Texas Instruments' Widebus™ Family
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot
- Industry Standard '16244 Pinout
- Distributed V<sub>CC</sub> and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout

### description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V<sub>CC</sub> operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity-gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

### DGG, DGV, OR DL PACKAGE (TOP VIEW)

$\overline{1OE}$	1	48	$\overline{2OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V <sub>CC</sub>	7	42	V <sub>CC</sub>
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V <sub>CC</sub>	18	31	V <sub>CC</sub>
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
$\overline{4OE}$	24	25	$\overline{3OE}$

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74ALB16244DL	ALB16244
		Tape and reel	SN74ALB16244DLR	
	TSSOP – DGG	Tape and reel	SN74ALB16244DGGR	ALB16244
	TVSOP – DGV	Tape and reel	SN74ALB16244DGVR	AV244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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$\overline{1OE}$	1	EN1		
$\overline{2OE}$	48	EN2		
$\overline{3OE}$	25	EN3		
$\overline{4OE}$	24	EN4		
1A1	47	1	1 ▽	2 1Y1
1A2	46			3 1Y2
1A3	44			5 1Y3
1A4	43			6 1Y4
2A1	41	1	2 ▽	8 2Y1
2A2	40			9 2Y2
2A3	38			11 2Y3
2A4	37			12 2Y4
3A1	36	1	3 ▽	13 3Y1
3A2	35			14 3Y2
3A3	33			16 3Y3
3A4	32			17 3Y4
4A1	30	1	4 ▽	19 4Y1
4A2	29			20 4Y2
4A3	27			22 4Y3
4A4	26			23 4Y4



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The image contains two logic diagrams for 3-to-8 line decoders. The left diagram is for the 74VHC161, which has an active-low enable input  $\overline{1OE}$  (pin 1) and four data inputs (1A1, 1A2, 1A3, 1A4) at pins 47, 46, 44, and 43. It has eight outputs (1Y1 to 1Y4) at pins 2, 3, 5, and 6. The right diagram is for the 74VHC162, which has an active-low enable input  $\overline{3OE}$  (pin 25) and four data inputs (3A1, 3A2, 3A3, 3A4) at pins 36, 35, 33, and 32. It has eight outputs (3Y1 to 3Y4) at pins 13, 14, 16, and 17. Both diagrams show the internal structure of the decoders, including inverters and AND gates.

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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## 16-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	3	3.6	V
$I_{OH}^{\dagger}$	High-level output current		–25	mA
$I_{OL}^{\dagger}$	Low-level output current		25	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

<sup>†</sup> See Figures 1 and 2 for typical I/O ranges.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V <sub>IK</sub>	Data inputs	V <sub>CC</sub> = 3 V	I <sub>I</sub> = 18 mA		3.6		V <sub>CC</sub> –1.2	V
			I <sub>I</sub> = –18 mA		–0.9    –1.2			
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V,    V <sub>I</sub> = V <sub>CC</sub> or GND			±10		μA	
	Data inputs	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = V <sub>CC</sub>	$\overline{OE}$ low	0.4	0.6	mA	
				$\overline{OE}$ high	25		μA	
			V <sub>I</sub> = 0	$\overline{OE}$ low	–0.8	–1	mA	
				$\overline{OE}$ high	–60		μA	
I <sub>OZH</sub>		V <sub>CC</sub> = 3.6 V,    V <sub>O</sub> = 3 V			0.6	20	μA	
I <sub>OZL</sub>		V <sub>CC</sub> = 3.6 V,    V <sub>O</sub> = 0.5 V			–0.1	–50	μA	
I <sub>CC</sub> /buffer		V <sub>CC</sub> = 3.6 V,    I <sub>O</sub> = 0,    V <sub>I</sub> = V <sub>CC</sub> or GND			3.7	5.6	mA	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6 V,    Control inputs = V <sub>CC</sub> or GND			0.8		mA	
ΔI <sub>CC</sub> §		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> –0.6 V, Other inputs at V <sub>CC</sub> or GND			600		μA	
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0			4.5		pF	
C <sub>O</sub>		V <sub>O</sub> = 3 V or 0			5.5		pF	

<sup>‡</sup> All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

#### switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			UNIT
			MIN	TYP <sup>‡</sup>	MAX	
$t_{pd}$	A	Y	0.6	1.3	2	ns
$t_{en}$	$\overline{OE}$	Y	1.3	2.5	4.7	ns
$t_{dis}$	$\overline{OE}$	Y	1.8	2.8	4.2	ns

<sup>‡</sup> All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



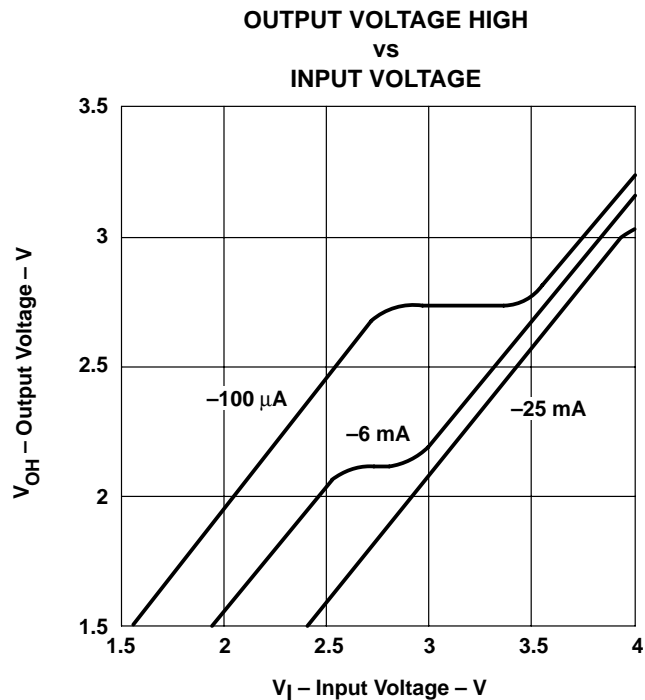


Figure 1.  $V_{OH}$  Over Recommended Free-Air Temperature Range

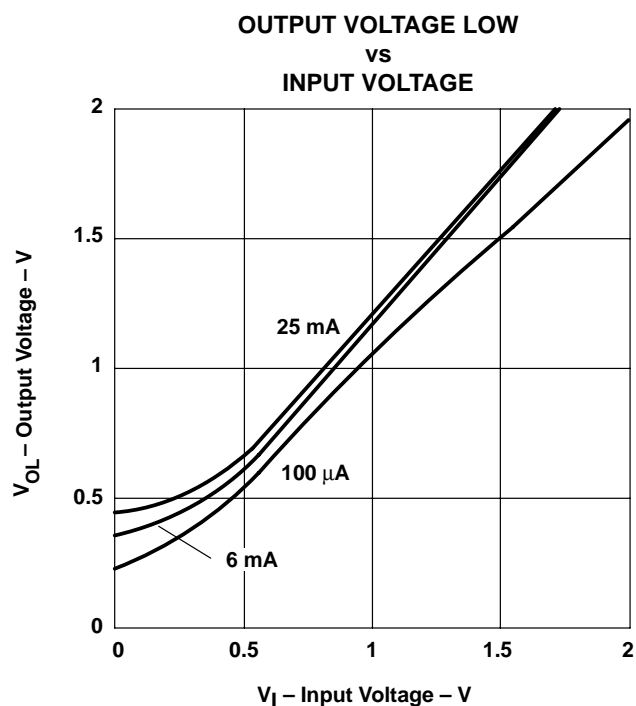


Figure 2.  $V_{OL}$  Over Recommended Free-Air Temperature Range

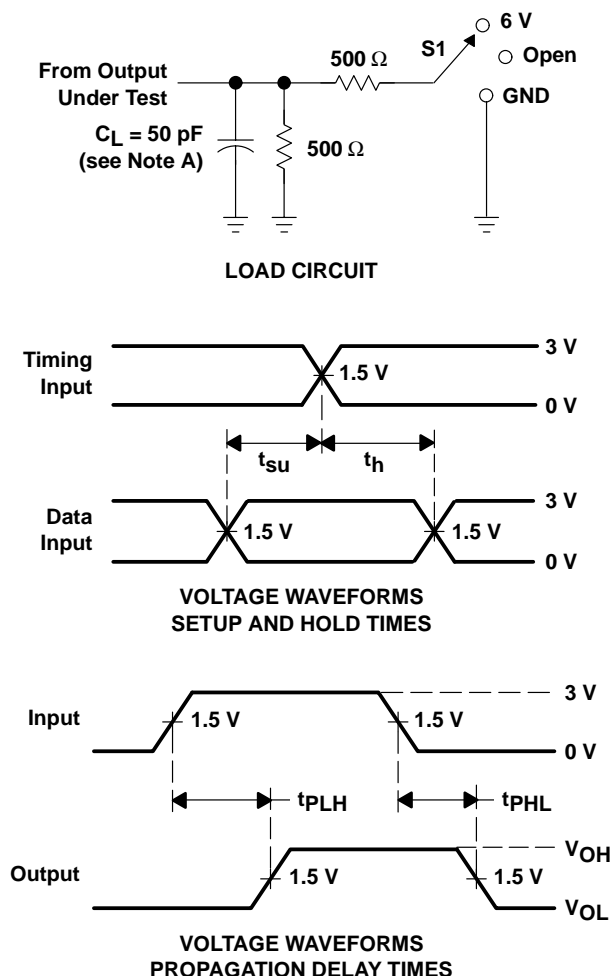
# SN74ALB16244

## 16-BIT BUFFER/DRIVER

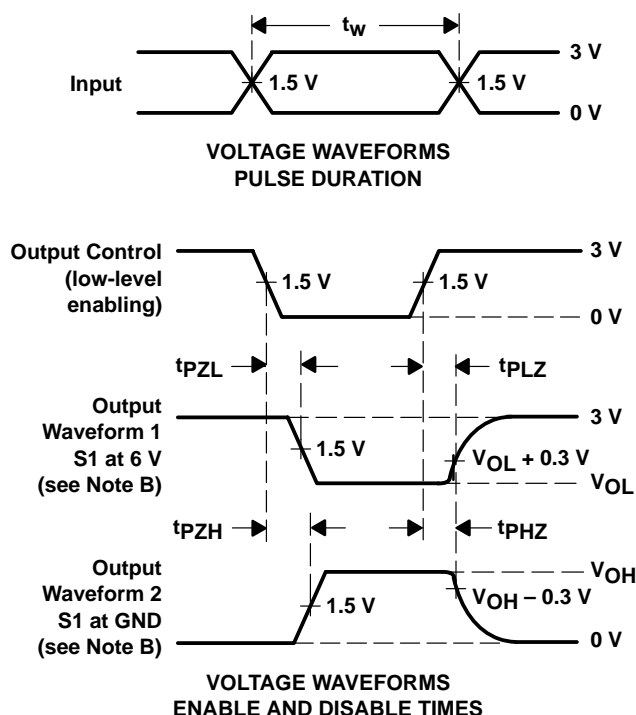
### WITH 3-STATE OUTPUTS

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#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ALB16244DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALB16244DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALB16244DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALB16244DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16244DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALB16244DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALB16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALB16244DGVR	TVSOP	DGV	48	2000	330.0	24.4	6.8	10.1	1.6	12.0	24.0	Q1
SN74ALB16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALB16244DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ALB16244DGVR	TVSOP	DGV	48	2000	346.0	346.0	41.0
SN74ALB16244DLR	SSOP	DL	48	1000	346.0	346.0	49.0

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

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