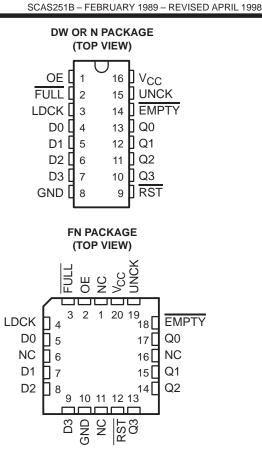
- Independent Asynchronous Inputs and Outputs
- 16 Words by 4 Bits
- Data Rates up to 40 MHz
- Fall-Through Time 14 ns Typical
- 3-State Outputs
- Package Options Include Plastic Small-Outline Package (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)

description

This 64-bit memory features high speed and fast fall-through times. It is organized as 16 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates up to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.



NC - No internal connection

Status of the FIFO memory is monitored by the FULL and EMPTY output flags. The FULL output is low when the memory is full and high when it is not full. The EMPTY output is low when the memory is empty and high when it is not empty.

A low level on the reset (RST) input resets the internal stack-control pointers and also sets EMPTY low and sets FULL high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a RST pulse or from an empty condition, causes EMPTY to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the FULL or EMPTY output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS232B is characterized for operation from 0°C to 70°C.



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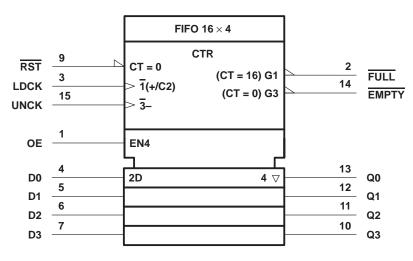
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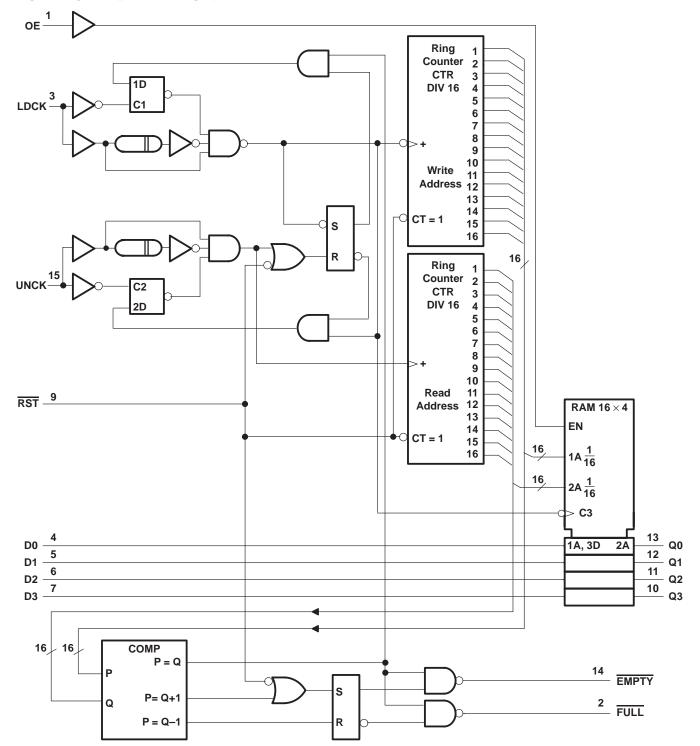
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0. Pin numbers shown are for the DW and N packages.



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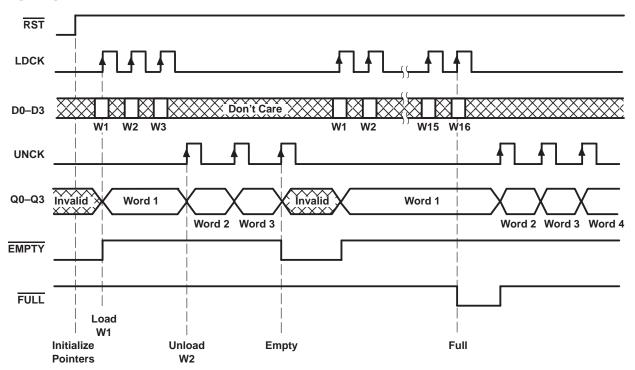
logic diagram (positive logic)

Pin numbers shown are for the DW and N packages.



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timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}		
Voltage range applied to a disabled 3-state outp		
Package thermal impedance, θ_{JA} (see Note 2):	DW package	105°C/W
	FN package	83°C/W
	N package	78°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

 [†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to GND.

2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	V	
VIH	VIH High-level input voltage					V
VIL	Low-level input voltage				0.8	V
		Q outputs			-2.6	mA
ЮН	High-level output current	FULL, EMPTY			-0.4	ША
	Low-level output current	Q outputs			24	mA
IOL		FULL, EMPTY			8	ША
TA	Operating free-air temperature		0		70	°C

NOTE 3: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum V_{IL}, minimum V_{IH}, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TES	TEST CONDITIONS				
VIK		$V_{CC} = 4.5 V,$	lı = -18 mA		-1.2	V	
∨он	Q outputs	$V_{CC} = 4.5 V,$	I _{OH} = -2.6 mA	2.4 3.2		V	
VОН	FULL, EMPTY	V_{CC} = 4.5 V to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2		v	
	Q outputs		I _{OL} = 12 mA	0.25	0.4		
Vei	Q Oulpuis	outputs V _{CC} = 4.5 V I _{OL} = 24 mA	0.35	0.5	v		
VOL	FULL, EMPTY $V_{CC} = 4.5 V$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	v		
		$v_{CC} = 4.5 v$	I _{OL} = 8 mA	0.35	0.5		
IOZH		V _{CC} = 5.5 V,	V _O = 2.7 V		20	μA	
IOZL		V _{CC} = 5.5 V,	V _O = 0.4 V		-20	μA	
Ц		V _{CC} = 5.5 V,	V _I = 7 V		0.1	mA	
ЧΗ		V _{CC} = 5.5 V,	V _I = 2.7 V		20	μA	
ΙL		V _{CC} = 5.5 V,	V _I = 0.4 V		-0.2	mA	
10 [‡]		V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-112	mA	
Icc		V _{CC} = 5.5 V		80	125	mA	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, IOS.



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timing requirements over recommended operating free-air temperature range (see Figure 1)

		-	MIN	NOM	MAX	UNIT	
4 +	Clock frequency	LDCK			40	MHz	
^f clock [†]	Clock nequency	UNCK			40		
		RST low	18				
		LDCK low	15				
tw	Pulse duration	LDCK high	10			ns	
		UNCK low	15				
		UNCK high	10				
+	Setup time	Data before LDCK↑	8			ns	
t _{su} Setup time	Setup time	LDCK inactive before RST↑	5			115	
t _h	Hold time	Data after LDCK↑	5			ns	
		LDCK inactive after RST [↑]	5			115	

[†] The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

switching characteristics (see Figure 1)

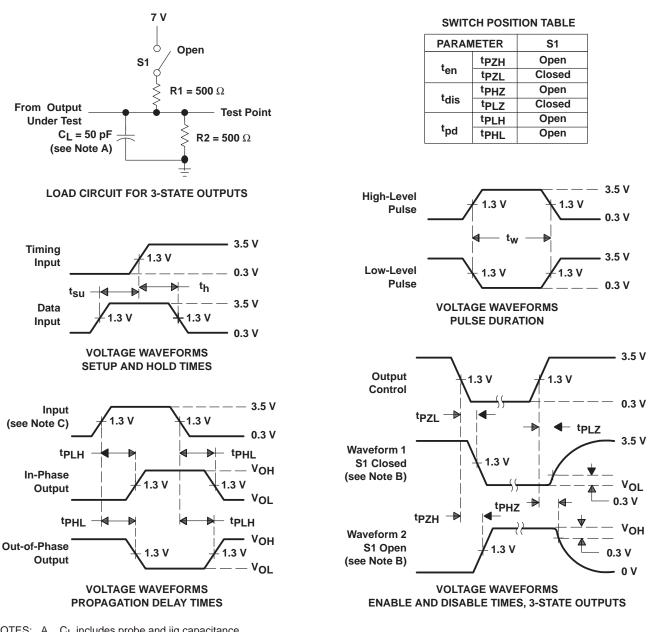
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN TYP‡	MAX	MIN	MAX	UNIT
fmax	LDCK, UNCK		50		40		MHz
. .	LDCK↑	Any 0	14	23	6	30	ns
^t pd	UNCK↑	Any Q	15	23	6	30	
^t PLH	LDCK [↑]	EMPTY	13	20	5	25	ns
	UNCK↑		15	22	6	27	ns
^t PHL	RST↓	EMPTY	15	21	5	26	
	LDCK↑	FULL	15	22	6	27	
t =	UNCK↑		13	20	5	25	
^t PLH	RST↓	FULL	16	23	7	28	ns
ten	OE↑	Q	5	12	1	14	ns
^t dis	OE↓	Q	5	12	1	16	ns

[‡] Typical values at V_{CC} – 5 V, T_A = 25°C.



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z₀ = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS232BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS232BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS232BFN	ACTIVE	PLCC	FN	20	46	TBD	CU SNPB	Level-1-220C-UNLIM
SN74ALS232BFNR	ACTIVE	PLCC	FN	20	1000	TBD	CU SNPB	Level-1-220C-UNLIM
SN74ALS232BN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



MECHANICAL DATA

MPLC004A - OCTOBER 1994

PLASTIC J-LEADED CHIP CARRIER

FN (S-PQCC-J**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-018



DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AA.



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