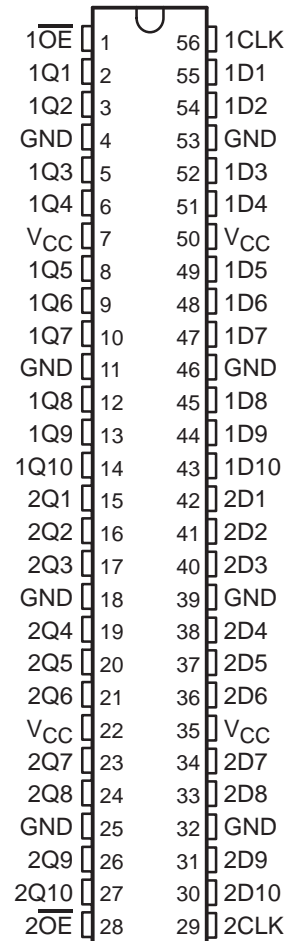


# SN54ALVTH16821, SN74ALVTH16821 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- High-Drive (–24/24 mA at 2.5-V and –32/64 mA at 3.3-V  $V_{CC}$ )
- Power Off Disables Outputs, Permitting Live Insertion
- High-Impedance State During Power Up and Power Down Prevents Driver Conflict
- Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds  $V_{CC} + 0.5$  V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

SN54ALVTH16821 . . . WD PACKAGE  
SN74ALVTH16821 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description

The 'ALVTH16821 devices are 20-bit bus-interface flip-flops with 3-state outputs designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20-bit flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK), the flip-flops store the logic levels set up at the D inputs.



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# SN54ALVTH16821, SN74ALVTH16821

## 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### description (continued)

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH16821 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALVTH16821 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

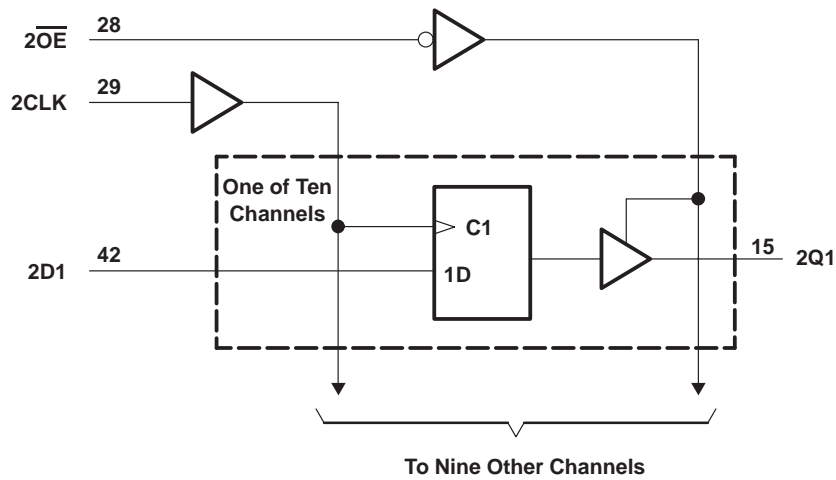
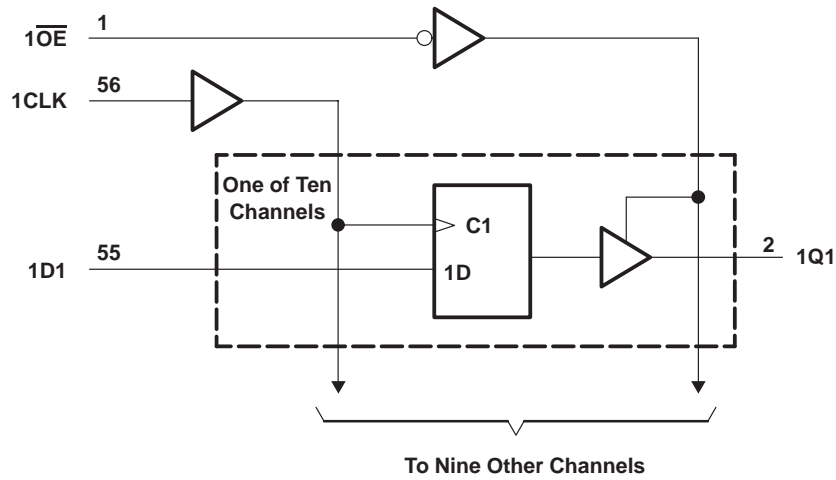
FUNCTION TABLE  
(each 10-bit section)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

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logic diagram (positive logic)



# SN54ALVTH16821, SN74ALVTH16821

## 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output current in the low state, $I_O$ : SN54ALVTH16821 .....	96 mA
SN74ALVTH16821 .....	128 mA
Output current in the high state, $I_O$ : SN54ALVTH16821 .....	-48 mA
SN74ALVTH16821 .....	-64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	81°C/W
DGV package .....	86°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Note 3)

		SN54ALVTH16821			SN74ALVTH16821			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	2.3		2.7	2.3		2.7	V
$V_{IH}$	High-level input voltage	1.7			1.7			V
$V_{IL}$	Low-level input voltage			0.7			0.7	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current			-6			-8	mA
$I_{OL}$	Low-level output current			6			8	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$			18			24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**WITH 3-STATE OUTPUTS**

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**recommended operating conditions,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (see Note 3)**

		SN54ALVTH16821			SN74ALVTH16821			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	3		3.6	3		3.6	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0	$V_{CC}$	5.5	0	$V_{CC}$	5.5	V
$I_{OH}$	High-level output current			-24			-32	mA
$I_{OL}$	Low-level output current			24			32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$			48			64	
$\Delta t/\Delta v$	Input transition rise or fall rate			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200			200			$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55		125	-40		85	$^{\circ}\text{C}$

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54ALVTH16821, SN74ALVTH16821

## 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	TEST CONDITIONS		SN54ALVTH16821		SN74ALVTH16821		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 2.3\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V
$V_{OH}$	$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
	$V_{CC} = 2.3\text{ V}$	$I_{OH} = -6\text{ mA}$	1.8		1.8		
$V_{OL}$	$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.3\text{ V}$	$I_{OL} = 6\text{ mA}$	0.4				
		$I_{OL} = 8\text{ mA}$			0.4		
		$I_{OL} = 18\text{ mA}$	0.5				
$I_I$	Control inputs	$V_{CC} = 2.7\text{ V}$ , $V_I = V_{CC}$ or GND	$\pm 1$		$\pm 1$		$\mu\text{A}$
		$V_{CC} = 0$ or $2.7\text{ V}$ , $V_I = 5.5\text{ V}$	10		10		
	Data inputs	$V_{CC} = 2.7\text{ V}$ , $V_I = 5.5\text{ V}$	10		10		
		$V_{CC} = 2.7\text{ V}$ , $V_I = V_{CC}$	1		1		
		$V_I = 0$	-5		-5		
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$
$I_{BHL}^\ddagger$	$V_{CC} = 2.3\text{ V}$ , $V_I = 0.7\text{ V}$		115		115		$\mu\text{A}$
$I_{BHH}^\S$	$V_{CC} = 2.3\text{ V}$ , $V_I = 1.7\text{ V}$		-10		-10		$\mu\text{A}$
$I_{BHLO}^\P$	$V_{CC} = 2.7\text{ V}$ , $V_I = 0$ to $V_{CC}$		300		300		$\mu\text{A}$
$I_{BHHO}^\#$	$V_{CC} = 2.7\text{ V}$ , $V_I = 0$ to $V_{CC}$		-300		-300		$\mu\text{A}$
$I_{EX}^\parallel$	$V_{CC} = 2.3\text{ V}$ , $V_O = 5.5\text{ V}$		125		125		$\mu\text{A}$
$I_{OZ(PU/PD)}^\star$	$V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 2.7\text{ V}$	$V_O = 2.3\text{ V}$ , $V_I = 0.7\text{ V or } 1.7\text{ V}$	5		5		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 2.7\text{ V}$	$V_O = 0.5\text{ V}$ , $V_I = 0.7\text{ V or } 1.7\text{ V}$	-5		-5		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 2.7\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high	0.04	0.1	0.04	0.1	mA
		Outputs low	2.3	4.5	2.3	4.5	
		Outputs disabled	0.04	0.1	0.04	0.1	
$C_i$	$V_{CC} = 2.5\text{ V}$ , $V_I = 2.5\text{ V or } 0$		3.5		3.5		pF
$C_o$	$V_{CC} = 2.5\text{ V}$ , $V_O = 2.5\text{ V or } 0$		6.5		6.5		pF

† All typical values are at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

\* High-impedance state during power up or power down

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**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54ALVTH16821		SN74ALVTH16821		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$		$V_{CC} = 3 \text{ V}$ , $I_I = -18 \text{ mA}$	-1.2		-1.2		V	
$V_{OH}$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$		$V_{CC}-0.2$		V	
		$V_{CC} = 3 \text{ V}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$	2		2			
$V_{OL}$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $I_{OL} = 100 \mu\text{A}$	0.2		0.2		V	
		$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$			0.4		
			$I_{OL} = 24 \text{ mA}$	0.5				
			$I_{OL} = 32 \text{ mA}$			0.5		
			$I_{OL} = 48 \text{ mA}$ $I_{OL} = 64 \text{ mA}$	0.55		0.55		
$I_I$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$	$\pm 1$		$\pm 1$		$\mu\text{A}$	
		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$	10		10			
	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$	10		10		
			$V_I = V_{CC}$ $V_I = 0$	1 -5		1 -5		
$I_{off}$		$V_{CC} = 0$ , $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$			$\pm 100$		$\mu\text{A}$	
$I_{BHL}^\ddagger$		$V_{CC} = 3 \text{ V}$ , $V_I = 0.8 \text{ V}$	75		75		$\mu\text{A}$	
$I_{BHH}^\S$		$V_{CC} = 3 \text{ V}$ , $V_I = 2 \text{ V}$	-75		-75		$\mu\text{A}$	
$I_{BHLO}^\P$		$V_{CC} = 3.6 \text{ V}$ , $V_I = 0 \text{ to } V_{CC}$	500		500		$\mu\text{A}$	
$I_{BHHO}^\#$		$V_{CC} = 3.6 \text{ V}$ , $V_I = 0 \text{ to } V_{CC}$	-500		-500		$\mu\text{A}$	
$I_{EX}^\parallel$		$V_{CC} = 3 \text{ V}$ , $V_O = 5.5 \text{ V}$	125		125		$\mu\text{A}$	
$I_{OZ(PU/PD)}^\star$		$V_{CC} \leq 1.2 \text{ V}$ , $V_O = 0.5 \text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$	$\pm 100$		$\pm 100$		$\mu\text{A}$	
$I_{OZH}$		$V_{CC} = 3.6 \text{ V}$ $V_O = 3 \text{ V}$ , $V_I = 0.8 \text{ V or } 2 \text{ V}$	5		5		$\mu\text{A}$	
$I_{OZL}$		$V_{CC} = 3.6 \text{ V}$ $V_O = 0.5 \text{ V}$ , $V_I = 0.8 \text{ V or } 2 \text{ V}$	-5		-5		$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC} \text{ or GND}$	Outputs high	0.07	0.1	0.07	0.1	mA
			Outputs low	3.2	5.5	3.2	5	
			Outputs disabled	0.07	0.1	0.07	0.1	
$\Delta I_{CC}^\square$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC} \text{ or GND}$	0.4		0.4		mA	
$C_i$		$V_{CC} = 3.3 \text{ V}$ , $V_I = 3.3 \text{ V or } 0$	3.5		3.5		pF	
$C_o$		$V_{CC} = 3.3 \text{ V}$ , $V_O = 3.3 \text{ V or } 0$	6		6		pF	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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**WITH 3-STATE OUTPUTS**

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5 V \pm 0.2 V$  (unless otherwise noted) (see Figure 1)**

		SN54ALVTH16821		SN74ALVTH16821		UNIT
		MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency	150		150		MHz
$t_w$	Pulse duration, CLK high or low	1.6		1.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	Data high	1.6	1.5		ns
		Data low	2.1	2		
$t_h$	Hold time, data after CLK $\uparrow$	Data high	0.4	0.3		ns
		Data low	1.1	1		

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 2)**

		SN54ALVTH16821		SN74ALVTH16821		UNIT
		MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency	150		150		MHz
$t_w$	Pulse duration, CLK high or low	1.6		1.5		ns
$t_{su}$	Setup time, data before CLK $\uparrow$	Data high	1.6	1.5		ns
		Data low	1.6	1.5		
$t_h$	Hold time, data after CLK $\uparrow$	Data high	1.1	1		ns
		Data low	1.1	1		

**switching characteristics over recommended operating free-air temperature range,  $C_L = 30 pF$ ,  $V_{CC} = 2.5 V \pm 0.2 V$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16821		SN74ALVTH16821		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			150		150		MHz
$t_{PLH}$	CLK	Q	1	4.2	1	4.1	ns
$t_{PHL}$			1	4.5	1	4.4	
$t_{PZH}$	$\overline{OE}$	Q	1.5	4.7	1.5	4.6	ns
$t_{PZL}$			1	4.2	1	4.1	
$t_{PHZ}$	$\overline{OE}$	Q	1.5	4.6	1.5	4.5	ns
$t_{PLZ}$			1	5	1	4.9	

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 pF$ ,  $V_{CC} = 3.3 V \pm 0.3 V$  (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH16821		SN74ALVTH16821		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			150		150		MHz
$t_{PLH}$	CLK	Q	1	3.6	1	3.5	ns
$t_{PHL}$			1	3.6	1	3.5	
$t_{PZH}$	$\overline{OE}$	Q	1	4.2	1	4.1	ns
$t_{PZL}$			1	3.7	1	3.6	
$t_{PHZ}$	$\overline{OE}$	Q	1	4.9	1	4.8	ns
$t_{PLZ}$			1	4.8	1	4.6	

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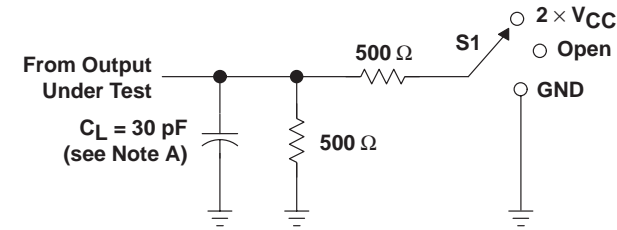


# SN54ALVTH16821, SN74ALVTH16821 2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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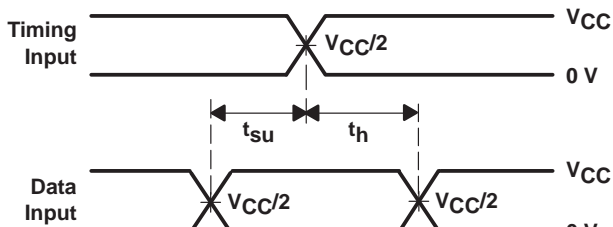
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

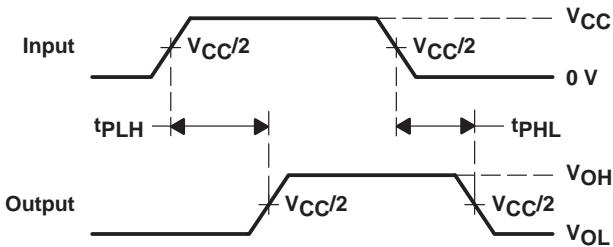


LOAD CIRCUIT

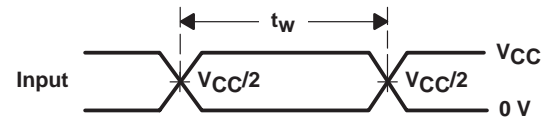
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



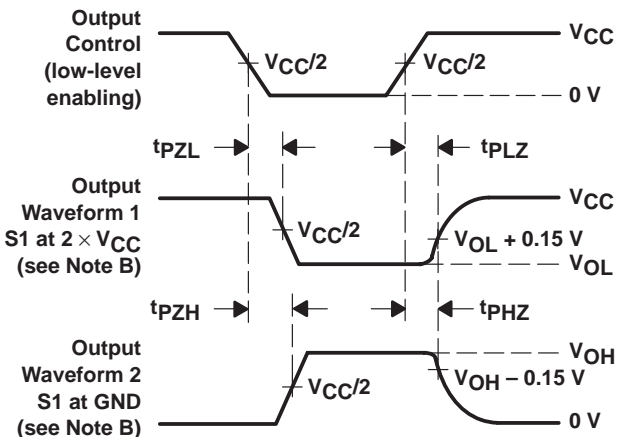
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

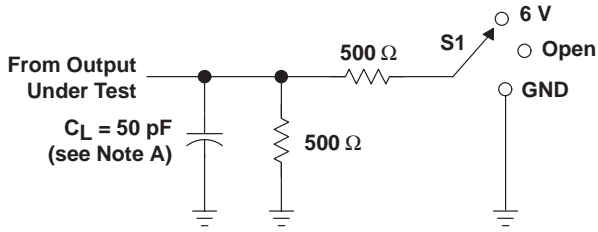
Figure 1. Load Circuit and Voltage Waveforms

**SN54ALVTH16821, SN74ALVTH16821**  
**2.5-V/3.3-V 20-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

SCES078E – JULY 1996 – REVISED JANUARY 1999

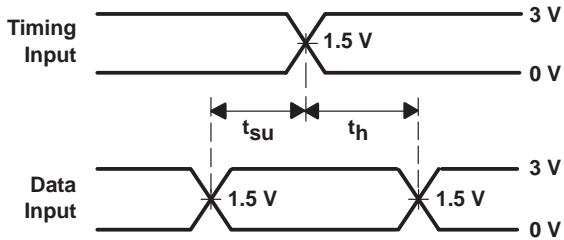
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

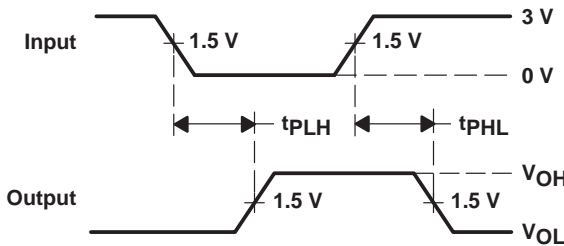


**LOAD CIRCUIT**

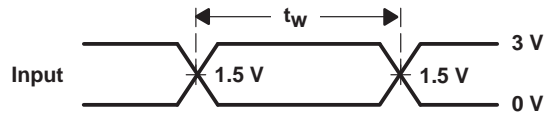
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



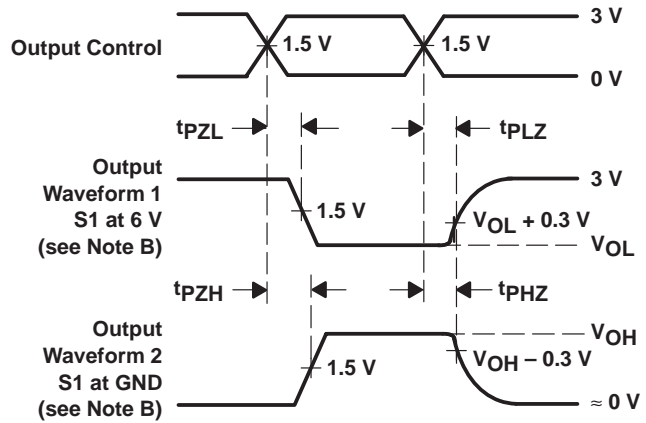
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ALVTH16821DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16821DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16821GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16821GRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16821VRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVTH16821VRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16821DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16821DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16821GR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVTH16821VR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

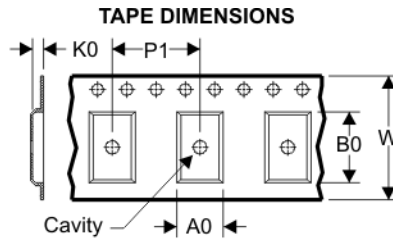
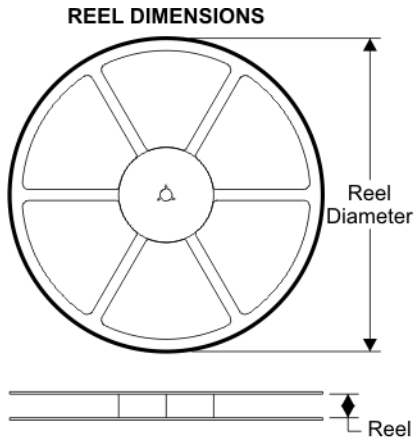
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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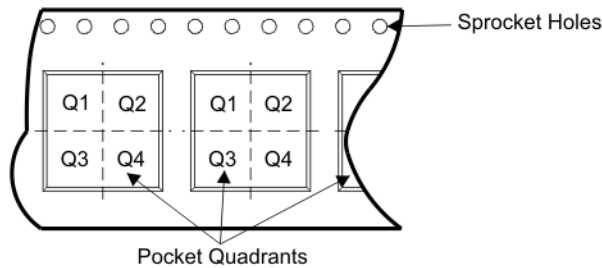
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**TAPE AND REEL BOX INFORMATION**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVTH16821DLR	DL	56	SITE 41	330	32	11.35	18.67	3.1	16	32	Q1
SN74ALVTH16821GR	DGG	56	SITE 41	330	24	8.6	15.6	1.8	12	24	Q1
SN74ALVTH16821VR	DGV	56	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1

**TAPE AND REEL BOX DIMENSIONS**



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALVTH16821DLR	DL	56	SITE 41	346.0	346.0	0.0
SN74ALVTH16821GR	DGG	56	SITE 41	346.0	346.0	0.0
SN74ALVTH16821VR	DGV	56	SITE 41	346.0	346.0	0.0

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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