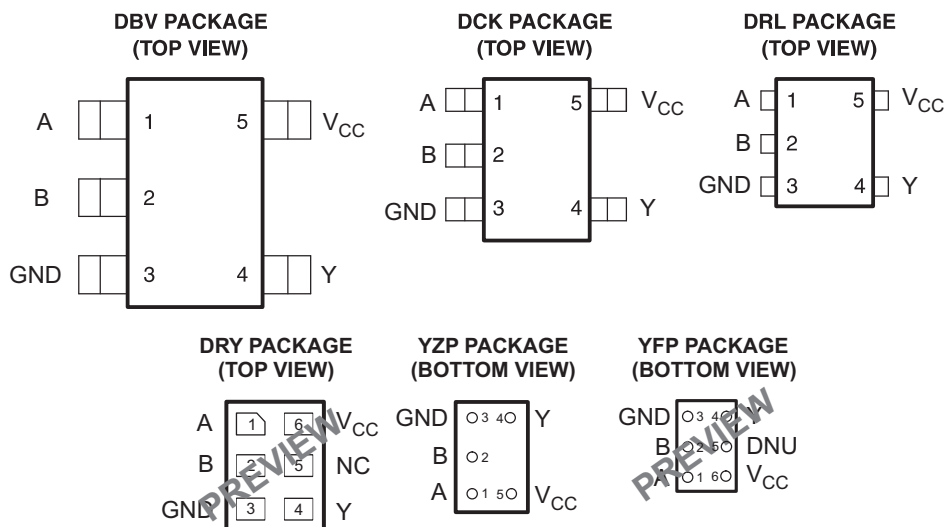


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu A$ Max)
- Low Dynamic-Power Consumption ($C_{pd} = 4.3$ pF Typ at 3.3 V)
- Low Input Capacitance ($C_i = 1.5$ pF Typ)
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching-Noise Immunity at the Input ($V_{hys} = 250$ mV Typ at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.5$ ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds ± 5000 V With Human-Body Model



See mechanical drawings for dimensions.
NC - No internal connection
DNU - Do not use

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see Figure 2).

This single 2-input positive-NOR gate performs the Boolean function $Y = \overline{A} + \overline{B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUP1G02

LOW-POWER SINGLE 2-INPUT POSITIVE-NOR GATE

SCES568D–JUNE 2004–REVISED MAY 2007

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

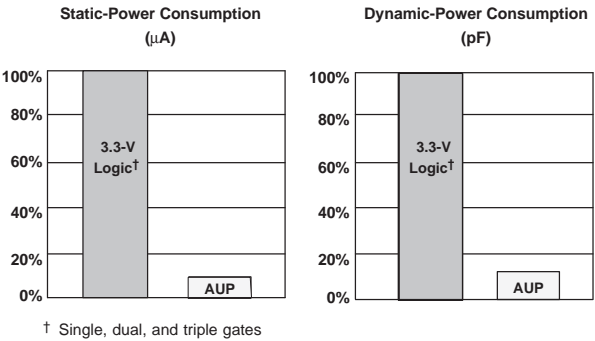


Figure 1. AUP – The Lowest-Power Family

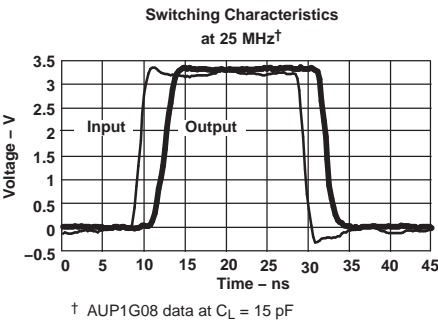


Figure 2. Excellent Signal Integrity

ORDERING INFORMATION

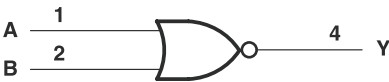
T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G02YFPR	PREVIEW
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G02YZPR	PREVIEW
	SON – DRY	Reel of 5000	SN74AUP1G02DRYR	PREVIEW
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G02DBVR	H02_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G02DCKR	HB_
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G02DRLR	HB_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site. YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
L	L	H
L	H	L
H	L	L
H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range ⁽²⁾		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		–0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾		–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package		206	°C/W
		DCK package		252	
		DRL package		142	
		DRY package		234	
		YFP/YZP package		132	
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUP1G02

LOW-POWER SINGLE 2-INPUT POSITIVE-NOR GATE

SCES568D–JUNE 2004–REVISED MAY 2007

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.6		
		V _{CC} = 3 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0		V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.9		
V _I	Input voltage		0	3.6	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	−20		μA
		V _{CC} = 1.1 V	−1.1		mA
		V _{CC} = 1.4 V	−1.7		
		V _{CC} = 1.65 V	−1.9		
		V _{CC} = 2.3 V	−3.1		
		V _{CC} = 3 V	−4		
I _{OL}	Low-level output current	V _{CC} = 0.8 V	20		μA
		V _{CC} = 1.1 V	1.1		mA
		V _{CC} = 1.4 V	1.7		
		V _{CC} = 1.65 V	1.9		
		V _{CC} = 2.3 V	3.1		
		V _{CC} = 3 V	4		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V	200		ns/V
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}		I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
		I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
		I _{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I _{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I _{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I _{OH} = –3.1 mA		1.9			1.85		
		I _{OH} = –2.7 mA	3 V	2.72			2.67		
		I _{OH} = –4 mA		2.6			2.55		
V _{OL}		I _{OL} = 20 μA	0.8 V to 3.6 V	0.1			0.1		V
		I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
		I _{OL} = 1.7 mA	1.4 V	0.31			0.37		
		I _{OL} = 1.9 mA	1.65 V	0.31			0.35		
		I _{OL} = 2.3 mA	2.3 V	0.31			0.33		
		I _{OL} = 3.1 mA		0.44			0.45		
		I _{OL} = 2.7 mA	3 V	0.31			0.33		
		I _{OL} = 4 mA		0.44			0.45		
I _I	A or B inputs	V _I = GND to 3.6 V	0 V to 3.6 V	0.1			0.5	μA	
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V	0.2			0.6	μA	
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V	0.2			0.6	μA	
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V	0.5			0.9	μA	
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V	40			50	μA	
C _i		V _I = V _{CC} or GND	0 V	1.5					pF
			3.6 V	1.5					
C _o		V _O = GND	0 V	3					pF

(1) One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND

Switching Characteristics

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8 V	19.3					ns
			1.2 V ± 0.1 V	2.6	7.3	13	2.1	16.3	
			1.5 V ± 0.1 V	1.4	5.2	8.9	0.9	10.8	
			1.8 V ± 0.15 V	1	4.2	6.8	0.5	8.7	
			2.5 V ± 0.2 V	1	3	4.6	0.5	5.9	
			3.3 V ± 0.3 V	1	2.4	3.7	0.5	4.6	

SN74AUP1G02

LOW-POWER SINGLE 2-INPUT POSITIVE-NOR GATE

SCES568D–JUNE 2004–REVISED MAY 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		22.3				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	1.5	8.5	14.9	1	17.9	
			$1.5\text{ V} \pm 0.1\text{ V}$	1	6.2	10.2	0.5	11.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	1	5	7.9	0.5	9.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	3.6	5.4	0.5	6.5	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	2.9	4.4	0.5	5	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		25				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.6	9.9	16.5	3.1	20.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	2.3	7.2	11.3	1.8	13.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	1.6	5.8	8.9	1.1	11.1	
			$2.5\text{ V} \pm 0.2\text{ V}$	1	4.3	6.1	0.5	7.7	
			$3.3\text{ V} \pm 0.3\text{ V}$	1	3.4	5	0.5	6.2	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

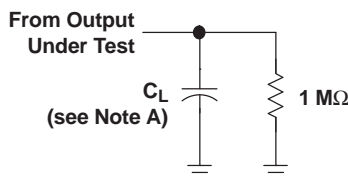
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		34.6				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.9	13.1	21.1	4.4	26.2	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.4	9.5	14.4	2.9	17.4	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.5	7.7	11.2	2	14	
			$2.5\text{ V} \pm 0.2\text{ V}$	1.8	5.7	7.8	1.3	9.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.5	4.7	6.4	1	7.8	

Operating Characteristics

$T_A = 25^\circ\text{C}$

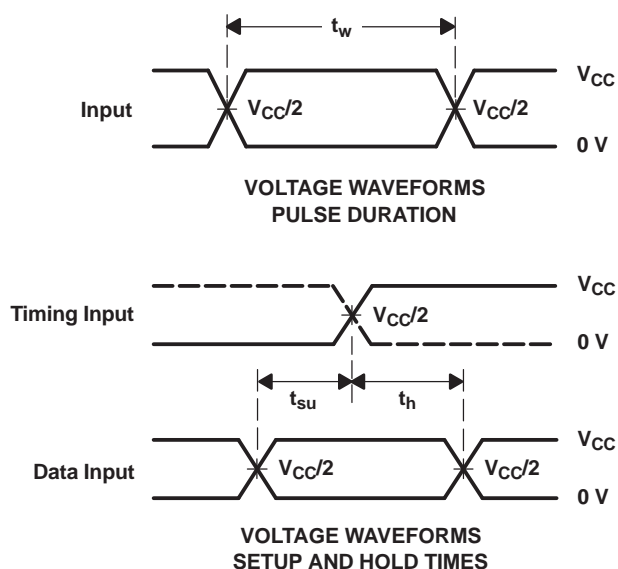
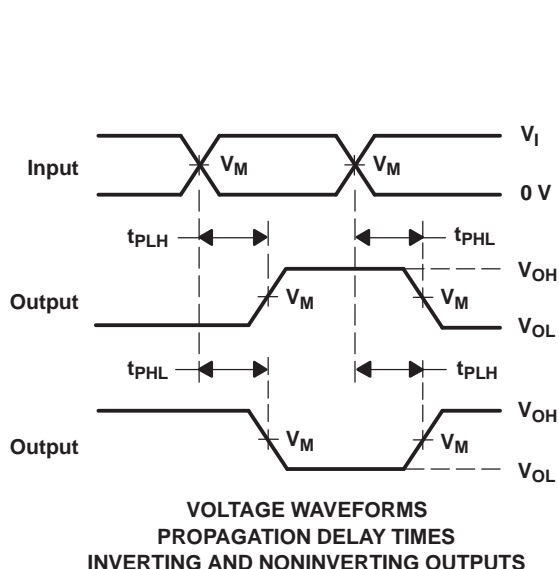
PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$		0.8 V	4.1	pF
				$1.2\text{ V} \pm 0.1\text{ V}$	4.1	
				$1.5\text{ V} \pm 0.1\text{ V}$	4.1	
				$1.8\text{ V} \pm 0.15\text{ V}$	4.1	
				$2.5\text{ V} \pm 0.2\text{ V}$	4.2	
				$3.3\text{ V} \pm 0.3\text{ V}$	4.3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

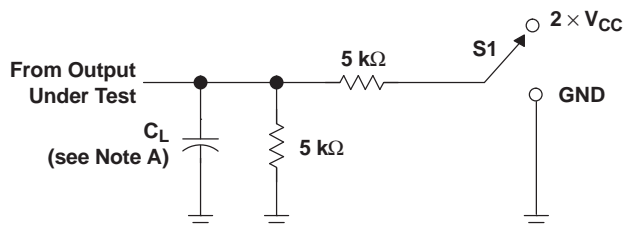
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

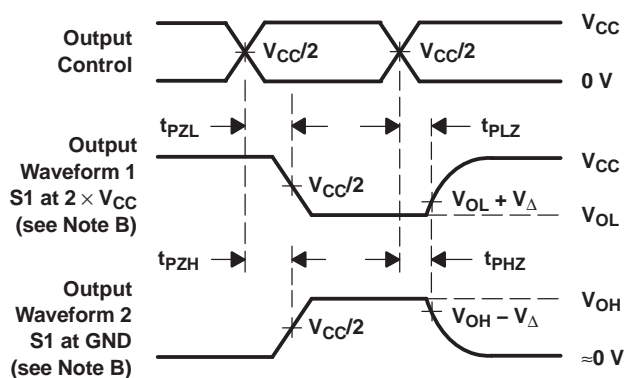
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHZ}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PHZ} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUP1G02DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G02DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G02DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G02DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G02DCKR	SC70	DCK	5	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G02DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G02DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G02DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G02DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G02DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G02DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G02DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.



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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

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