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SN74CB3T3125
QUADRUPLE FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER
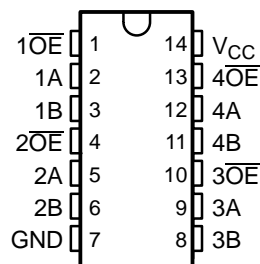**SCDS120A – FEBRUARY 2003 – REVISED JANUARY 2006**

FEATURES

- **Output Voltage Translation Tracks V_{CC}**
- **Supports Mixed-Mode Signal Operation On All Data I/O Ports**
  - **5-V Input Down to 3.3-V Output-Level Shift With 3.3-V V_{CC}**
  - **5-V/3.3-V Input Down to 2.5-V Output-Level Shift With 2.5-V V_{CC}**
- **5-V-Tolerant I/Os With Device Powered Up or Powered Down**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typ)**
- **Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 4.5 pF Typ)**
- **Data and Control Inputs Provide Undershoot Clamp Diodes**

- **Low Power Consumption (I_{CC} = 20 μA Max)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Digital Applications: Level Translation, USB Interface, Bus Isolation**
- **Ideal for Low-Power Portable Equipment**

DGV OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	14	V_{CC}
1A	2	13	4$\overline{OE}$
1B	3	12	4A
2$\overline{OE}$	4	11	4B
2A	5	10	3$\overline{OE}$
2B	6	9	3A
GND	7	8	3B

DESCRIPTION/ORDERING INFORMATION

The SN74CB3T3125 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3125 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tube	SN74CB3T3125PW	KS125
		Tape and reel	SN74CB3T3125PWR	
	TVSOP – DGV	Tape and reel	SN74CB3T3125DGVR	KS125

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)
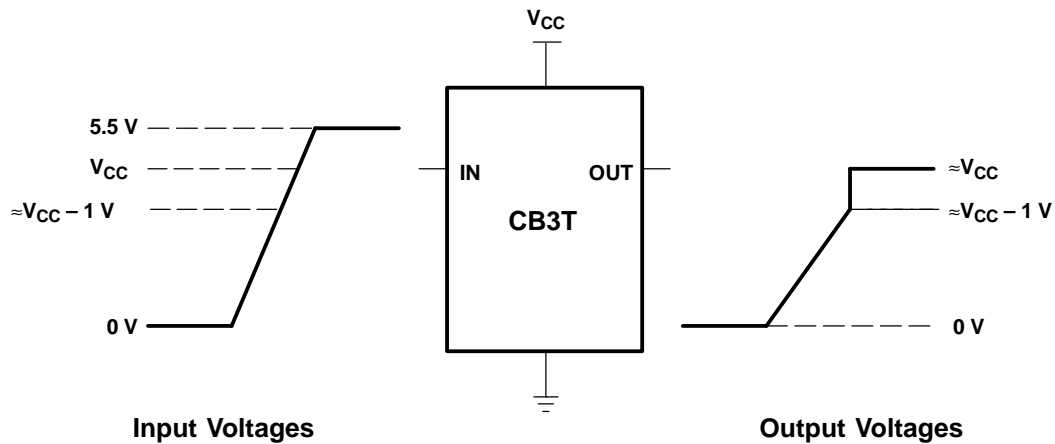
NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1$ V, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level is approximately equal to the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The SN74CB3T3125 is organized as four 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When $\overline{OE}$ is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.
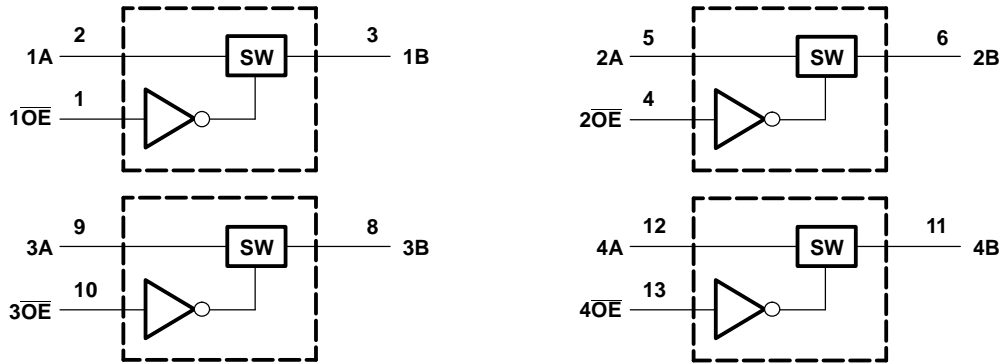
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.
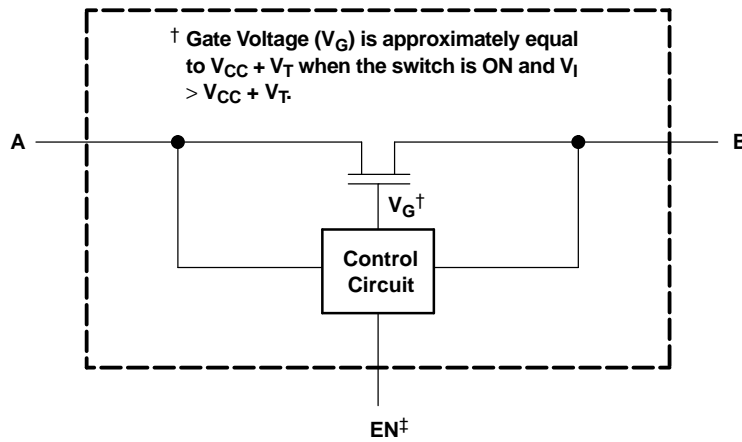
FUNCTION TABLE
(EACH BUS SWITCH)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)

SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)

† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.

‡ EN is the internal enable signal applied to the switch.

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Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[2]		−0.5	7	V
V_{IN}	Control input voltage range[2][3]		−0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2][3][4]		−0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		−50	mA
$I_{I/O}$	ON-state switch current[5]			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[6]	DGV package		127	°C/W
		PW package		113	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics[1]

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}		$V_{CC} = 3$ V, $I_I = -18$ mA				-1.2	V
V_{OH}		See Figure 3 and Figure 4					
I_{IN}	Control inputs	$V_{CC} = 3.6$ V, $V_{IN} = 3.6$ V to 5.5 V or GND				± 10	µA
I_I		$V_{CC} = 3.6$ V, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7$ V to 5.5 V			± 20	µA
			$V_I = 0.7$ V to $V_{CC} - 0.7$ V			-40	
			$V_I = 0$ to 0.7 V			± 5	
I_{OZ}[3]		$V_{CC} = 3.6$ V, $V_O = 0$ to 5.5 V, $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND				± 10	µA
I_{off}		$V_{CC} = 0$, $V_O = 0$ to 5.5 V, $V_I = 0$				10	µA
I_{CC}		$V_{CC} = 3.6$ V, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND			20	µA
			$V_I = 5.5$ V			20	
ΔI_{CC}[4]	Control inputs	$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	$V_{CC} = 3.3$ V, $V_{IN} = V_{CC}$ or GND			3		pF
$C_{io(OFF)}$		$V_{CC} = 3.3$ V, $V_{I/O} = 5.5$ V, 3.3 V, or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND			4.5		pF
$C_{io(ON)}$		$V_{CC} = 3.3$ V, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5$ V or 3.3 V		4		pF
			$V_{I/O} = $ GND		10		
r_{on}[5]		$V_{CC} = 2.3$ V, TYP at $V_{CC} = 2.5$ V, $V_I = 0$	$I_O = 24$ mA		5	8	Ω
			$I_O = 16$ mA		5	8	
		$V_{CC} = 3$ V, $V_I = 0$	$I_O = 64$ mA		5	7	
			$I_O = 32$ mA		5	7	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2)   All typical values are at $V_{CC} = 3.3$ V (unless otherwise noted), $T_A = 25°$C.
(3)   For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4)   This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5)   Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.
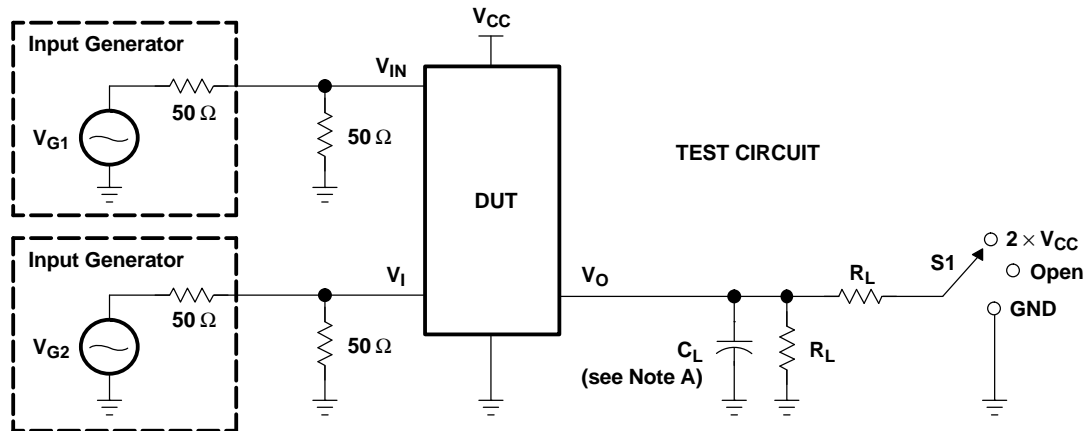
Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 3.3$ V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[1]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	8.5	1	4.4	ns
t_{dis}	$\overline{OE}$	A or B	1	9	1	9	ns

(1)   The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER
SCDS120A−FEBRUARY 2003−REVISED JANUARY 2006

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V	2 × V_{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V_{CC}	500 Ω	GND	50 pF	0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V
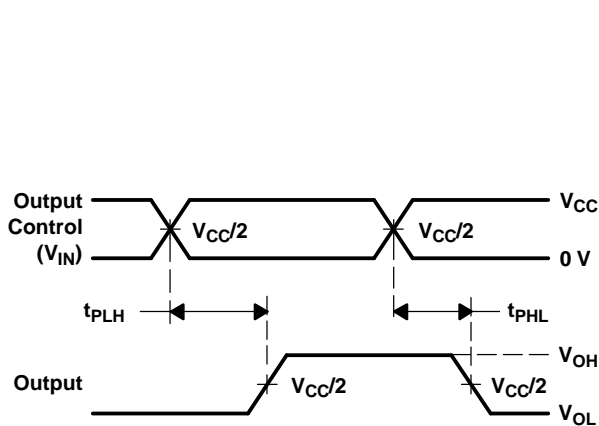
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)**
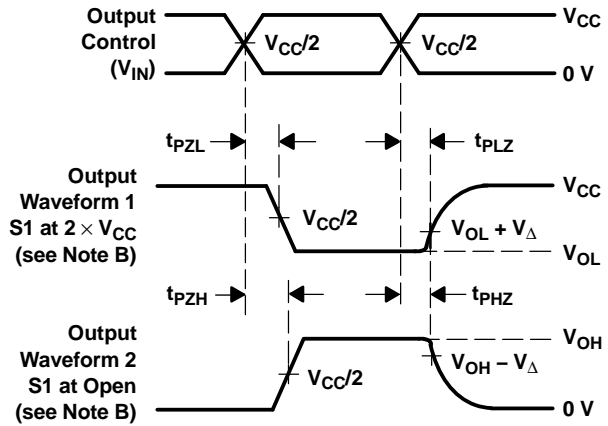
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

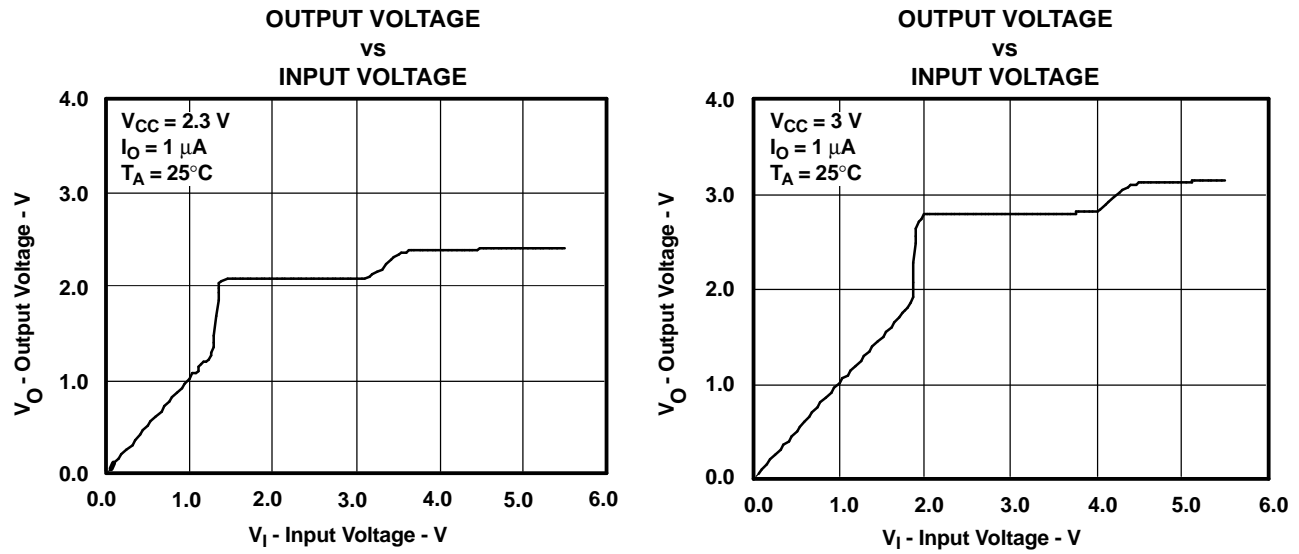**Figure 2. Test Circuit and Voltage Waveforms**

TYPICAL CHARACTERISTICS

Figure 3. Data Output Voltage vs Data Input Voltage

SN74CB3T3125

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TYPICAL CHARACTERISTICS (continued)

**OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE**

**OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE**

**OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE**
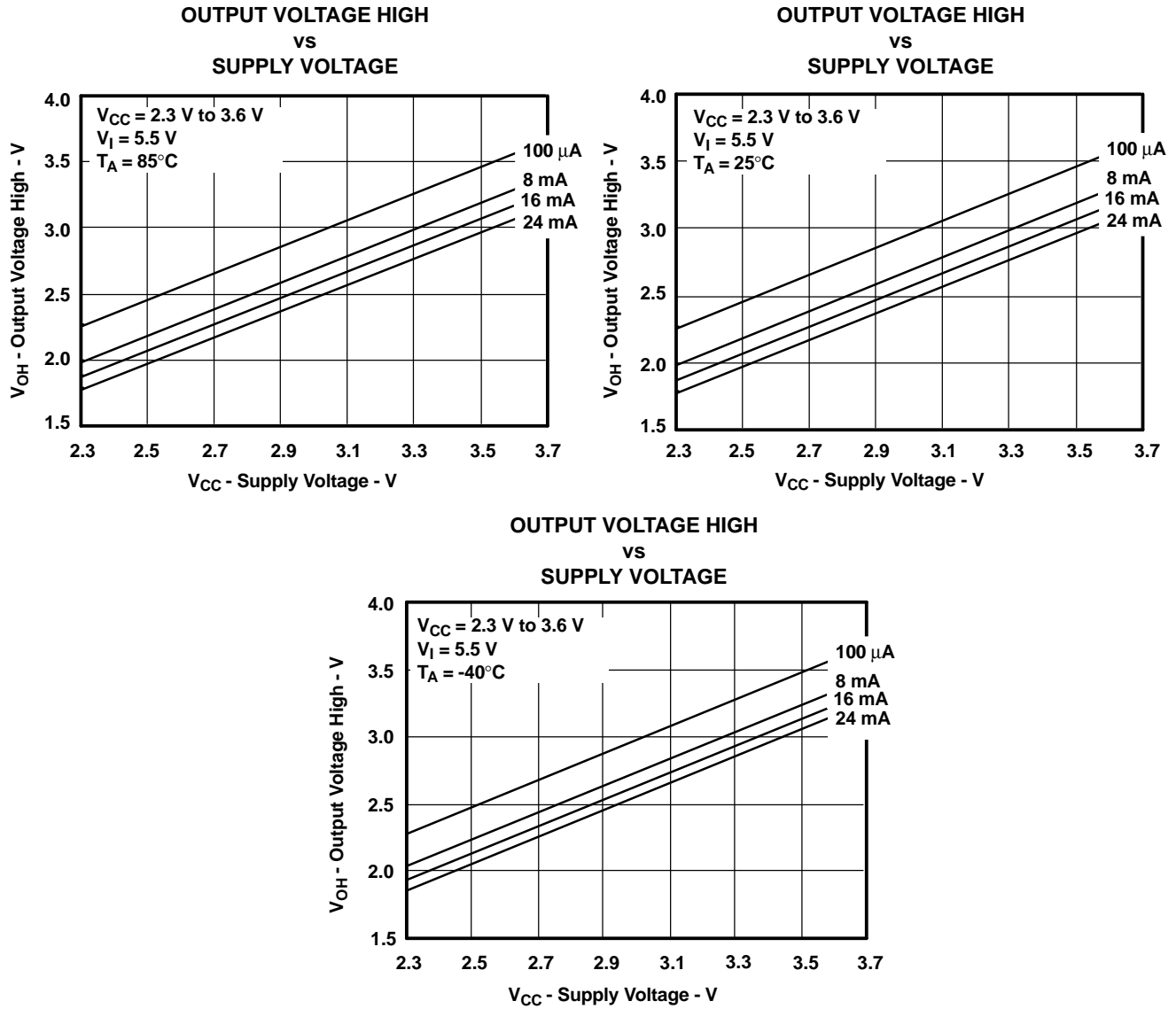
Figure 4. V$_{OH}$ Values

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74CB3T3125DGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3T3125DGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3T3125RGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CB3T3125DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3T3125RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

User Direction of Feed

Pocket Quadrants

Sprocket Holes

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3T3125PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74CB3T3125RGYR	QFN	RGY	14	1000	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
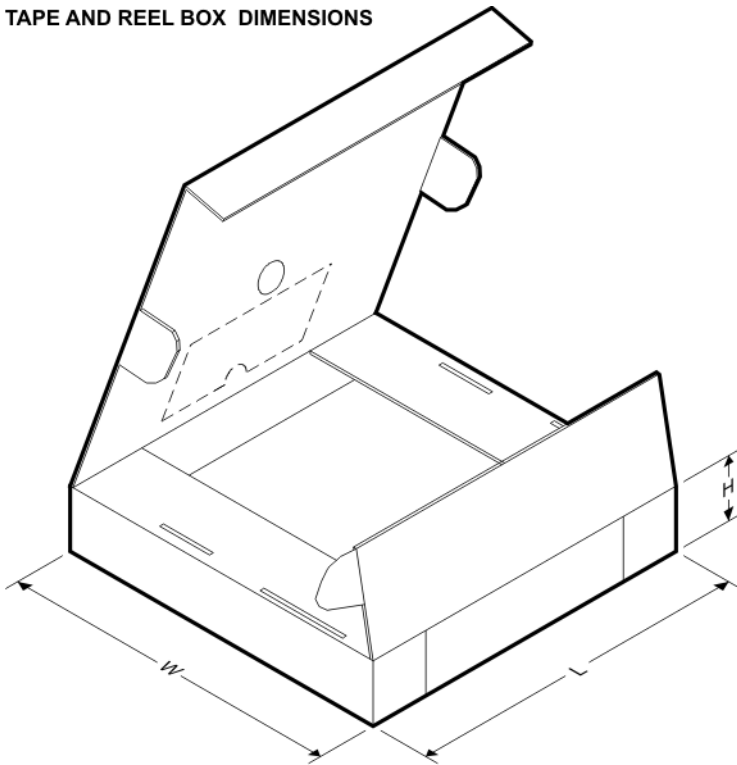
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3125DGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74CB3T3125PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74CB3T3125RGYR	QFN	RGY	14	1000	190.5	212.7	31.8

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (S−PQFP−N14)   PLASTIC QUAD FLATPACK

3,65 / 3,35 A

B

13   9

14   8

3,65 / 3,35

Pin 1 Index Area
Top and Bottom
E

1   2   6

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

0,05 / 0,00
Seating Height

C

△ 0,08 C

2,00

0,50

14X 0,50 / 0,30

2   6

1   7

1,50

2,05 +0,10 −0,15

14   8

Exposed Thermal Pad
D

13   9

14X 0,30 / 0,18

2,05 +0,10 −0,15

⊕ 0,10 Ⓜ C A B
0,05 Ⓜ C

Bottom View
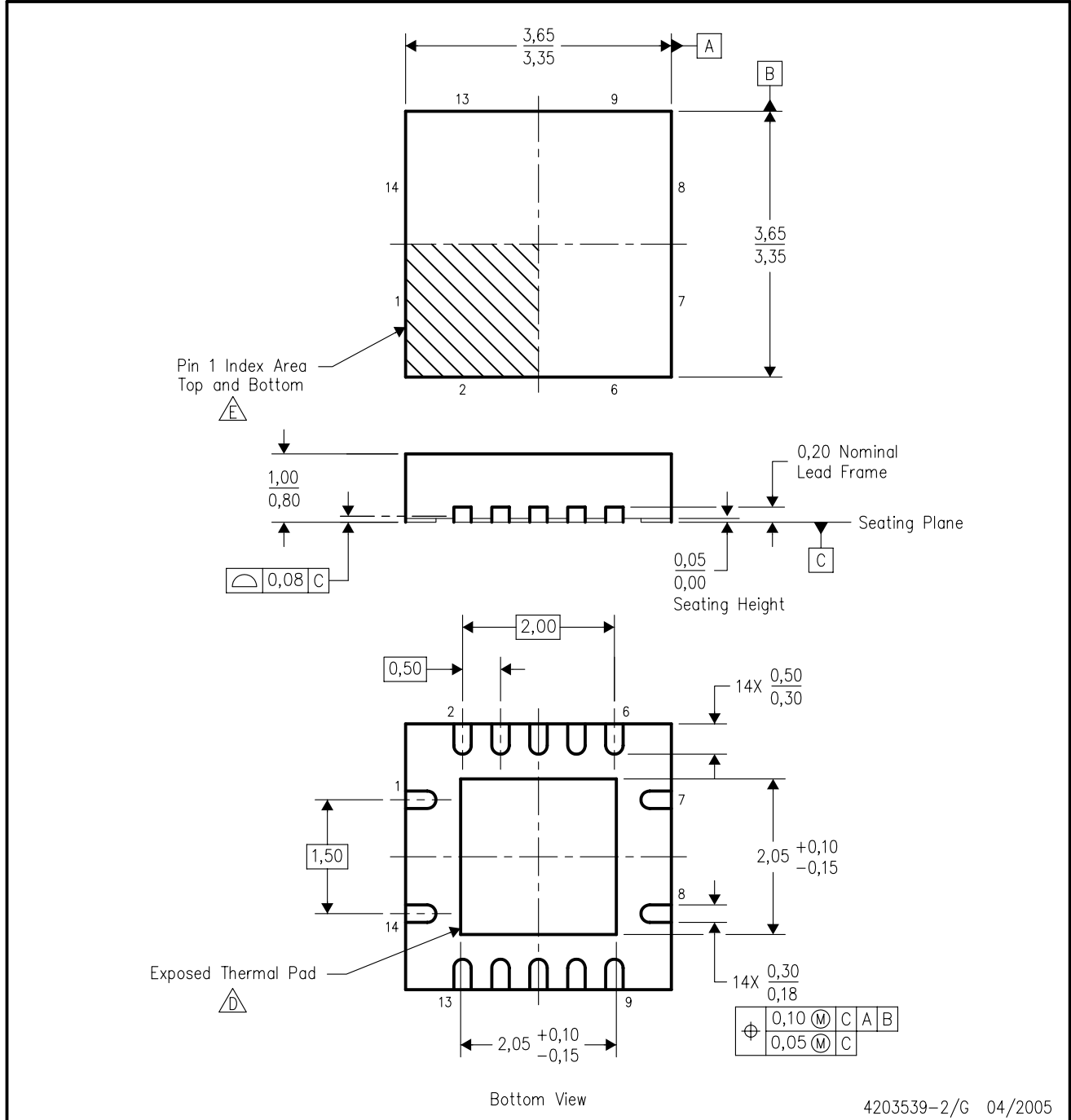
4203539−2/G 04/2005

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
            The Pin 1 identifiers are either a molded, marked, or metal feature.
        F. Package complies to JEDEC MO−241 variation BA.

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THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
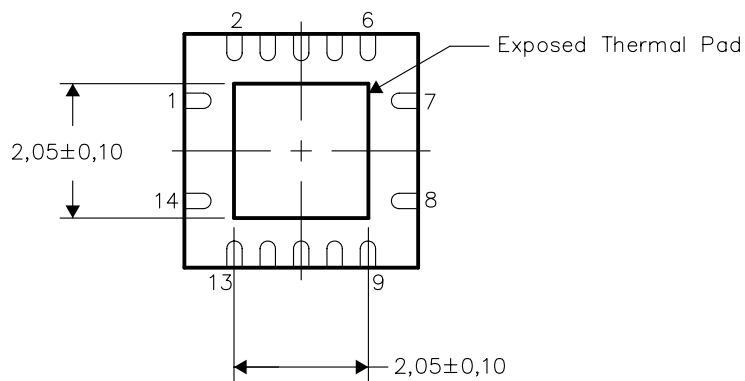
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R–PQFP–N14)
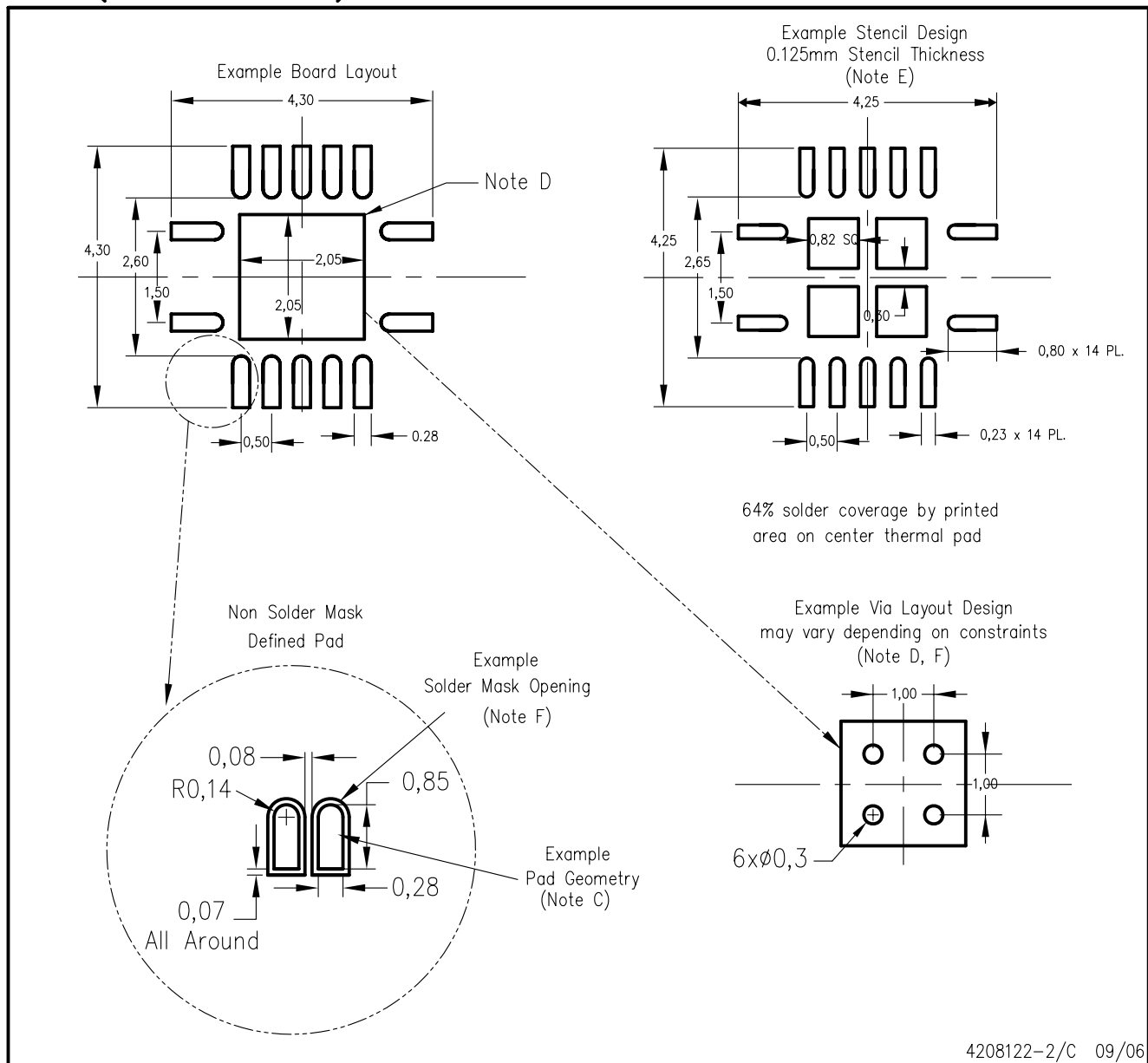
Example Board Layout

4,30

4,30

2,60

2,05

2,05

1,50

Note D

0,50

0.28

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,25

4,25

2,65

1,50

0,82 SQ

0,80

0,80 x 14 PL.

0,50

0,23 x 14 PL.

64% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

Example
Pad Geometry
(Note C)

0,07

All Around

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6xØ0,3

4208122–2/C   09/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board.   Refer to Application Note, Quad Flat–Pack
              Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout.   These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.   Customers should
              contact their board assembly site for stencil design recommendations.   Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE