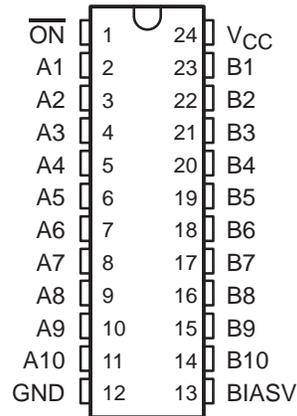# 10-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS
AND ACTIVE-CLAMP UNDERSHOOT-PROTECTION CIRCUIT

SCDS107B – APRIL 2000 – REVISED OCTOBER 2000

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Power Off Disables Outputs, Permitting Live Insertion**
- **Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion**
- **Active-Clamp Undershoot-Protection Circuit on the I/Os Clamps Undershoots Down to –2 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

$\overline{\text{ON}}$	1	24	V_{CC}
A1	2	23	B1
A2	3	22	B2
A3	4	21	B3
A4	5	20	B4
A5	6	19	B5
A6	7	18	B6
A7	8	17	B7
A8	9	16	B8
A9	10	15	B9
A10	11	14	B10
GND	12	13	BIASV

description

The SN74CBTK6800 device provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The A and B ports have an active-clamp undershoot-protection circuit. When there is an undershoot, the active-clamp circuit is enabled and current from V_{CC} is supplied to clamp the output, preventing the pass transistor from turning on.

The SN74CBTK6800 is organized as one 10-bit switch with a single enable ($\overline{\text{ON}}$) input. When $\overline{\text{ON}}$ is low, the switch is on, and port A is connected to port B. When $\overline{\text{ON}}$ is high, the switch between port A and port B is open. When $\overline{\text{ON}}$ is high or V_{CC} is 0 V, B port is precharged to BIASV through the equivalent of a 10-kΩ resistor.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – DW	Tube	SN74CBTK6800DW	CBTK6800
		Tape and reel	SN74CBTK6800DWR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTK6800DBQR	CBTK6800
	TSSOP – PW	Tape and reel	SN74CBTK6800PWR	BK6800
	TVSOP – DGV	Tape and reel	SN74CBTK6800DGVR	BK6800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{\text{ON}}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

logic diagram (positive logic)
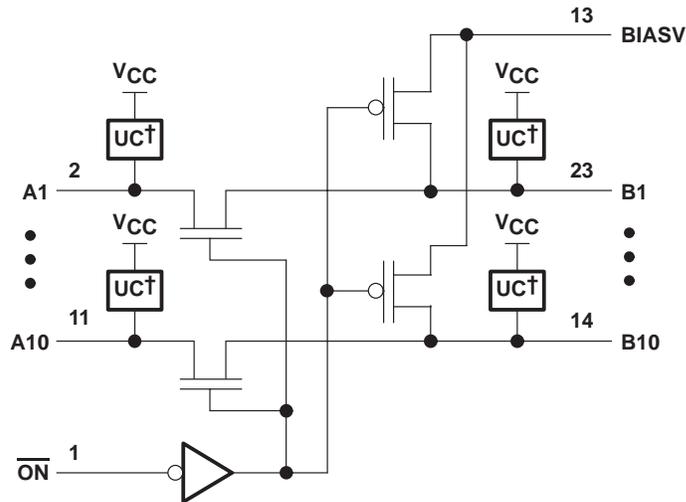
† Undershoot clamp

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Bias voltage range, BIASV . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Continuous channel current . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBQ package . . . . 61°C/W
DGV package . . . . 86°C/W
DW package . . . . 46°C/W
PW package . . . . 88°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V_{CC}	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{IKU}		V_{CC} = 5.5 V,	0 mA ≥ I_I ≥ −50 mA,	$\overline{OE}$ = 5.5 V			−2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	μA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 5.5 V,	BIASV = Open			20	μA
I_O		V_{CC} = 4.5 V,	V_O= 0,	BIASV = 2.4 V	0.25			mA
I_{CC}		V_{CC} = 5.5 V,	V_I = V_{CC} or GND,	I_O = 0			20	μA
ΔI_{CC}[‡]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_i	Control inputs	V_I = 3 V or 0					3	pF
$C_{O(OFF)}$		V_O = 3 V or 0,	Switch off				8.5	pF
r_{on}[§]		V_{CC} = 4 V, TYP at V_{CC} = 4 V	V_I = 2.4 V,	I_I = 15 mA		11	20	Ω
		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		3	7	
				I_I = 30 mA		3	7	
			V_I = 2.4 V,	I_I = 15 mA		6	15	

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
[‡] This is the increase in supply current for each input that is at the specified TTL-voltage level rather than V_{CC} or GND.
[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 4 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}[¶]	A or B	B or A			0.35		0.25	ns
t_{PZH}	$\overline{ON}$	A or B	BIASV = GND		6	2	5.1	ns
t_{PZL}			BIASV = 3 V		6	2	5.6	
t_{PHZ}	$\overline{ON}$	A or B	BIASV = GND		5.5	1	5	ns
t_{PLZ}			BIASV = 3 V		5.5	2	5.9	

[¶] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

TEXAS INSTRUMENTS

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{OUTU}	See Figures 1 and 2, and Table 1	2	V_{OH}–0.3		V

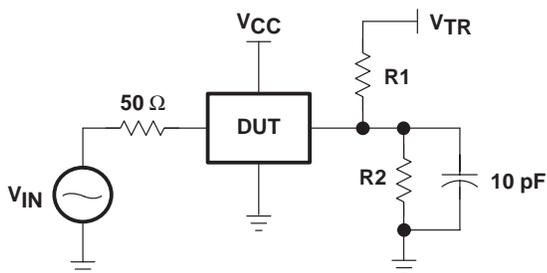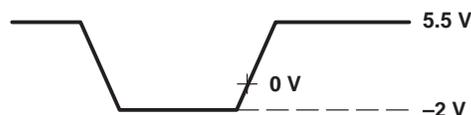[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

Figure 1. Device Test Setup

Figure 2. Transient Input Voltage Waveform
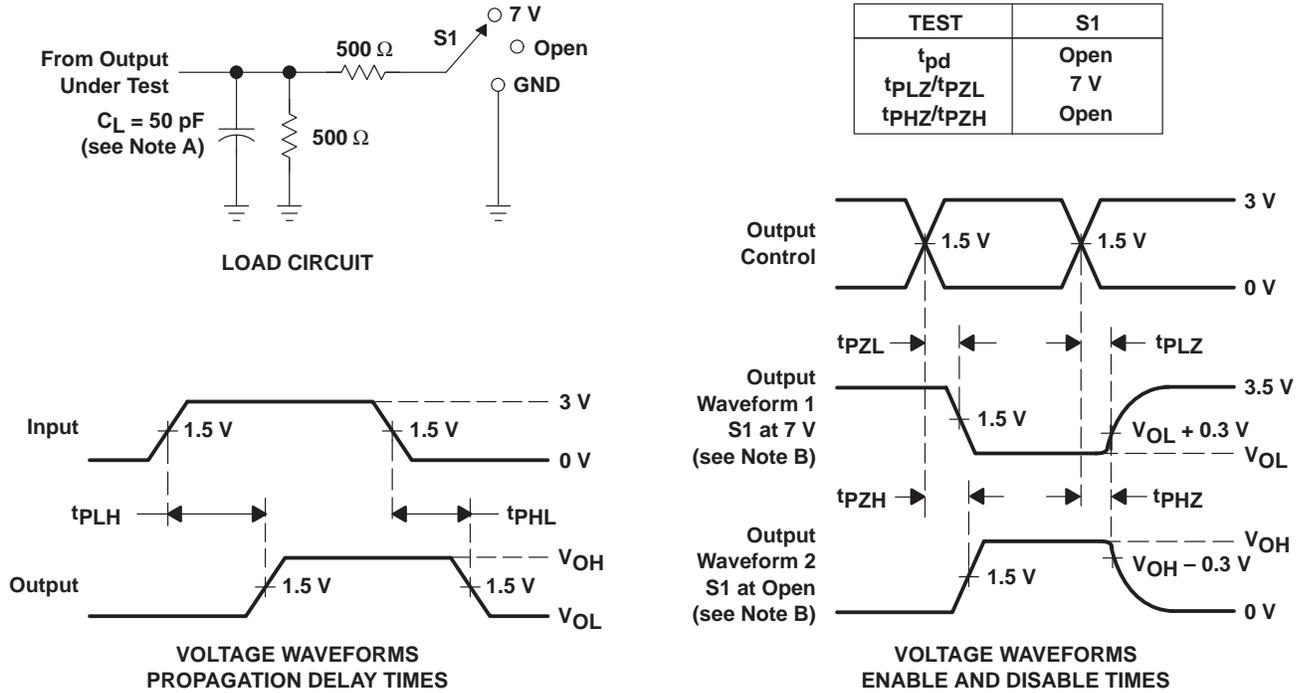
Table 1. Device Test Conditions

PARAMETER	VALUE	UNIT
B port under test[‡]	See Figure 1	
V_{IN}	See Figure 2	V
t_w	20	ns
t_r	2	ns
t_f	2	ns
R1 = R2	100	kΩ
V_{TR}	11	V
V_{CC}	5.5	V
BIASV	Open	

[‡] Other B-port outputs are open.

PARAMETER MEASUREMENT INFORMATION

From Output Under Test 500 Ω **S1** 7 V Open GND

C_L = 50 pF (see Note A) 500 Ω

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

Output Control 1.5 V 1.5 V 3 V 0 V

t_{PZL} t_{PLZ}

Output Waveform 1 S1 at 7 V (see Note B) 1.5 V 3.5 V V_{OL} + 0.3 V V_{OL}

t_{PZH} t_{PHZ}

Output Waveform 2 S1 at Open (see Note B) 1.5 V V_{OH} V_{OH} − 0.3 V 0 V

Input 1.5 V 1.5 V 3 V 0 V

t_{PLH} t_{PHL}

Output 1.5 V 1.5 V V_{OH} V_{OL}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74CBTK6800DBQRE4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CBTK6800DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
74CBTK6800DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTK6800DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74CBTK6800DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTK6800PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
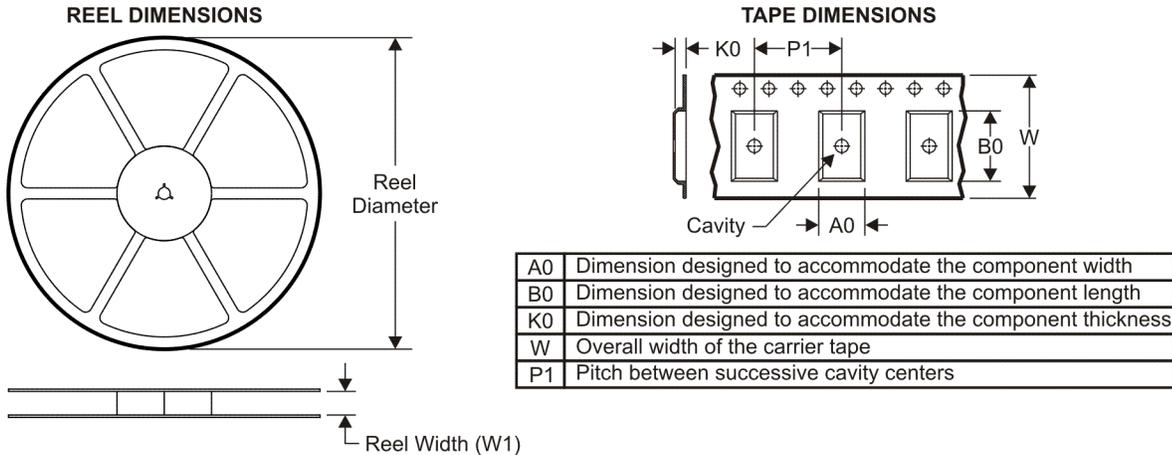
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
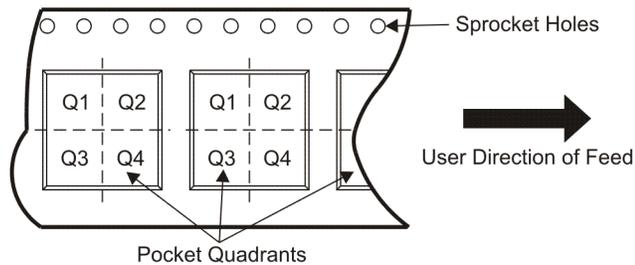
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTK6800DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTK6800DGVR	TVSOP	DGV	24	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74CBTK6800DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTK6800PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
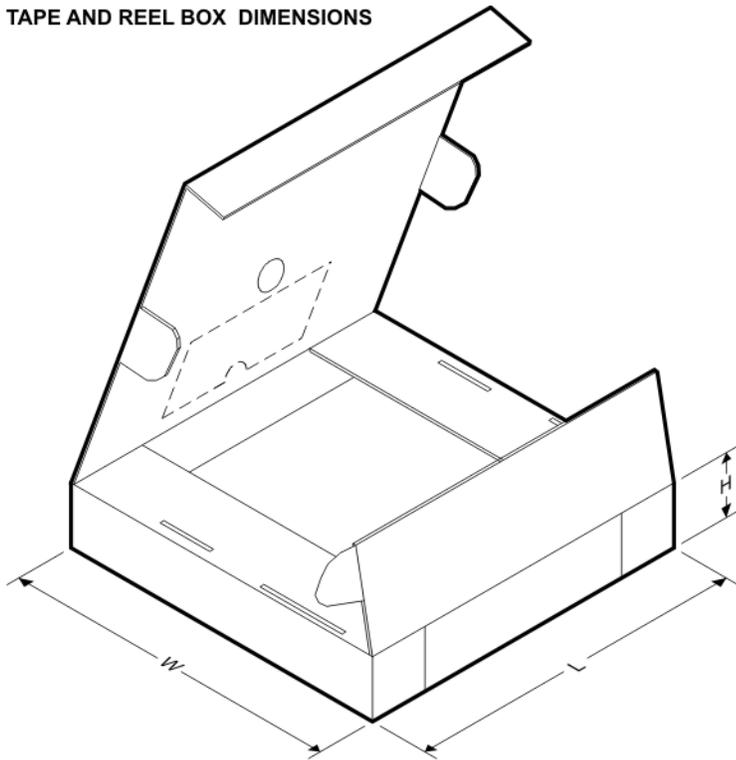
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTK6800DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
SN74CBTK6800DGVR	TVSOP	DGV	24	2000	346.0	346.0	29.0
SN74CBTK6800DWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74CBTK6800PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

DIM \ PINS**	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
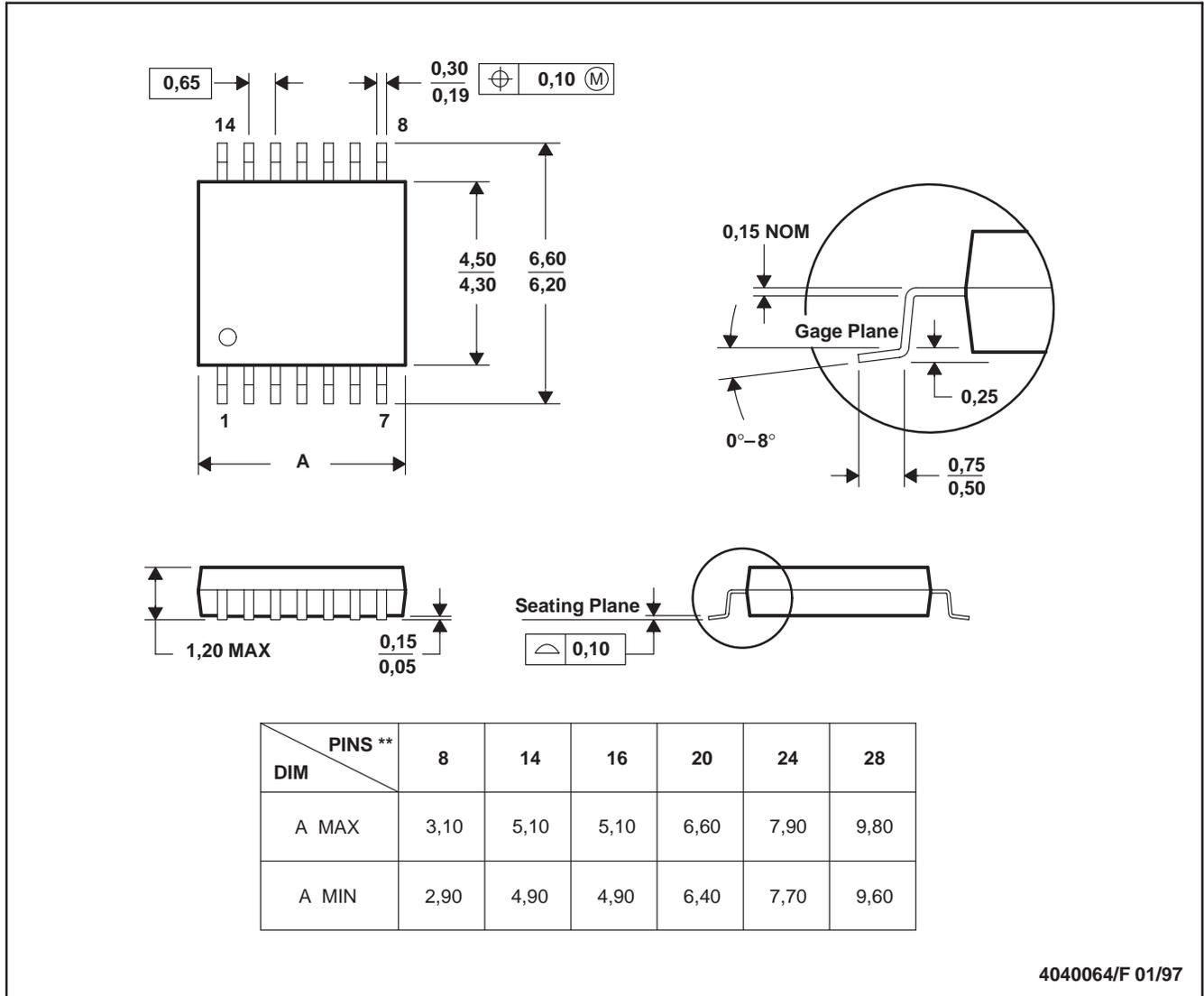
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
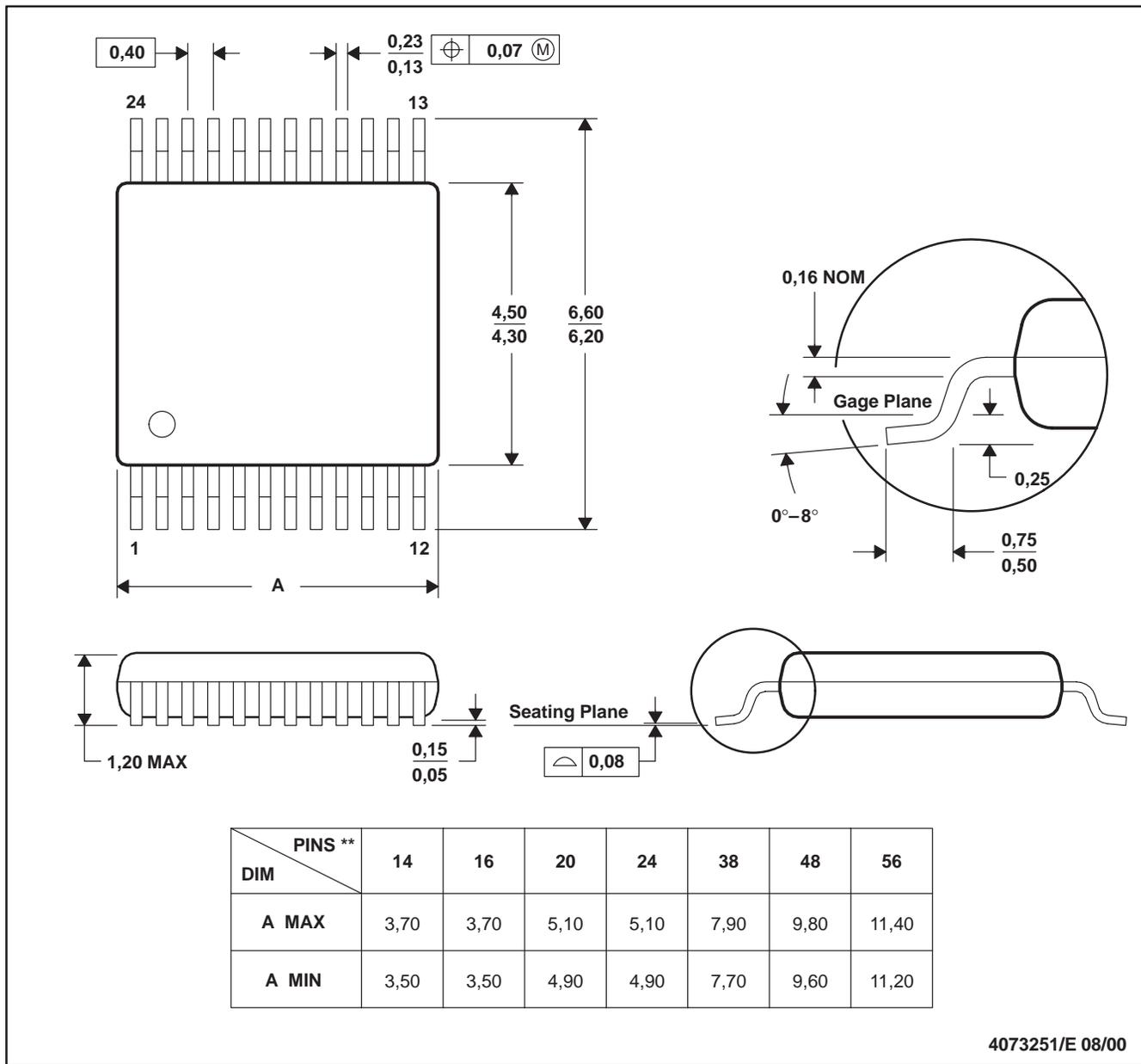
PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
  D. Falls within JEDEC: 24/48 Pins – MO-153
                14/16/20/56 Pins – MO-194

DBQ (R−PDSO−G24)　　　　　PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

24

13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

12

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.006 (0,15)

Gauge Plane

0.010 (0,25)

0°−8°

0.004 (0,10)

Seating Plane

0.035 (0,89)
0.016 (0,40)

4073301−4/G 02/2005

NOTES:　A. All linear dimensions are in inches (millimeters).
　　　　　B. This drawing is subject to change without notice.
　　　　　C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
　　　　　D. Falls within JEDEC MO−137 variation AE.

DW (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60)
0.598 (15,20)

24   13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−5/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D. Falls within JEDEC MS−013 variation AD.