

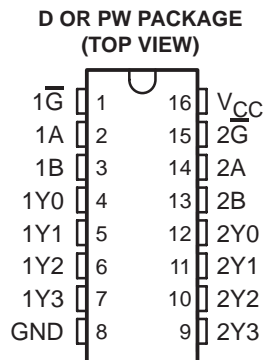
# SN74HC139-Q1

## DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCLS598A – NOVEMBER 2004 – REVISED MARCH 2005

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Targeted Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to Ten LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 10$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- ESD Protection Level per AEC-Q100 Classification
  - 2000-V (H2) Human-Body Model
  - 200-V (M3) Machine Model
  - 1000-V (C5) Charged-Device Model

† Contact factory for details. Q100 qualification data available on request.



### description/ordering information

The SN74HC139 device is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of this decoder and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The SN74HC139 device comprises two individual 2-line to 4-line decoders in a single package. The active-low enable ( $\overline{G}$ ) input can be used as a data line in demultiplexing applications. This decoder/demultiplexer features fully buffered inputs, each of which represents only one normalized load to its driving circuit.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Reel of 2500	SN74HC139QDRQ1	HC139Q
	TSSOP – PW	Reel of 2000	SN74HC139QPWRQ1	HC139Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L



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### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 4.5 V	3.15		
		V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5		V
		V <sub>CC</sub> = 4.5 V	1.35		
		V <sub>CC</sub> = 6 V	1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V	1000		ns
		V <sub>CC</sub> = 4.5 V	500		
		V <sub>CC</sub> = 6 V	400		
T <sub>A</sub>	Operating free-air temperature	-40	125		°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9	1.9			V
			4.5 V	4.4	4.499	4.4	4.4			
			6 V	5.9	5.999	5.9	5.9			
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7	3.84			
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8	5.2	5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1	0.1	0.1		V
			4.5 V		0.001	0.1	0.1	0.1		
			6 V		0.001	0.1	0.1	0.1		
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26	0.4	0.33		
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26	0.4	0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100	±1000	±1000		nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	160	80		μA	
C <sub>i</sub>		2 V to 6 V		3	10	10	10		pF	



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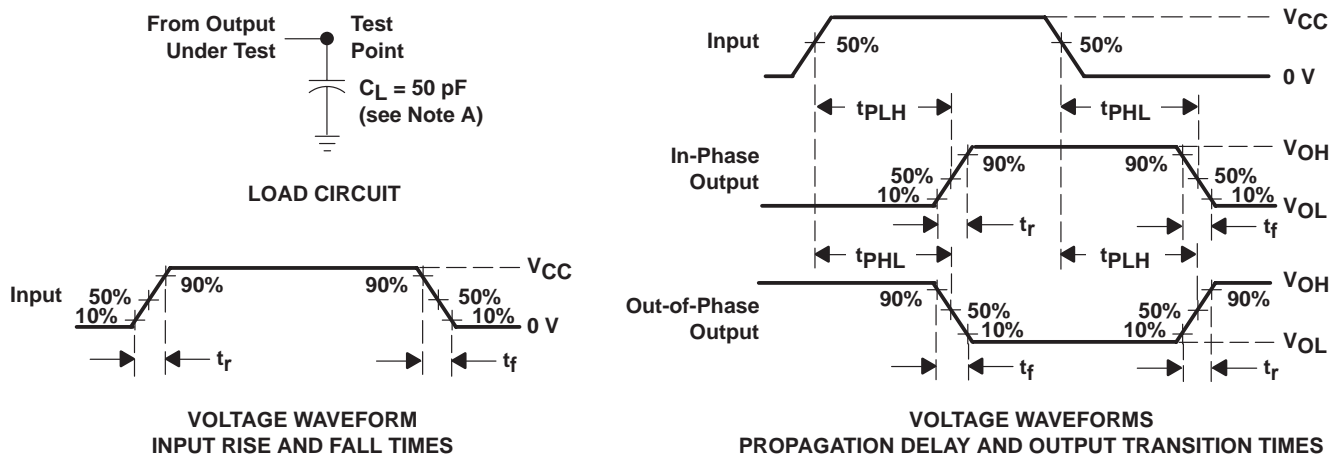
switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	2 V		47	175		255		220	ns
			4.5 V		14	35		51		44	
			6 V		12	30		44		38	
	$\bar{G}$	Y	2 V		39	175		255		220	
			4.5 V		11	35		51		44	
			6 V		10	30		44		38	
$t_t$		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per decoder	No load	25	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. The outputs are measured one at a time, with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HC139QDRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74HC139QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

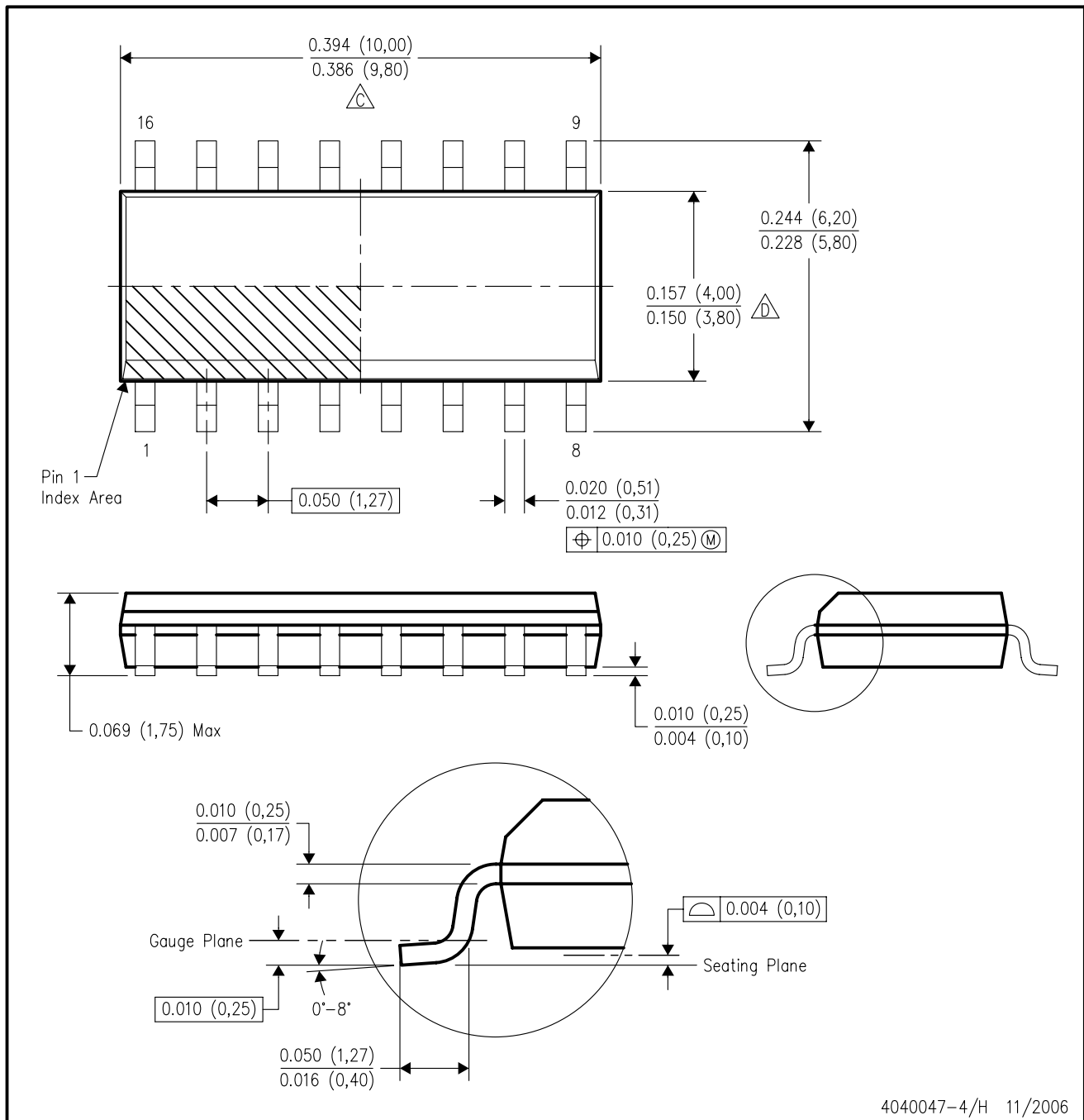
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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