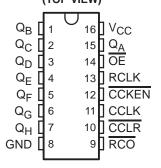
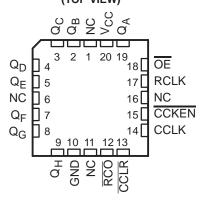
- 2-V to 6-V V_{CC} Operation
- High-Current 3-State Parallel Register
 Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 14 ns

SN54HC590A . . . J OR W PACKAGE SN74HC590A . . . D, DW, OR N PACKAGE (TOP VIEW)



- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- 8-Bit Counter With Register
- Counter Has Direct Clear

SN54HC590A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

description/ordering information

The 'HC590A devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features direct clear (CCLR) and count-enable (CCKEN) inputs. A ripple-carry output (RCO) is provided for cascading. Expansion is accomplished easily for two stages by connecting RCO of the first stage to CCKEN of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to the counter clock (CCLK) input of the following stage.

CCLK and the register clock (RCLK) inputs are positive-edge triggered. If both clocks are connected together, the counter state always is one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

ORDERING INFORMATION

| TA | PACI | KAGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|--------------|--------------------------|---------------------|
| | PDIP – N | Tube of 25 | SN74HC590AN | SN74HC590AN |
| | | Tube of 40 | SN74HC590AD | |
| 4000 1- 0500 | SOIC - D | Reel of 2500 | SN74HC590ADR | HC590A |
| -40°C to 85°C | | Reel of 250 | SN74HC590ADT | |
| | | Tube of 40 | SN74HC590ADW | 1105004 |
| | SOIC - DW | Reel of 2000 | SN74HC590ADWR | HC590A |
| | CDIP – J | Tube of 25 | SNJ54HC590AJ | SNJ54HC590AJ |
| –55°C to 125°C | CFP – W | Tube of 150 | SNJ54HC590AW | SNJ54HC590AW |
| | LCCC - FK | Tube of 55 | SNJ54HC590AFK | SNJ54HC590AFK |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design quidelines are available at www.ti.com/sc/package.



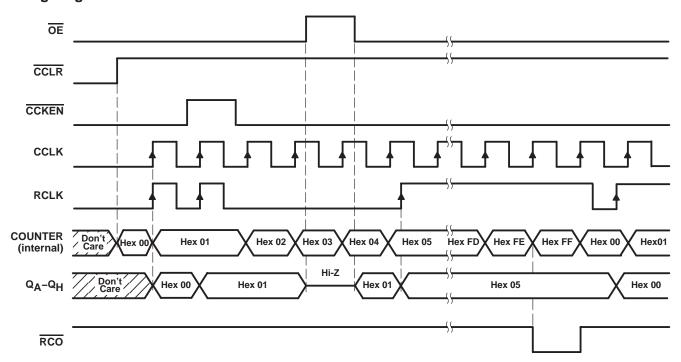
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54HC590A, SN74HC590A 8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

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timing diagram

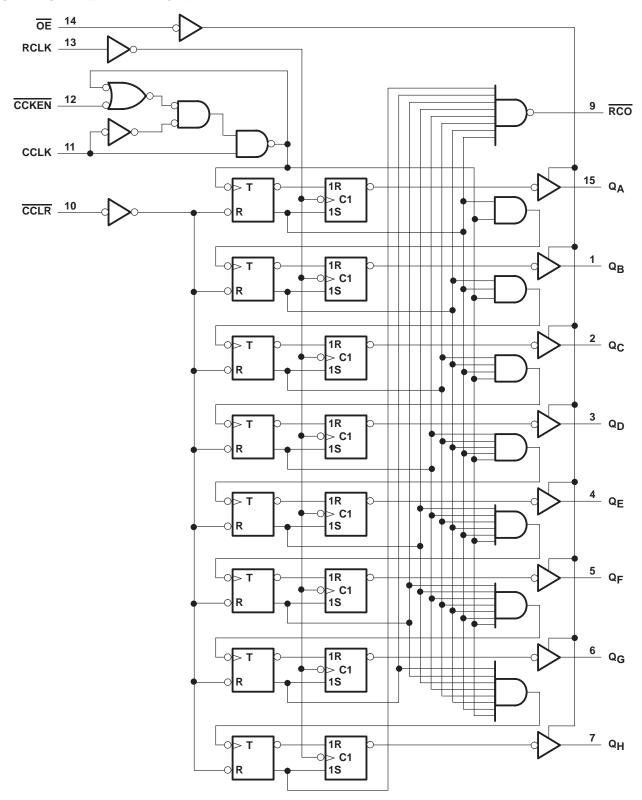


TIMING SEQUENCE

- 1. Clear Counter (asynchronous).
- 2. Count up: 0x01. Store 0x00 in register.
- 3. Inhibit counter clock (CCKEN = HIGH). Store 0x01 in register.
- 4. Count 0x02, 0x03.
- 5. 3-state the outputs
- 6. Count up: 0x04
- 7. Enable outputs.
- 8. Continue up: 0x05
- 9. Store 0x05 in register.
- 10. Continue counting: 0x06...0xFD, 0xFE, 0xFF, 0x00, etc.
- 11. Store 0x00 in register.



logic diagram (positive logic)



Pin numbers shown are for the D, DW, J, N, and W packages.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| Supply voltage range, V _{CC} | | 0.5 V to 7 V |
|--|-----------------|----------------|
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see | ee Note 1) | ±20 mA |
| Output clamp current, IOK (VO < 0 or VO > VC | c) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | | ±35 mA |
| Continuous current through V _{CC} or GND | | ±70 mA |
| Package thermal impedance, θ _{JA} (see Note 2) | : D package | 73°C/W |
| | DW package | 57°C/W |
| | N package | 67°C/W |
| Storage temperature range, T _{sto} | | –65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

| | | | SN | 54HC59 | 0A | SN | 74HC590 |)A | |
|------------------|---------------------------------------|-------------------------|------|--------|------|------|---------|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | UNIT |
| Vcc | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| | | V _{CC} = 2 V | 1.5 | | | 1.5 | | | |
| V_{IH} | High-level input voltage | V _{CC} = 4.5 V | 3.15 | | | 3.15 | | | V |
| | | VCC = 6 V | 4.2 | | | 4.2 | | | |
| | | V _{CC} = 2 V | | | 0.5 | | | 0.5 | |
| VIL | Low-level input voltage | V _{CC} = 4.5 V | | | 1.35 | | | 1.35 | V |
| | | VCC = 6 V | | | 1.8 | | | 1.8 | |
| VI | Input voltage | | 0 | | VCC | 0 | | VCC | V |
| ٧o | Output voltage | | 0 | | VCC | 0 | | VCC | V |
| | | V _{CC} = 2 V | | | 1000 | | | 1000 | |
| t _t ‡ | Input transition (rise and fall) time | V _{CC} = 4.5 V | | | 500 | | | 500 | ns |
| | | V _{CC} = 6 V | | | 400 | | | 400 | |
| TA | Operating free-air temperature | | -55 | | 125 | -40 | | 85 | °C |

[‡] If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CCLK and RCLK inputs are not ensured while in the shift, count, or toggle operating modes.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | | CONDITIONS | ., | Т | A = 25°C | ; | SN54H | C590A | SN74H | C590A | |
|-----------|----------------------|---|---------------|------|----------|------|-------|-------|-------|-------|------|
| PARAMETER | TEST | CONDITIONS | VCC | MIN | TYP | MAX | MIN | MAX | MIN | MAX | UNIT |
| | | | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | |
| | | I _{OH} = -20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| Voн | VI = VIH or VIL | \overline{RCO} , $I_{OH} = -4 \text{ mA}$ | 45.77 | 3.98 | 4.3 | | 3.7 | | 3.84 | | V |
| | | $Q_A - Q_H$, $I_{OH} = -6$ mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | \overline{RCO} , $I_{OH} = -5.2 \text{ mA}$ | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | $Q_A - Q_H$, $I_{OH} = -7.8 \text{ mA}$ | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| | | | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| VOL | VI = VIH or VIL | \overline{RCO} , $I_{OL} = 4 \text{ mA}$ | 45.7 | | 0.17 | 0.26 | | 0.4 | | 0.33 | V |
| | | Q_A-Q_H , $I_{OL}=6$ mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | \overline{RCO} , $I_{OL} = 5.2 \text{ mA}$ | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| | | Q_A-Q_H , $I_{OL} = 7.8 \text{ mA}$ | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| lį | $V_I = V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| loz | $V_O = V_{CC}$ or 0 | | 6 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μΑ |
| ICC | $V_I = V_{CC}$ or 0, | I _O = 0 | 6 V | | | 8 | | 160 | | 80 | μΑ |
| Ci | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | 1 | T _A = | 25°C | SN54H | C590A | SN74H | C590A | |
|-----------------|-----------------|-----------------------------------|-------|------------------|------|-------|-------|-------|-------|------|
| | | | VCC | MIN | MAX | MIN | MAX | MIN | MAX | UNIT |
| | | | 2 V | | 4 | | 2.5 | | 3.2 | |
| fclock | Clock frequency | | 4.5 V | | 20 | | 13 | | 16 | MHz |
| | | | 6 V | | 24 | | 16 | | 19 | |
| | | | 2 V | 125 | | 200 | | 155 | | |
| | | CCLK or RCLK high or low | 4.5 V | 25 | | 38 | | 31 | | |
| | Dulas dunation | | 6 V | 21 | | 32 | | 26 | | |
| t _W | Pulse duration | | 2 V | 100 | | 150 | | 125 | | ns |
| | | CCLR low | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 26 | | 21 | | |
| | | | 2 V | 100 | | 150 | | 125 | | |
| | | CCKEN low before CCLK↑ | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 26 | | 21 | | |
| | | | 2 V | 100 | | 150 | | 125 | | |
| t _{su} | Setup time | CCLR high (inactive) before CCLK↑ | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | | 6 V | 17 | | 26 | | 21 | | |
| | | | 2 V | 100 | | 150 | | 125 | | |
| | | CCLK↑ before RCLK↑† | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 26 | | 21 | | |
| | | | 2 V | 50 | | 75 | | 60 | | |
| th | Hold time | CCKEN low after CCLK↑ | 4.5 V | 10 | | 15 | | 12 | | ns |
| | | | 6 V | 9 | | 13 | | 11 | | |

[†] This setup time ensures that the register gets stable data from the counter outputs. The clocks may be tied together, in which case the register is one clock pulse behind the counter.



switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| | | | | SN54HC590A | | | | | |
|------------------|-----------------|----------------|-----------------|------------|------------------------------------|-----|-----|-----|------|
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | ν _{CC} | T, | T _A = 25°C N TYP MAX | | | | UNIT |
| | (1141-01) | (001701) | | MIN | TYP | MAX | MIN | MAX | |
| | | | 2 V | 4 | 8 | | 2.5 | | |
| f _{max} | | | 4.5 V | 20 | 35 | | 13 | | MHz |
| | | | 6 V | 24 | 40 | | 16 | | |
| | | | 2 V | | 80 | 150 | | 225 | |
| ^t pd | CCLK↑ | RCO | 4.5 V | | 20 | 31 | | 45 | ns |
| , . | | | 6 V | | 15 | 26 | | 38 | |
| | | | 2 V | | 70 | 130 | | 195 | |
| ^t PLH | CCLR↓ | RCO | 4.5 V | | 18 | 28 | | 39 | ns |
| | | | 6 V | | 14 | 23 | | 33 | |
| | | | 2 V | | 70 | 140 | | 210 | |
| ^t pd | RCLK↑ | Q | 4.5 V | | 18 | 31 | | 42 | ns |
| ρ | | | 6 V | | 14 | 25 | | 36 | |
| | | | 2 V | | 80 | 125 | | 185 | |
| t _{en} | ŌĒ↓ | Q | 4.5 V | | 20 | 30 | | 37 | ns |
| 0 | | | 6 V | | 15 | 28 | | 31 | |
| | | | 2 V | | 80 | 125 | | 185 | |
| ^t dis | ŌĒ↑ | Q | 4.5 V | | 20 | 30 | | 37 | ns |
| alo | | | 6 V | | 15 | 28 | | 31 | |
| | | | 2 V | | 38 | 75 | | 110 | |
| | | RCO | 4.5 V | | 8 | 15 | | 22 | |
| | | | 6 V | | 6 | 13 | | 19 | |
| t _t * | | | 2 V | | 38 | 60 | | 90 | ns |
| | | Q | 4.5 V | | 8 | 12 | | 18 | |
| | | | 6 V | | 6 | 10 | | 15 | |

^{*} This parameter is not production tested for the SN54HC590A.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| | | | | | SN | 74HC590 | 0A | | |
|---|-----------------|----------------|-------|-----|----------|---------|-----|-----|------|
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | VCC | T, | Δ = 25°C | ; | | | UNIT |
| | (INFOT) | (0011-01) | | MIN | TYP | MAX | MIN | MAX | |
| | | | 2 V | 4 | 8 | | 3.2 | | |
| f _{max} | | | 4.5 V | 20 | 35 | | 16 | | MHz |
| | | | 6 V | 24 | 40 | | 19 | | |
| | | | 2 V | | 80 | 150 | | 190 | |
| ^t pd | CCLK↑ | RCO | 4.5 V | | 20 | 30 | | 38 | ns |
| r - | | | 6 V | | 15 | 26 | | 33 | |
| | | | 2 V | | 70 | 130 | | 165 | |
| t _{PLH} | CCLR↓ | RCO | 4.5 V | | 18 | 26 | | 33 | ns |
| | | | 6 V | | 14 | 22 | | 28 | |
| | | | 2 V | | 70 | 140 | | 175 | |
| t _{pd} | RCLK↑ | Q | 4.5 V | | 18 | 28 | | 35 | ns |
| r - | | | 6 V | | 14 | 24 | | 30 | |
| | | | 2 V | | 80 | 125 | | 155 | |
| t _{en} | ŌĒ↓ | Q | 4.5 V | | 20 | 25 | | 31 | ns |
| • | | | 6 V | | 15 | 21 | | 26 | |
| | | | 2 V | | 80 | 125 | | 155 | |
| ^t dis | ŌĒ↑ | Q | 4.5 V | | 20 | 25 | | 31 | ns |
| | | | 6 V | | 15 | 21 | | 26 | |
| | | | 2 V | | 38 | 75 | | 95 | |
| | | RCO | 4.5 V | | 8 | 15 | | 19 | 1 |
| | | | 6 V | | 6 | 13 | | 16 |] |
| t _t | | | 2 V | | 38 | 60 | | 75 | ns |
| | | Q | 4.5 V | | 8 | 12 | | 15 | 1 |
| | | | 6 V | | 6 | 10 | | 13 | 1 |

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

| | | | | | SN | 54HC59 | 0A | | |
|------------------|-------------------|----------------|-------|-----|----------|--------|------|-----|------|
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | VCC | ΤΔ | √ = 25°C | ; | MINI | MAY | UNIT |
| | (1141 01) | (0011 01) | | MIN | TYP | MAX | MIN | MAX | |
| | | | 2 V | | 100 | 300 | | 447 | |
| ^t pd | RCLK [↑] | Q | 4.5 V | | 24 | 60 | | 90 | ns |
| · | | | 6 V | | 20 | 51 | | 77 | |
| | | | 2 V | | 90 | 200 | | 300 | |
| t _{en} | ŌĒ | Q | 4.5 V | | 23 | 40 | | 60 | ns |
| | | | 6 V | | 19 | 34 | | 51 | |
| | | | 2 V | | 45 | 210 | | 315 | |
| t _t * | | Q | 4.5 V | | 17 | 42 | | 63 | ns |
| | | | 6 V | | 13 | 36 | | 53 | |

^{*} This parameter is not production tested for the SN54HC590A.

switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

| | | | | | SN | 74HC59 | 0A | | |
|-----------------|-------------------|----------------|-------|-----|--------|--------|------|-----|------|
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | VCC | TA | = 25°C | ; | MINI | MAY | UNIT |
| | (1141 01) | (0011 01) | | MIN | TYP | MAX | MIN | MAX | |
| | | | 2 V | | 100 | 300 | | 380 | |
| ^t pd | RCLK [↑] | Q | 4.5 V | | 24 | 60 | | 76 | ns |
| • | | | 6 V | | 20 | 51 | | 65 | |
| | | | 2 V | | 90 | 200 | | 250 | |
| t _{en} | ŌĒ | Q | 4.5 V | | 23 | 40 | | 50 | ns |
| | | | 6 V | | 19 | 34 | | 43 | |
| | | | 2 V | | 45 | 210 | | 265 | |
| t _t | | Q | 4.5 V | | 17 | 42 | | 53 | ns |
| | | | 6 V | | 13 | 36 | | 45 | |

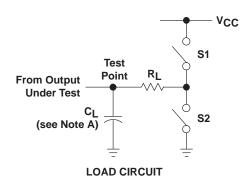
operating characteristics, $T_A = 25^{\circ}C$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | No load | 250 | pF |

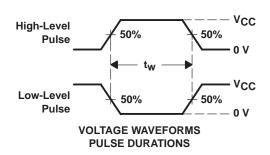


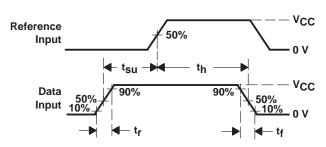
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PARAMETER MEASUREMENT INFORMATION

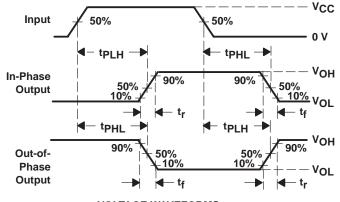


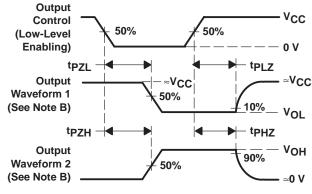
| DADAI | METER | Ь. | Cı | S1 | S2 |
|--------------------|-----------|--------------|-----------------------|--------|--------|
| FANAI | AIC L CK | RL | ∪_L | 31 | 32 |
| 1. | tPZH | 1 k Ω | 50 pF or | Open | Closed |
| ten | tPZL | 1 K22 | 150 pF | Closed | Open |
| | tPHZ | 410 | | Open | Closed |
| ^t dis | tPLZ | 1 k Ω | 50 pF | Closed | Open |
| t _{pd} or | tpd or tt | | 50 pF or 150 pF | Open | Open |





VOLTAGE WAVEFORMS SETUP AND HOLD AND INPUT RISE AND FALL TIMES





VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_r = 6 ns, t_f = 6 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms









PACKAGING INFORMATION

| 5962-89603012A ACTIVE LCCC FK 20 1 TBD POST-PLATE N / A for Pkg Type 5962-8960301EA ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type 5962-8960301EA ACTIVE CDIP W 16 1 TBD A42 SNPB N / A for Pkg Type SN54HC590AD ACTIVE CDIP J 16 40 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/B1) SN74HC590ADE4 ACTIVE SOIC D 16 40 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/B1) SN74HC590ADG4 ACTIVE SOIC D 16 2500 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/B1) SN74HC590ADR ACTIVE SOIC D 16 2500 Green (RoHS & CU NIPDAU Level-1-260C-UNLIM no Sb/B1) SN74HC590ADR64 ACTIVE SOIC D 16 250 Green (ROHS & CU NIPDAU Level-1-260C-UNLIM no Sb/B1) SN74HC590ADT4 ACTIVE SOIC D < | Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | e Eco Plan ⁽²⁾ | Lead/Ball Finish | n MSL Peak Temp ⁽³⁾ |
|--|------------------|-----------------------|-----------------|--------------------|------|----------------|---------------------------|------------------|--------------------------------|
| S962-8960301FA | 5962-89603012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SN54HC590AD | 5962-8960301EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74HC590AD | 5962-8960301FA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74HC590ADE4 | SN54HC590AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74HC590ADG4 | SN74HC590AD | ACTIVE | SOIC | D | 16 | 40 | | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADR | SN74HC590ADE4 | ACTIVE | SOIC | D | 16 | 40 | ` | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADRE4 | SN74HC590ADG4 | ACTIVE | SOIC | D | 16 | 40 | , | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADRG4 | SN74HC590ADR | ACTIVE | SOIC | D | 16 | 2500 | , | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADT | SN74HC590ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | ` | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADTG4 | SN74HC590ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | , | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADTG4 | SN74HC590ADT | ACTIVE | SOIC | D | 16 | 250 | | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADW | SN74HC590ADTE4 | ACTIVE | SOIC | D | 16 | 250 | | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADWG4 | SN74HC590ADTG4 | ACTIVE | SOIC | D | 16 | 250 | | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADWR | SN74HC590ADW | ACTIVE | SOIC | DW | 16 | 40 | ` | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590ADWRG4 | SN74HC590ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | ` | CU NIPDAU | Level-1-260C-UNLIM |
| N74HC590AN ACTIVE PDIP N 16 25 Pb-Free (RoHS) CU NIPDAU N / A for Pkg Type SN74HC590AN3 OBSOLETE PDIP N 16 TBD Call TI Call TI SN74HC590ANE4 ACTIVE PDIP N 16 25 Pb-Free (RoHS) CU NIPDAU N / A for Pkg Type SNJ54HC590AFK ACTIVE LCCC FK 20 1 TBD POST-PLATE N / A for Pkg Type SNJ54HC590AJ ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type | SN74HC590ADWR | ACTIVE | SOIC | DW | 16 | 2000 | , | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590AN3 OBSOLETE PDIP N 16 TBD Call TI Call TI | SN74HC590ADWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | | CU NIPDAU | Level-1-260C-UNLIM |
| SN74HC590AN3 OBSOLETE PDIP N 16 TBD Call TI Call TI SN74HC590ANE4 ACTIVE PDIP N 16 25 Pb-Free (RoHS) CU NIPDAU N / A for Pkg Type SNJ54HC590AFK ACTIVE LCCC FK 20 1 TBD POST-PLATE N / A for Pkg Type SNJ54HC590AJ ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type | SN74HC590AN | ACTIVE | PDIP | N | 16 | 25 | | CU NIPDAU | N / A for Pkg Type |
| (RoHS) SNJ54HC590AFK ACTIVE LCCC FK 20 1 TBD POST-PLATE N / A for Pkg Type SNJ54HC590AJ ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type | SN74HC590AN3 | OBSOLETE | PDIP | N | 16 | | | Call TI | Call TI |
| SNJ54HC590AJ ACTIVE CDIP J 16 1 TBD A42 SNPB N / A for Pkg Type | SN74HC590ANE4 | ACTIVE | PDIP | N | 16 | 25 | | CU NIPDAU | N / A for Pkg Type |
| • <i>7</i> | SNJ54HC590AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54HC590AW ACTIVE CFP W 16 1 TBD A42 N / A for Pkg Type | SNJ54HC590AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| | SNJ54HC590AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

9-Oct-2007

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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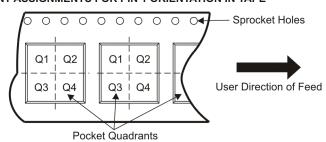
TAPE AND REEL INFORMATION





| | Dimension designed to accommodate the component width |
|----|---|
| В0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|-----------------|--------------------|----|------|--------------------------|--------------------------|---------|---------|---------|------------|-----------|------------------|
| SN74HC590ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC590ADWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |





*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC590ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC590ADWR | SOIC | DW | 16 | 2000 | 346.0 | 346.0 | 33.0 |

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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