- Single-Rail Outputs on 'LS399
- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock
- Applications:

Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability

Universal Type Register for Implementing Various Shift Patterns: Even Has Compound Left-Right Capabilities

description

This monolithic quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54LS157/SN74LS157 and SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the positive-going edge of the clock pulse.

Typical power dissipation is 37 milliwatts. The SN54LS399 is characterized for operation over the full military range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The SN74LS399 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

FUNCTION TABLE

	INPUTS			OUTPUTS				
	WORD ELECT	CLOCK	QΑ	αB	σc	σ_{D}		
Г	L	1	a1	b1	c1	d1		
·	н	1	a2	b2	c2	d2		
	X	L	Q _{A0}	α_{B0}	σ_{C0}	σ_{D0}		

SN54LS399 . . . J OR W PACKAGE SN74LS399 . . . D OR N PACKAGE (TOP VIEW)

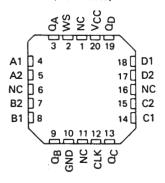
WS 1 1 16 VCC
QA 2 15 QD
A1 3 14 D1
A2 4 13 D2
B2 5 12 C2
B1 6 11 C1

GND □8

SN54LS399 . . . FK PACKAGE (TOP VIEW)

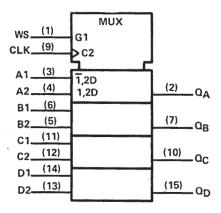
10 Q QC

9 CLK



NC - No internal connection

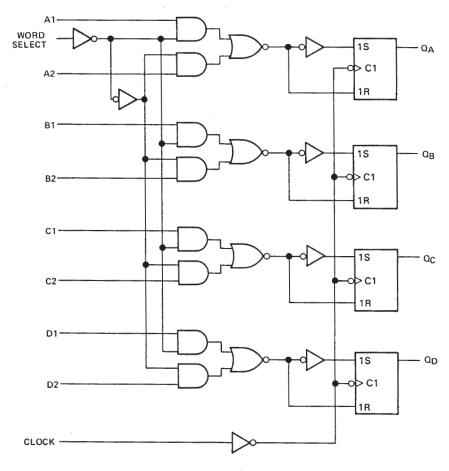
logic symbol[†]



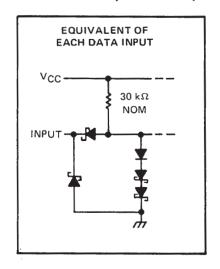
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

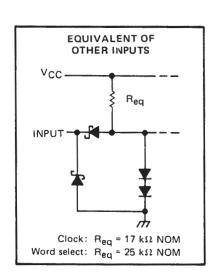
Pin numbers shown are for D, J, N, and W packages.

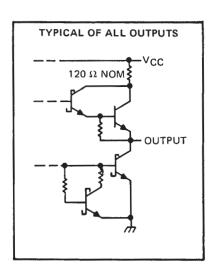
logic diagram (positive logic)



schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 \	✓
Input voltage	7 \	✓
Operating free-air temperature range: SN54LS399	-55°C to 125°C	C
SN74LS399	0°C to 70°0	0
Storage temperature range	-65°C to 150°C	C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54LS399		SN74LS399				
· · · · · · · · · · · · · · · · · · ·		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				-400			-400	μА
Low-level output current, IOL				4			8	mA
Width of clock pulse, high or low level, tw		20			20			ns
Setup time, t _{su}	Data	25			25			ns
octop time, t _{su}	Word select	45			45			
Hold time, th	Data	0			0			
Thora time, th	Word select	0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°c

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS399		399	SN74LS399				
	N N		MIN	ТҮР‡	MAX	MIN	ТҮР‡	MAX	UNIT		
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
, V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I =18 mA				-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = V _{IL} max	V _{IH} = 2 V, I _{OH} = -400 μA		2.5	3.4		2.7	3.4		V
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V,	I _{OL} = 4 mA		0.25	0.4		0.25 0.35	0.4	V
'I ₁	Input current at maximum input voltage	V _{CC} = MAX,	V ₁ = 7 V	TOL TOTAL			0.1		0.35	0.5	mA
ЧН	High-level input current	V _{CC} = MAX,	V _I = 2.7 V				20			20	μΑ
ΊL	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V				-0.4			-0.4	mA
los	Short-circuit output current§	V _{CC} = MAX			-20		-100	-20		-100	mA
1CC	Supply current	V _{CC} = MAX,	See Note 2	•		7.3	13		7.3	13	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	C _L = 15 pF,	$R_L = 2 k\Omega$,		18	27	
tPHL	Propagation delay time, high-to-low-level output	See Note 3			21	32	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



 $[\]ddagger$ AII typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time, duration of the short-circuit should not exceed one second .

NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input,

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dsp.ti.com	Broadband	www.ti.com/broadband
interface.ti.com	Digital Control	www.ti.com/digitalcontrol
logic.ti.com	Military	www.ti.com/military
power.ti.com	Optical Networking	www.ti.com/opticalnetwork
microcontroller.ti.com	Security	www.ti.com/security
www.ti.com/lpw	Telephony	www.ti.com/telephony
	Video & Imaging	www.ti.com/video
	Wireless	www.ti.com/wireless
	dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com	amplifier.ti.com dataconverter.ti.com dsp.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti.com/lpw Audio Audio Audio Audio Automotive Broadband Digital Control Military Optical Networking Security Telephony Video & Imaging

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interface.ti.com	Digital Control	www.ti.com/digitalcontrol
logic.ti.com	Military	www.ti.com/military
power.ti.com	Optical Networking	www.ti.com/opticalnetwork
microcontroller.ti.com	Security	www.ti.com/security
www.ti.com/lpw	Telephony	www.ti.com/telephony
	Video & Imaging	www.ti.com/video
	Wireless	www.ti.com/wireless
	dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com	amplifier.ti.com dataconverter.ti.com dsp.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti.com/lpw Audio Audio Audio Audio Automotive Broadband Digital Control Military Optical Networking Security Telephony Video & Imaging



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)	
84154012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
8415401EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type	
8415401EA	ACTIVE	CDIP	J	16	1	1 TBD A42 SNPB		N / A for Pkg Type	
8415401FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
8415401FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SN54LS399J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type	
SN54LS399J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type	
SN74LS399D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74LS399DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74LS399N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS399N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS399N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS399N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	
SN74LS399NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS399NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS399NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399NSR	ACTIVE	so	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS399NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54LS399FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS399FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS399J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type	
SNJ54LS399J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type	



PACKAGE OPTION ADDENDUM

9-Oct-2007

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins P	ackage Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SNJ54LS399W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS399W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in

a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS399NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LS399NSR	SO	NS	16	2000	346.0	346.0	33.0	

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

