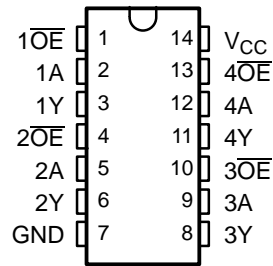


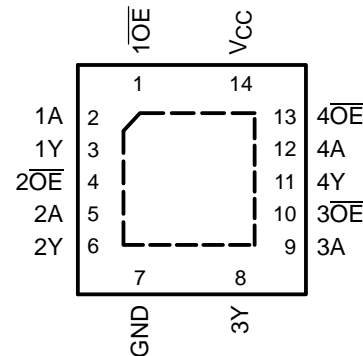
FEATURES

- Operates From 1.65 V to 3.6 V
- Specified From -40°C to 85°C and -40°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

D, DB, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC125A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC125ARGYR	LC125A
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC125AD	LVC125A
		Reel of 2500	SN74LVC125ADR	
		Reel of 250	SN74LVC125ADT	
	SOP – NS	Reel of 2000	SN74LVC125ANSR	LVC125A
	SSOP – DB	Reel of 2000	SN74LVC125ADBR	LC125A
	TSSOP – PW	Tube of 90	SN74LVC125APW	LC125A
Reel of 2000		SN74LVC125APWR		
Reel of 250		SN74LVC125APWT		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

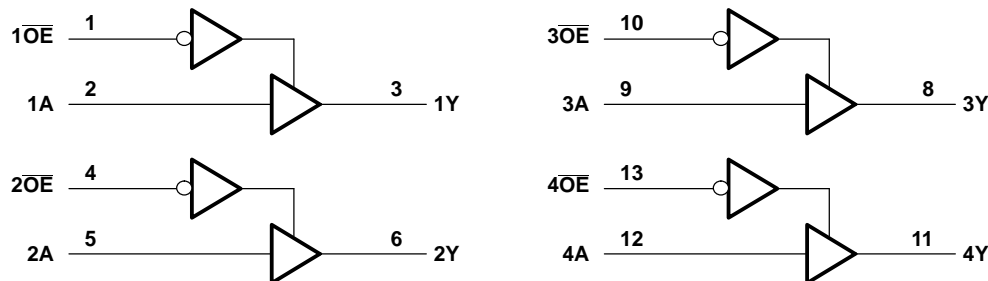
SN74LVC125A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS2900–JANUARY 1993–REVISED AUGUST 2005

**FUNCTION TABLE
(EACH BUFFER)**

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current		-50	$V_I < 0$ mA
I_{OK}	Output clamp current		-50	$V_O < 0$ mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance		86	°C/W
		D package ⁽⁴⁾		
		DB package ⁽⁴⁾	96	
		NS package ⁽⁴⁾	76	
		PW package ⁽⁴⁾	113	
	RGY package ⁽⁵⁾	47		
T_{stg}	Storage temperature range	-65	150	°C
P_{tot}	Power dissipation		500	$T_A = -40^\circ\text{C to } 125^\circ\text{C}^{(6)(7)}$ mW

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions⁽¹⁾

			T _A = 25°C		–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V	2		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V	–4		–4		–4		mA
		V _{CC} = 2.3 V	–8		–8		–8		
		V _{CC} = 2.7 V	–12		–12		–12		
		V _{CC} = 3 V	–24		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		4		mA
		V _{CC} = 2.3 V	8		8		8		
		V _{CC} = 2.7 V	12		12		12		
		V _{CC} = 3 V	24		24		24		
Δt/Δv	Input transition rise or fall rate	8		8		8		ns/V	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3 V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
	I _{OH} = –24 mA	3 V	2.4			2.4		2.25		
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I _{OL} = 4 mA	1.65 V	0.24			0.45		0.6		
	I _{OL} = 8 mA	2.3 V	0.3			0.7		0.75		
	I _{OL} = 12 mA	2.7 V	0.4			0.4		0.6		
	I _{OL} = 24 mA	3 V	0.55			0.55		0.8		
I _I	V _I = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±1			±10		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3 V	5							pF

SN74LVC125A

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS2900–JANUARY 1993–REVISED AUGUST 2005

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

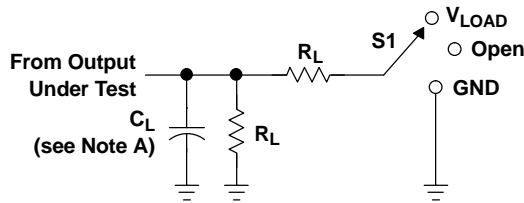
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	1	4.5	11.8	1	12.3	1	13.8	ns
			2.5 V ± 0.2 V	1	2.7	5.8	1	6.3	1	8.4	
			2.7 V	1	3	5.3	1	5.5	1	7	
			3.3 V ± 0.3 V	1	2.5	4.6	1	4.8	1	6	
t _{en}	\overline{OE}	Y	1.8 V ± 0.15 V	1	4.3	13.8	1	14.3	1	15.8	ns
			2.5 V ± 0.2 V	1	2.7	6.9	1	7.4	1	9.5	
			2.7 V	1	3.3	6.4	1	6.6	1	8.5	
			3.3 V ± 0.3 V	1	2.4	5.2	1	5.4	1	7	
t _{dis}	\overline{OE}	Y	1.8 V ± 0.15 V	1	4.3	10.6	1	11.1	1	12.6	ns
			2.5 V ± 0.2 V	1	2.2	5.1	1	5.6	1	7.7	
			2.7 V	1	2.5	4.8	1	5	1	6.5	
			3.3 V ± 0.3 V	1	2.4	4.4	1	4.6	1	6	
t _{sk(o)}			3.3 V ± 0.3 V					1		1.5	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8 V	7.4	pF
			2.5 V	11.3	
			3.3 V	15	

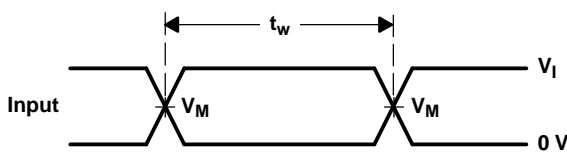
PARAMETER MEASUREMENT INFORMATION



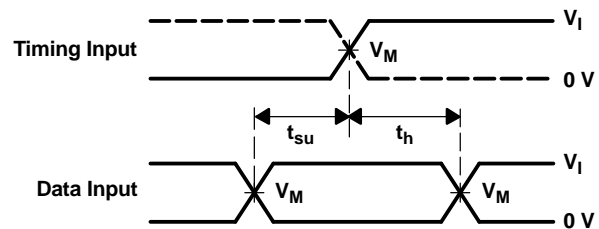
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

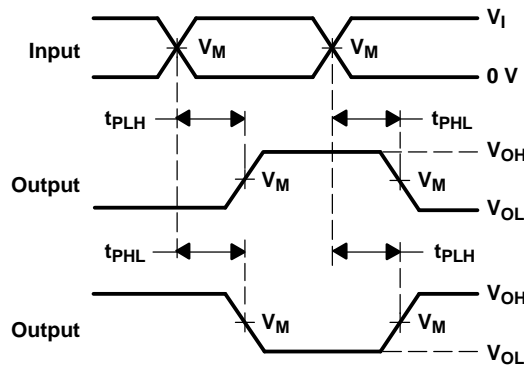
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PZL} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC125AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74LVC125ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ADTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC125APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC125AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LVC125ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVC125ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

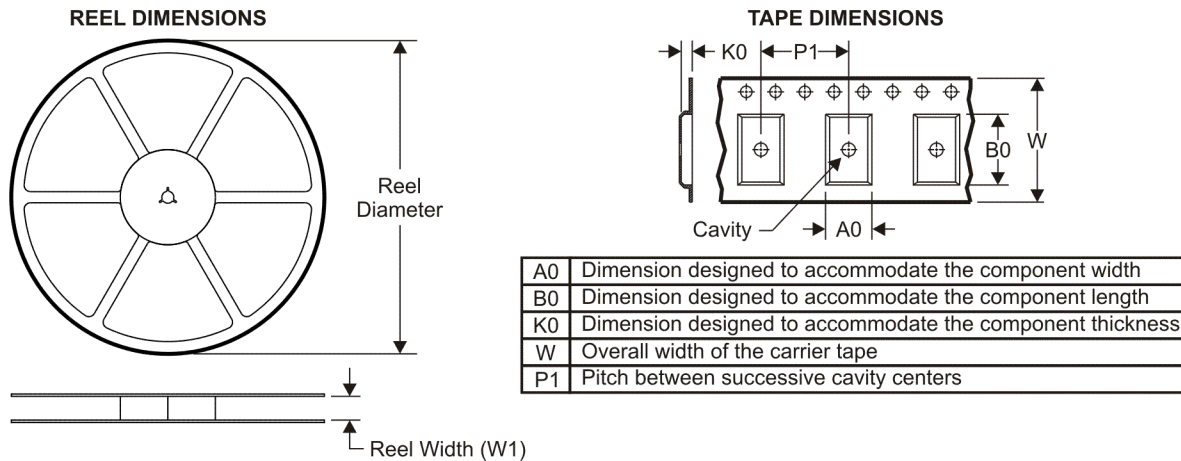
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC125ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVC125ARGYR	QFN	RGY	14	1000	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC125ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LVC125ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LVC125ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC125ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LVC125APWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74LVC125ARGYR	QFN	RGY	14	1000	190.5	212.7	31.8

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G14)

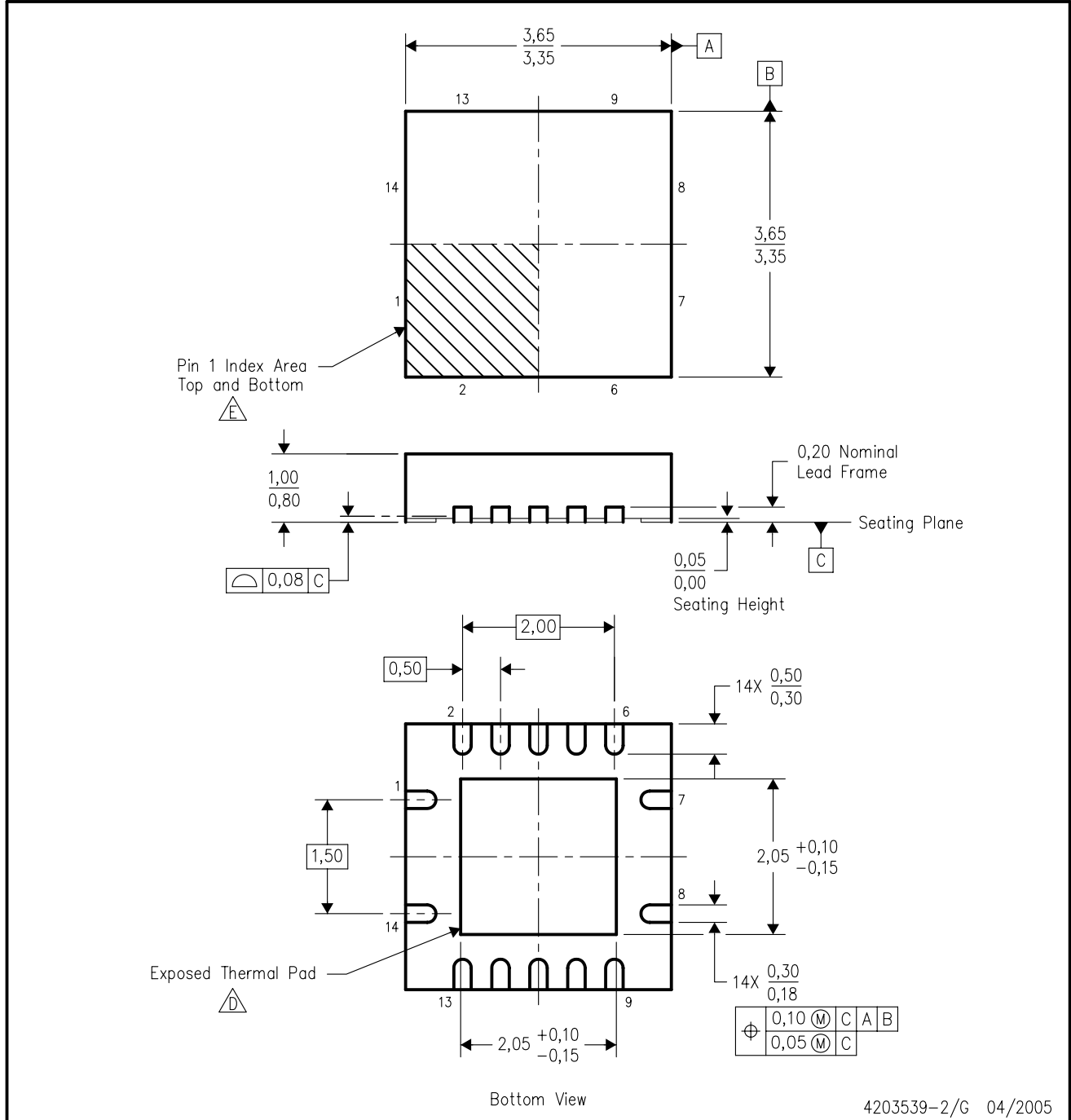
PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



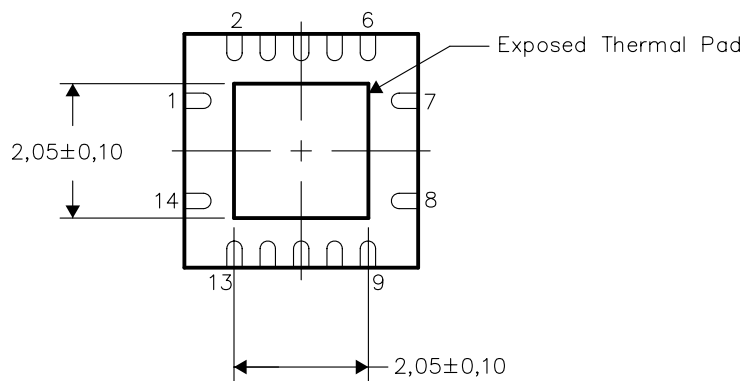
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

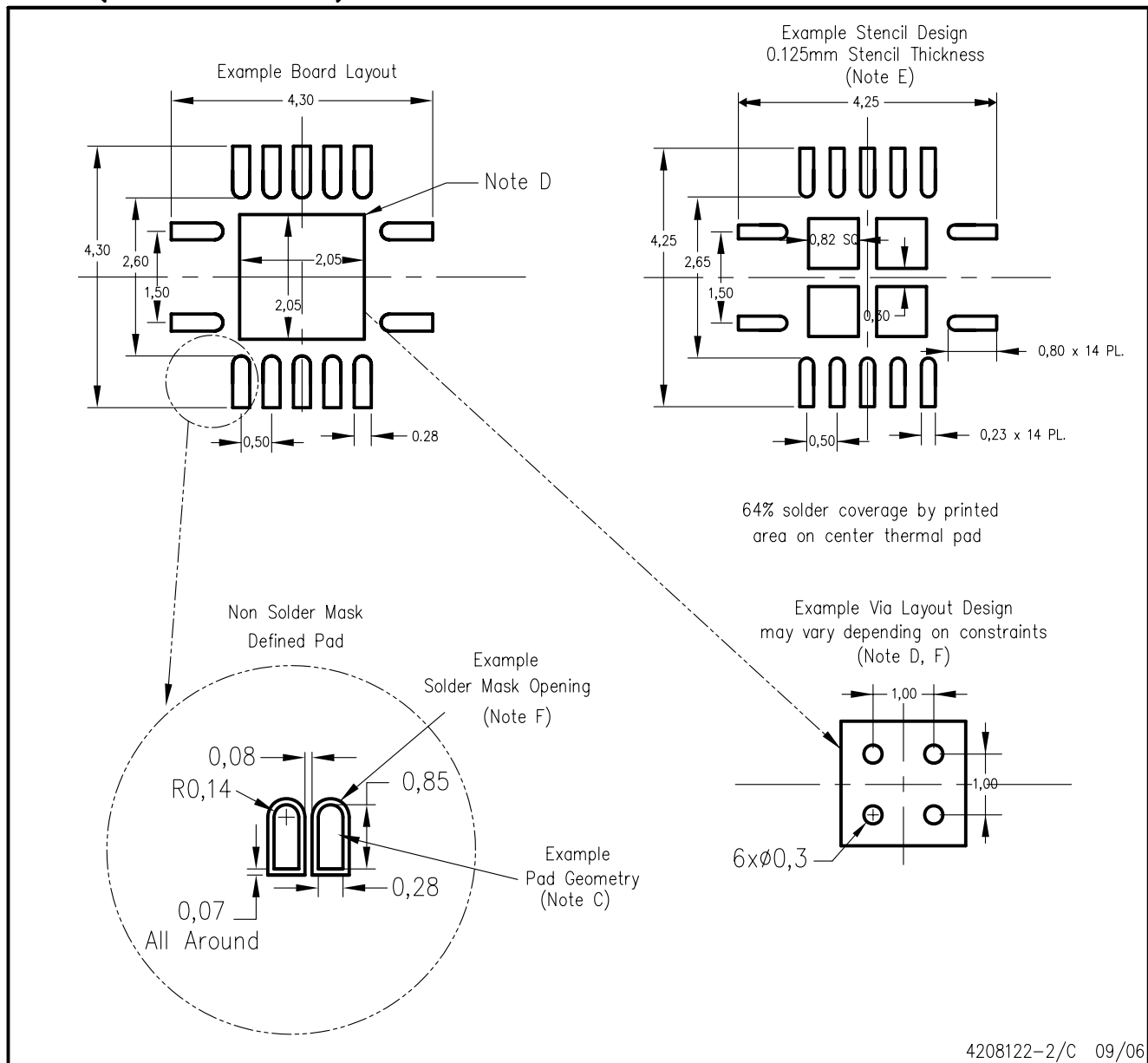


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N14)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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