

SN74S225

16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY WITH 3-STATE OUTPUTS

SDLS207B – SEPTEMBER 1976 – REVISED APRIL 1998

- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits
- DC to 10-MHz Data Rate
- 3-State Outputs
- Packaged in Standard Plastic 300-mil DIPs

description

This 80-bit active-element memory is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words by 5 bits. A memory system using the SN74S225 easily can be expanded in multiples of 48 words or of 10 bits as shown in Figure 3. The 3-state outputs controlled by a single output-enable (\overline{OE}) input make bus connection and multiplexing easy.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from dc to 10 MHz in a bit-parallel format, word by word.

Reading or writing is done independently, utilizing separate asynchronous data clocks. Data can be written into the array on the low-to-high transition of either load-clock (CLKA, CLKB) input. Data can be read out of the array on the low-to-high transition of the unload-clock (UNCK IN) input (normally high). Writing data into the FIFO can be accomplished in one of two ways:

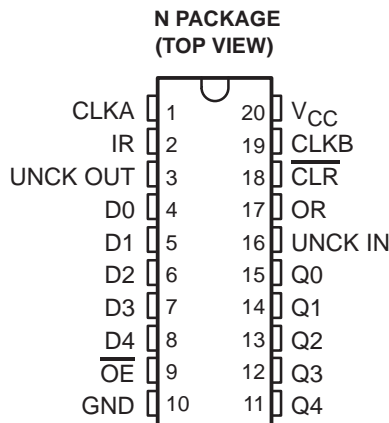
- In applications not requiring a gated clock control, best results are achieved by applying the clock input to one of the clocks while tying the other clock input high.
- In applications needing a gated clock, the load clock (gate control) must be high for the FIFO to load on the next clock pulse.

CLKA and CLKB can be used interchangeably for either clock gate control or clock input.

Status of the SN74S225 is provided by three outputs. The input-ready (IR) output monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload-clock (UNCK OUT) output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready (OR), is high when the first word location contains valid data and UNCK IN is high. When UNCK IN goes low, OR will go low and stay low until new valid data is in the first word position. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are 3-state, with a common control input (\overline{OE}). When \overline{OE} is low, the data outputs are enabled to function as totem-pole outputs. A high logic level forces each data output to a high-impedance state while all other inputs and outputs remain active. The clear (\overline{CLR}) input invalidates all data stored in the memory array by clearing the control logic and setting OR to a low logic level on the high-to-low transition of a low-active pulse.

The SN74S225 is characterized for operation from 0°C to 70°C.



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**TEXAS
INSTRUMENTS**

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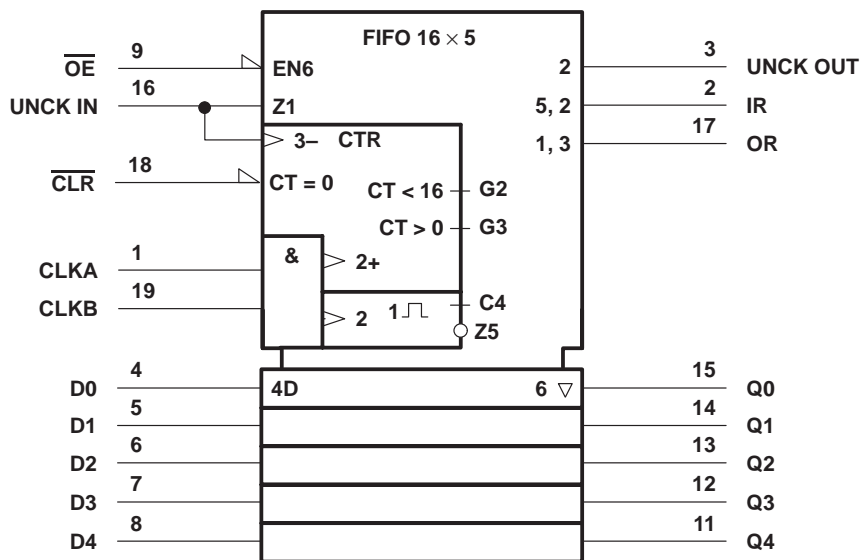
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logic symbol†

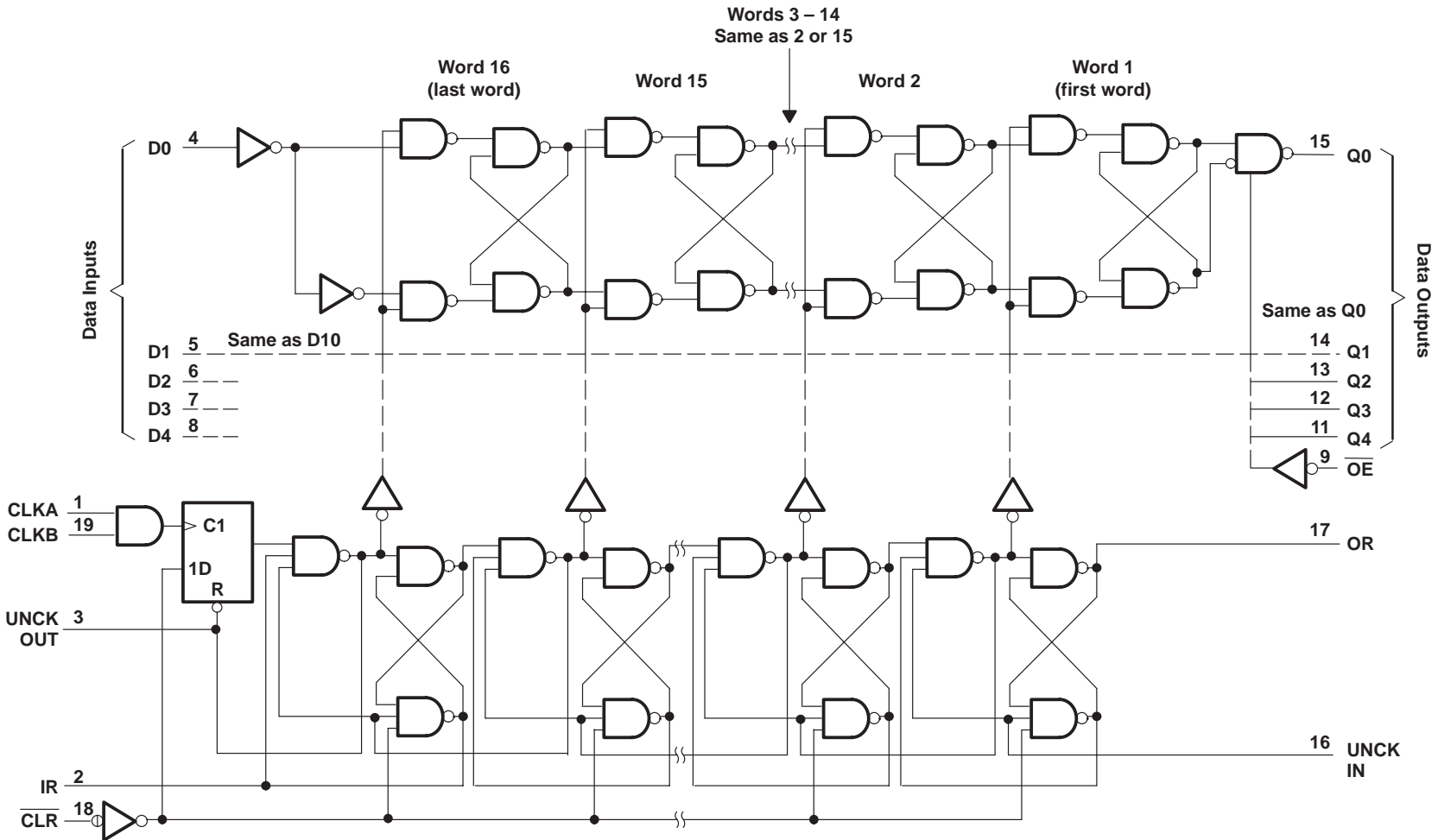


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

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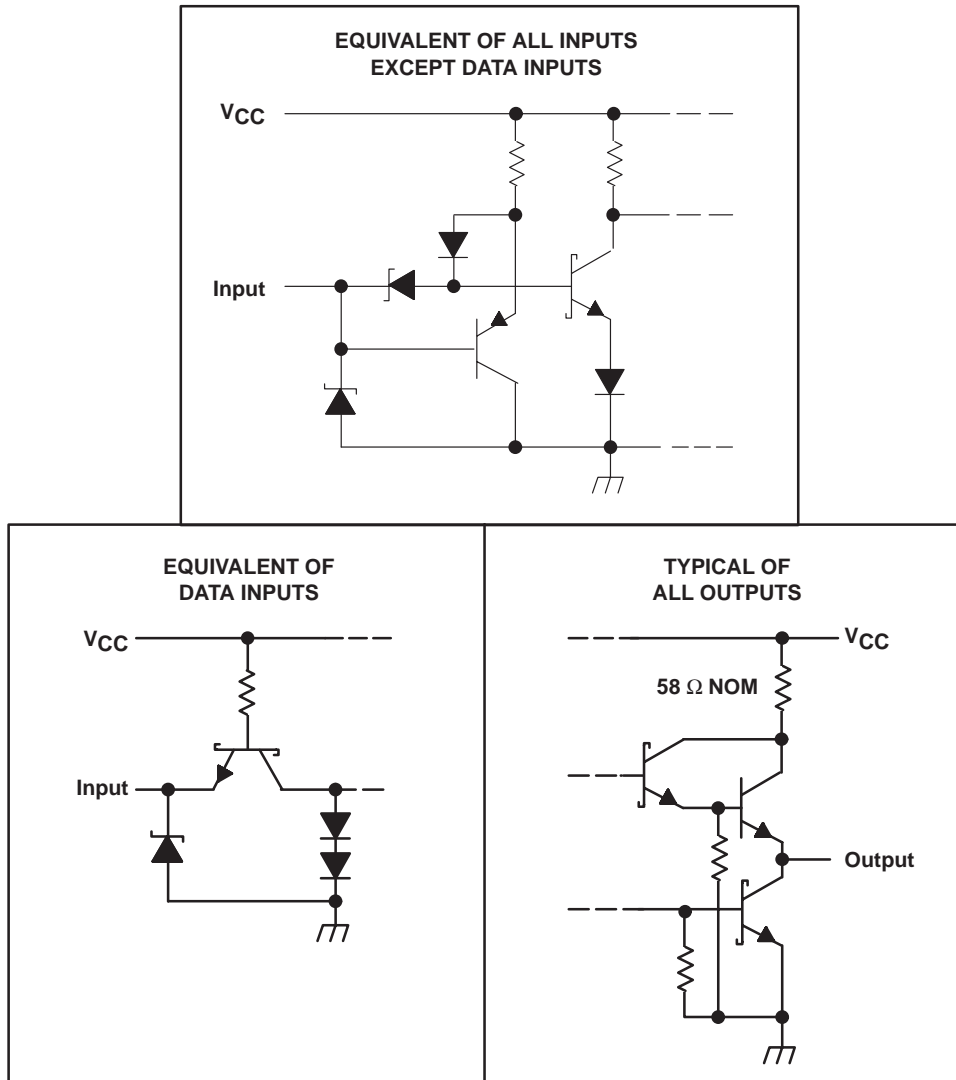
functional block diagram



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	-0.5 V to 7 V
Input voltage range, V_I	-0.5 V to 5.5 V
Off-state output voltage range	-0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 2)	67°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			V
V _{IL}	Low-level input voltage			0.8	V
I _{OH}	High-level output current	Q outputs		-6.5	mA
		All other outputs		-3.2	
I _{OL}	Low-level output current	Q outputs		16	mA
		All other outputs		8	
T _A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.75 V,	I _I = -18 mA			-1.2	V
V _{OH}	Q outputs	V _{CC} = 4.75 V,	I _{OL} = -6.5 mA	2.4	2.9		V
	All others	V _{CC} = 4.75 V,	I _{OL} = -3.2 mA	2.4	2.9		
V _{OL}	Q outputs	V _{CC} = 4.75 V,	I _{OL} = 16 mA		0.35	0.5	V
	All others	V _{CC} = 4.75 V,	I _{OL} = 8 mA		0.35	0.5	
I _{OZH}		V _{CC} = 5.25 V,	V _O = 2.4 V			50	μA
I _{OZL}		V _{CC} = 5.25 V,	V _O = 0.5 V			-50	μA
I _I		V _{CC} = 5.25 V,	V _I = 5.5 V			1	mA
I _{IH}	Data	V _{CC} = 5.25 V,	V _I = 2.7 V			40	μA
	All others					25	
I _{IL}	Data	V _{CC} = 5.25 V,	V _I = 0.5 V			-1	mA
	All others					-0.25	
I _{OS} ‡		V _{CC} = 5.25 V,	V _O = 0	-30		-100	mA
I _{CC} §		V _{CC} = 5.25 V			80	120	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Duration of the short circuit should not exceed one second.

§ I_{CC} is measured with all inputs grounded and the outputs open.

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

		MIN	NOM	MAX	UNIT
f _{clock}	Clock frequency			10	MHz
t _w	Pulse duration	CLKA or CLKB high	25		ns
		UNCK IN low	7		
		CLR low	40		
t _{su}	Setup time before CLKA↑ or CLKB↑	Data (see Note 3)	-20		ns
		CLR inactive	25		
t _h	Hold time after CLKA↑ or CLKB↑		70		ns

NOTE 3: Data must be set up within 20 ns after the load-clock positive transition.



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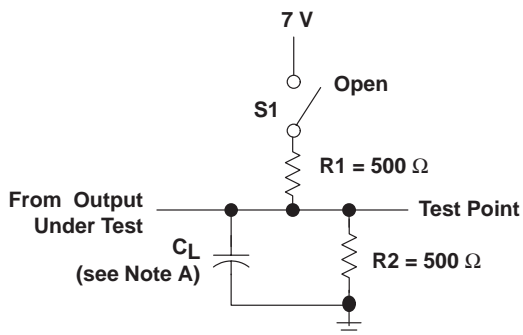
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f _{max}	CLKA		C _L = 30 pF	10	20		MHz
	CLKB			10	20		
	UNCK IN			10	20		
t _w	UNCK OUT		C _L = 30 pF	7	14		ns
t _{dis}	OE	Any Q	C _L = 5 pF		10	25	ns
t _{en}	OE	Any Q	C _L = 30 pF		25	40	ns
t _{PLH}	UNCK IN	Any Q	C _L = 30 pF		50	75	ns
t _{PHL}					50	75	
t _{PLH}	CLKA or CLKB	OR	C _L = 30 pF		190	300	ns
t _{PLH}	UNCK IN	OR	C _L = 30 pF		40	60	ns
t _{PHL}					30	45	
t _{PHL}	CLR	OR	C _L = 30 pF		35	60	ns
	CLKA or CLKB	UNCK OUT			25	45	
	UNCK IN				270	400	
	CLKA or CLKB	IR			55	75	
t _{PLH}	UNCK IN	IR	C _L = 30 pF		255	400	ns
	CLR				16	35	
	OR↑			Any Q		10	

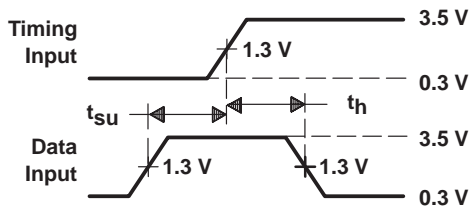
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

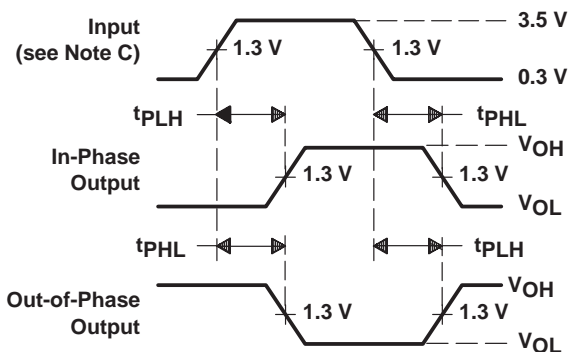


LOAD CIRCUIT FOR 3-STATE OUTPUTS

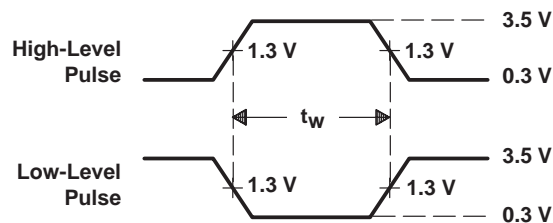
PARAMETER	S1	
t_{en}	tpZH	Open
	tpZL	Closed
t_{dis}	tPHZ	Open
	tPLZ	Closed
t_{pd}	tPLH	Open
	tPHL	Open



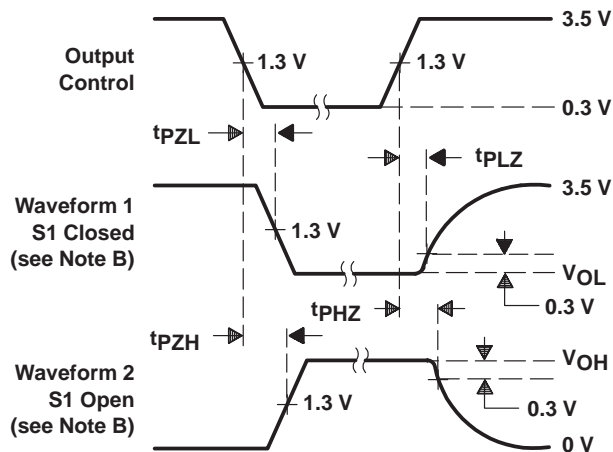
**VOLTAGE WAVEFORMS
SET UP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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APPLICATION INFORMATION

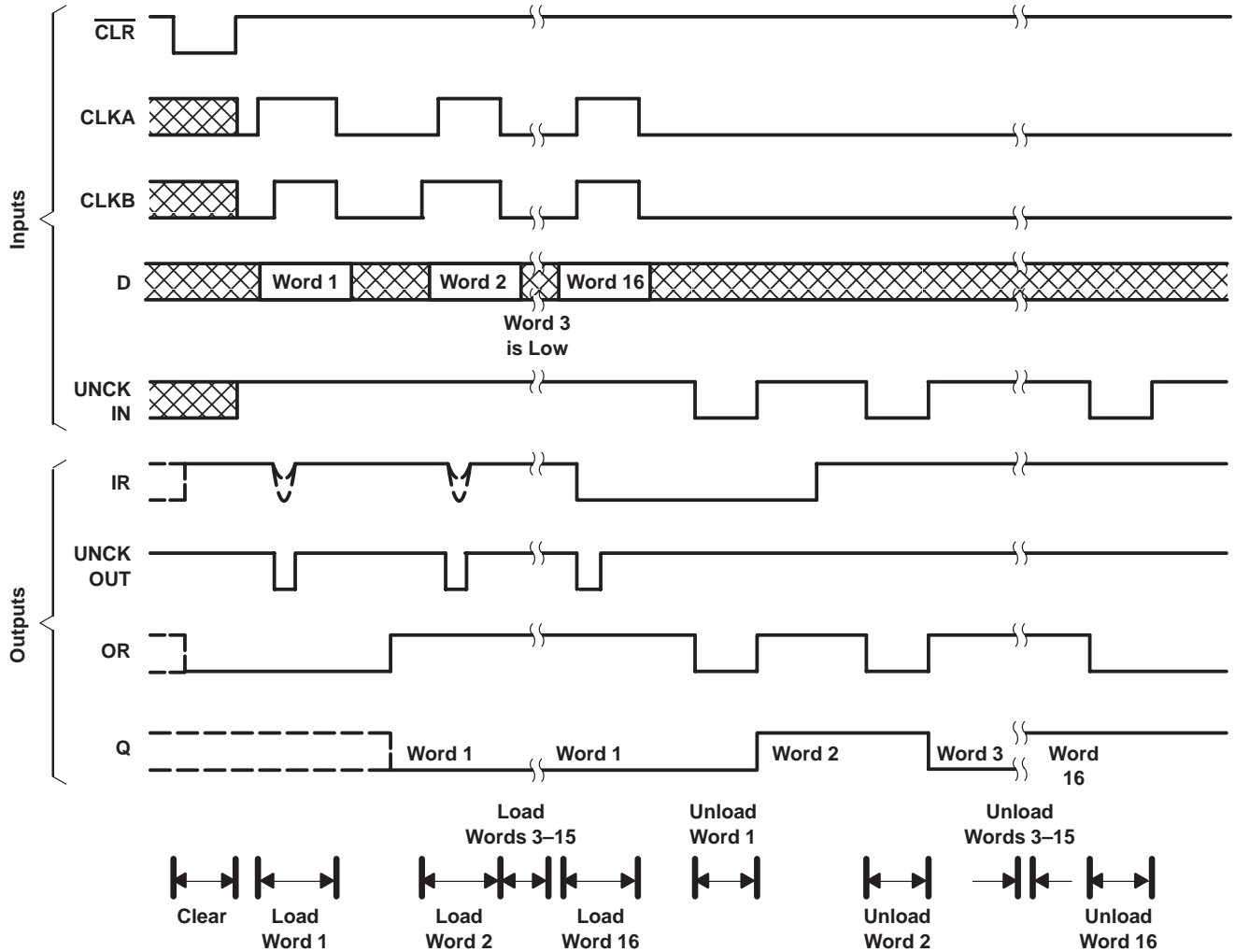


Figure 2. Typical Waveforms for a 16-Word FIFO

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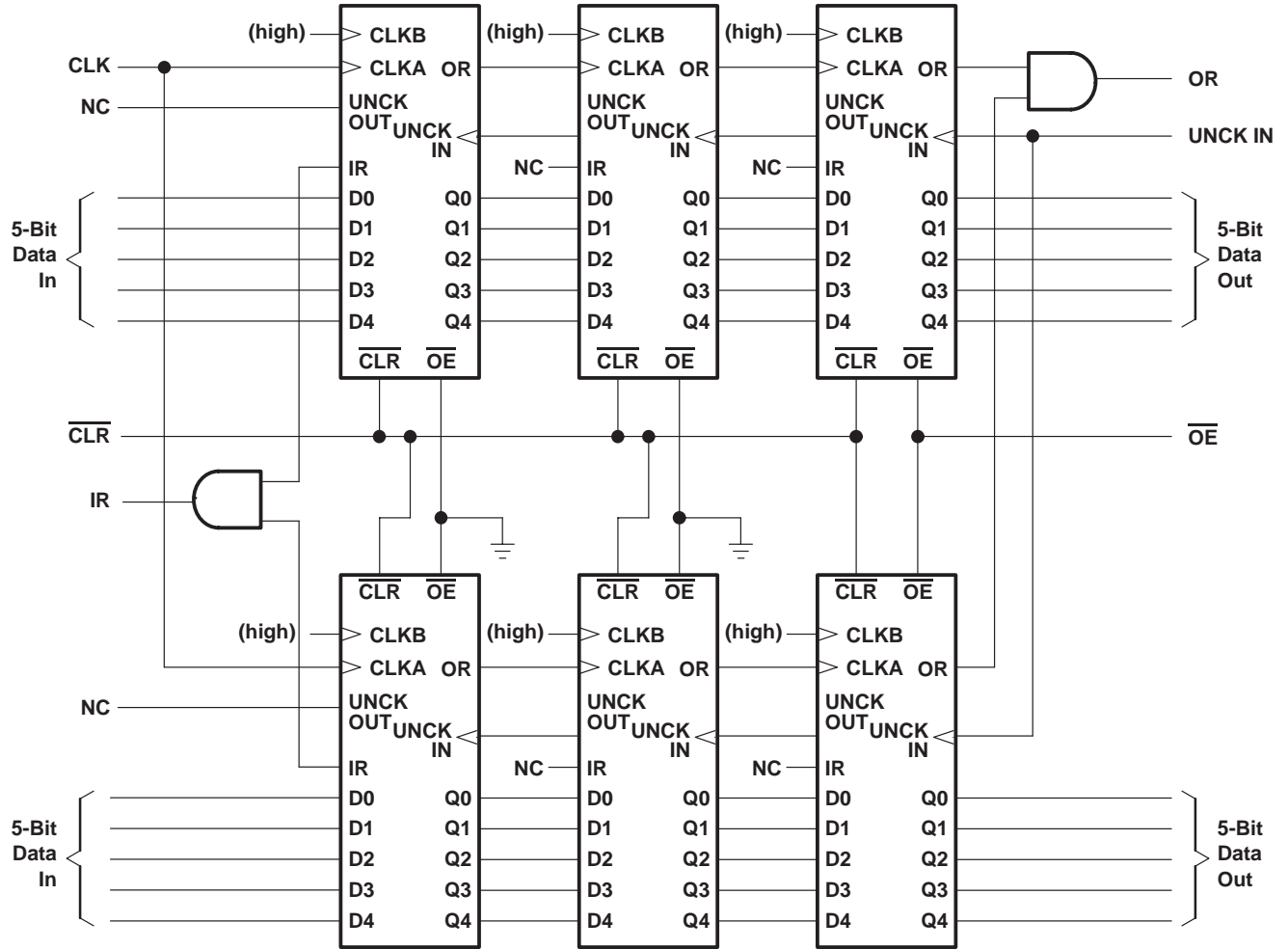


Figure 3. Word-Width Expansion: 48 × 10 Bits

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74S225J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74S225N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S225N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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