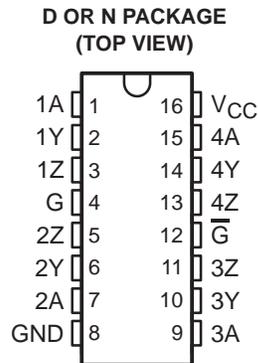


# SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS007D – JULY 1985 – REVISED APRIL 1998

- Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11
- Designed to Operate up to 20 Mbaud
- 3-State TTL Compatible
- Single 5-V Supply Operation
- High Output Impedance in Power-Off Condition
- Complementary Output-Enable Inputs
- Improved Replacement for the AM26LS31



## description

The four differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendations V.11 and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

High-impedance inputs maintain low input currents, less than 1  $\mu$ A for a high level and less than 100  $\mu$ A for a low level. Complementary output-enable inputs (G and  $\bar{G}$ ) allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 Mbit/s and is designed to operate with the SN75ALS193 quadruple line receiver.

The SN75ALS192 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE  
(each driver)**

| INPUT<br>A | ENABLES |           | OUTPUTS |   |
|------------|---------|-----------|---------|---|
|            | G       | $\bar{G}$ | Y       | Z |
| H          | H       | X         | H       | L |
| L          | H       | X         | L       | H |
| H          | X       | L         | H       | L |
| L          | X       | L         | L       | H |
| X          | L       | H         | Z       | Z |

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

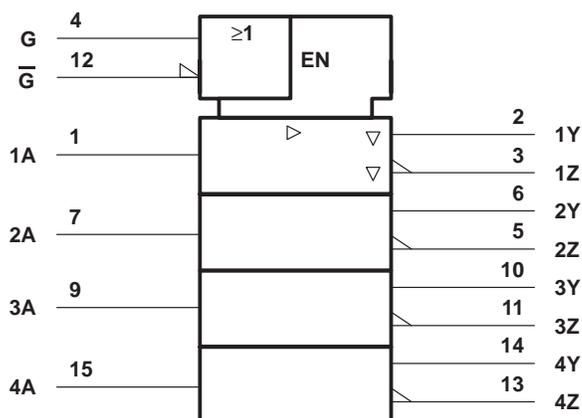
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# SN75ALS192 QUADRUPLE DIFFERENTIAL LINE DRIVER

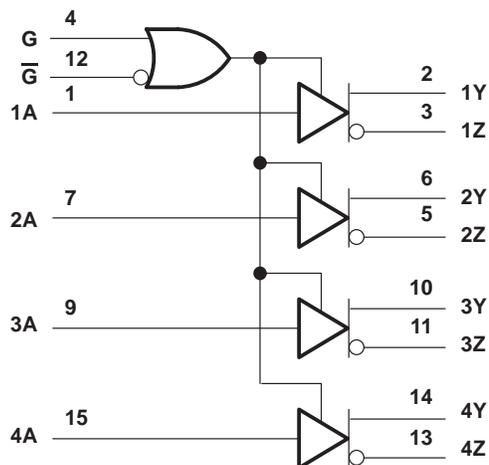
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## logic symbol†

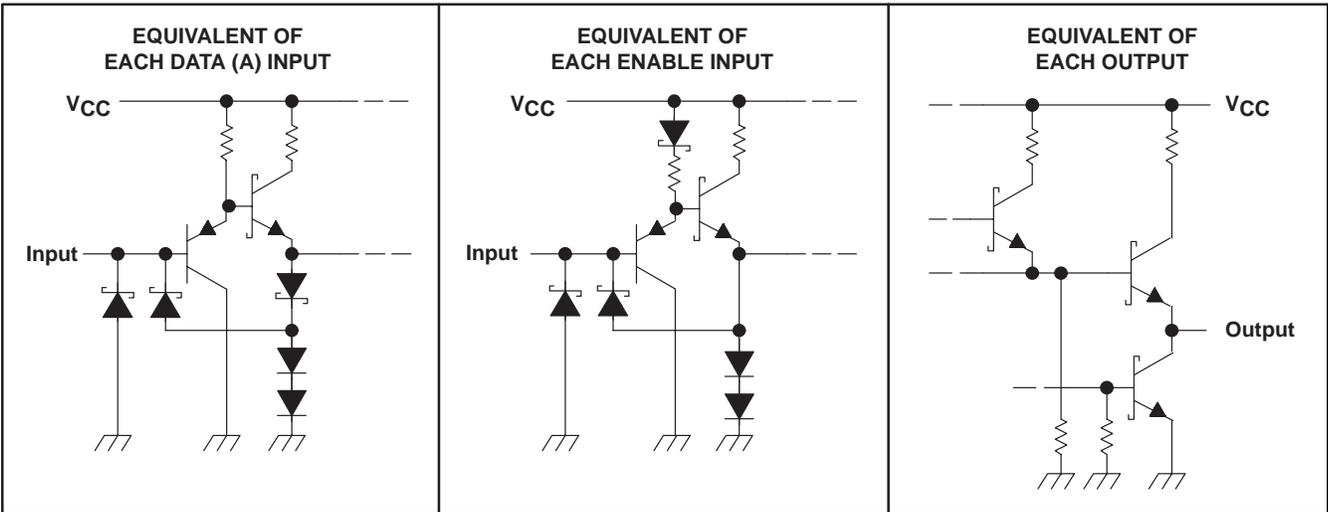


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



**schematics of inputs and outputs**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|  |                              |
|--|------------------------------|
| Supply voltage, $V_{CC}$ (see Note 1)                        | 7 V                          |
| Input voltage, $V_I$   | 7 V                          |
| Off-state output voltage                                     | 6 V                          |
| Continuous total dissipation                                 | See Dissipation Rating Table |
| Storage temperature range, $T_{stg}$                         | -65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except differential output voltage,  $V_{OD}$ , are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 125^\circ\text{C}$<br>POWER RATING |
|---------|---|---|--|---|
| D       | 950 mW                                      | 7.6 mW/°C   | 608 mW                                   | N/A                                       |
| N       | 1150 mW                                     | 9.2 mW/°C   | 736 mW                                   | N/A                                       |

**recommended operating conditions**

|                                       | MIN  | NOM | MAX  | UNIT |
|---------------------------------------|------|-----|------|------|
| Supply voltage, $V_{CC}$              | 4.75 | 5   | 5.25 | V    |
| High level input voltage, $V_{IH}$    | 2    |     |      | V    |
| Low-level input voltage, $V_{IL}$     |      |     | 0.8  | V    |
| High-level output current, $I_{OH}$   |      |     | -20  | mA   |
| Low-level output current, $I_{OL}$    |      |     | 20   | mA   |
| Operating free-air temperature, $T_A$ | 0    |     | 70   | °C   |

# SN75ALS192

## QUADRUPLE DIFFERENTIAL LINE DRIVER

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         |   | TEST CONDITIONS†        |                          | MIN                        | TYP‡ | MAX  | UNIT |
|-------------------|---|-------------------------|--------------------------|----------------------------|------|------|------|
| V <sub>IK</sub>   | Input clamp voltage                                 | V <sub>CC</sub> = MIN,  | I <sub>I</sub> = -18 mA  |                            |      | -1.5 | V    |
| V <sub>OH</sub>   | High-level output voltage                           | V <sub>CC</sub> = MIN,  | I <sub>OH</sub> = -20 mA | 2.5                        |      |      | V    |
| V <sub>OL</sub>   | Low-level output voltage                            | V <sub>CC</sub> = MIN,  | I <sub>OL</sub> = 20 mA  |                            |      | 0.5  | V    |
| V <sub>O</sub>    | Output voltage                                      | V <sub>CC</sub> = MAX,  | I <sub>O</sub> = 0       | 0                          |      | 6    | V    |
| V <sub>OD1</sub>  | Differential output voltage                         | V <sub>CC</sub> = MIN,  | I <sub>O</sub> = 0       | 1.5                        |      | 6    | V    |
| V <sub>OD2</sub>  | Differential output voltage                         | R <sub>L</sub> = 100 Ω, | See Figure 1             | 1/2 V <sub>OD1</sub> or 2§ |      |      | V    |
| Δ V <sub>OD</sub> | Change in magnitude of differential output voltage¶ | R <sub>L</sub> = 100 Ω, | See Figure 1             |                            |      | ±0.2 | V    |
| V <sub>OC</sub>   | Common-mode output voltage#                         | R <sub>L</sub> = 100 Ω, | See Figure 1             |                            |      | ±3   | V    |
| Δ V <sub>OC</sub> | Change in magnitude of common-mode output voltage¶  | R <sub>L</sub> = 100 Ω, | See Figure 1             |                            |      | ±0.2 | V    |
| I <sub>O</sub>    | Output current with power off                       | V <sub>CC</sub> = 0     | V <sub>O</sub> = 6 V     |                            |      | 100  | μA   |
|                   |   |                         | V <sub>O</sub> = -0.25 V |                            |      | -100 |      |
| I <sub>OZ</sub>   | Off-state (high-impedance state) output current     | V <sub>CC</sub> = MAX   | V <sub>O</sub> = 0.5 V   |                            |      | -20  | μA   |
|                   |   |                         | V <sub>O</sub> = 2.5 V   |                            |      | 20   |      |
| I <sub>I</sub>    | Input current at maximum input voltage              | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 7 V     |                            |      | 100  | μA   |
| I <sub>IH</sub>   | High-level input current                            | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 2.7 V   |                            |      | 20   | μA   |
| I <sub>IL</sub>   | Low-level input current                             | V <sub>CC</sub> = MAX,  | V <sub>I</sub> = 0.4 V   |                            |      | -200 | μA   |
| I <sub>OS</sub>   | Short-circuit output current                        | V <sub>CC</sub> = MAX   |                          | -30                        |      | -150 | mA   |
| I <sub>CC</sub>   | Supply current (all drivers)                        | V <sub>CC</sub> = MAX,  | All outputs disabled     |                            | 26   | 45   | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

§ The minimum V<sub>OD2</sub> with a 100-Ω load is either 1/2 V<sub>OD1</sub> or 2 V, whichever is greater.

¶ |V<sub>OD</sub>| and |V<sub>OC</sub>| are the changes in magnitude of V<sub>OD</sub> and V<sub>OC</sub>, respectively, that occur when the input is changed from a high level to a low level.

# In ANSI Standard EIA/TIA-422-B, V<sub>OC</sub>, which is the average of the two output voltages with respect to ground, is called output offset voltage, V<sub>OS</sub>.

|| Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 2)

| PARAMETER        |  | TEST CONDITIONS        |                        | MIN | TYP | MAX | UNIT |
|------------------|--|------------------------|------------------------|-----|-----|-----|------|
| t <sub>PLH</sub> | Propagation delay time, low-to-high-level output | S1 and S2 open,        | C <sub>L</sub> = 30 pF |     | 6   | 13  | ns   |
| t <sub>PHL</sub> | Propagation delay time, high-to-low-level output | S1 and S2 open,        | C <sub>L</sub> = 30 pF |     | 9   | 14  | ns   |
|                  | Output-to-output skew                            | S1 and S2 open,        | C <sub>L</sub> = 30 pF |     | 3   | 6   | ns   |
| t <sub>PZH</sub> | Output enable time to high level                 | S1 open and S2 closed  |                        |     | 11  | 15  | ns   |
| t <sub>PZL</sub> | Output enable time to low level                  | S1 closed and S2 open  |                        |     | 16  | 20  | ns   |
| t <sub>PHZ</sub> | Output disable time from high level              | S1 open and S2 closed, | C <sub>L</sub> = 10 pF |     | 8   | 15  | ns   |
| t <sub>PLZ</sub> | Output disable time from low level               | S1 and S2 closed,      | C <sub>L</sub> = 10 pF |     | 18  | 20  | ns   |



PARAMETER MEASUREMENT INFORMATION

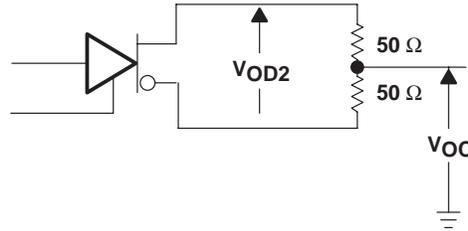
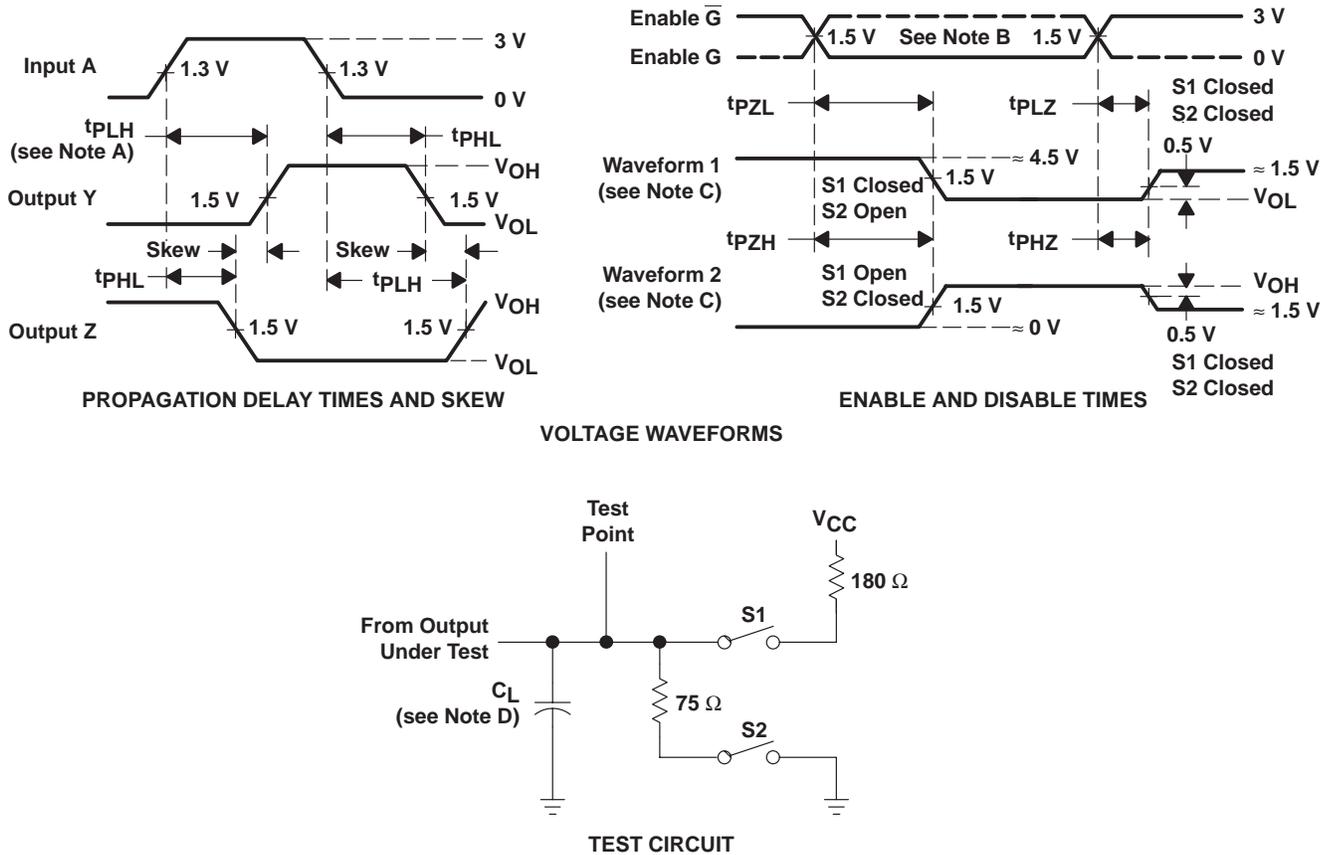


Figure 1. Differential and Common-Mode Output Voltages



- NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.  
 B. Each enable is tested separately.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D.  $C_L$  includes probe and jig capacitance.  
 E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\ \text{MHz}$ ,  $Z_O \approx 50\ \Omega$ ,  $t_r \leq 15\ \text{ns}$ , and  $t_f \leq 6\ \text{ns}$ .

Figure 2. Test Circuit and Voltage Waveforms

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## TYPICAL CHARACTERISTICS†

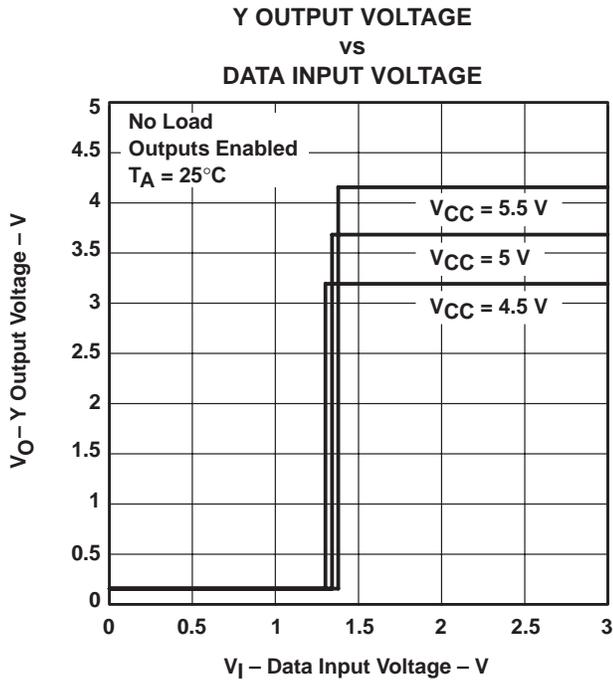


Figure 3

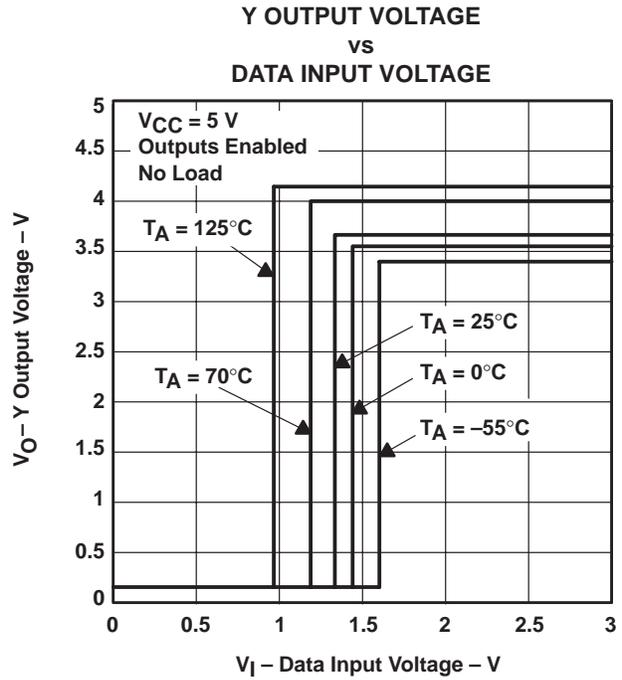


Figure 4

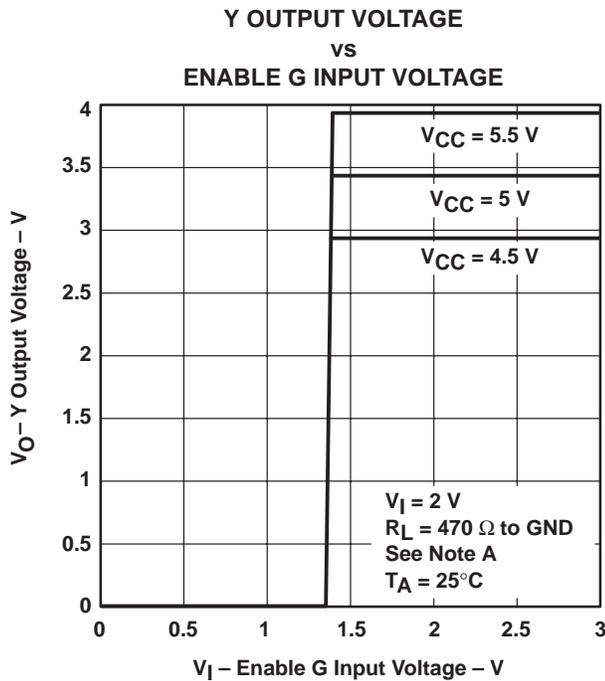


Figure 5

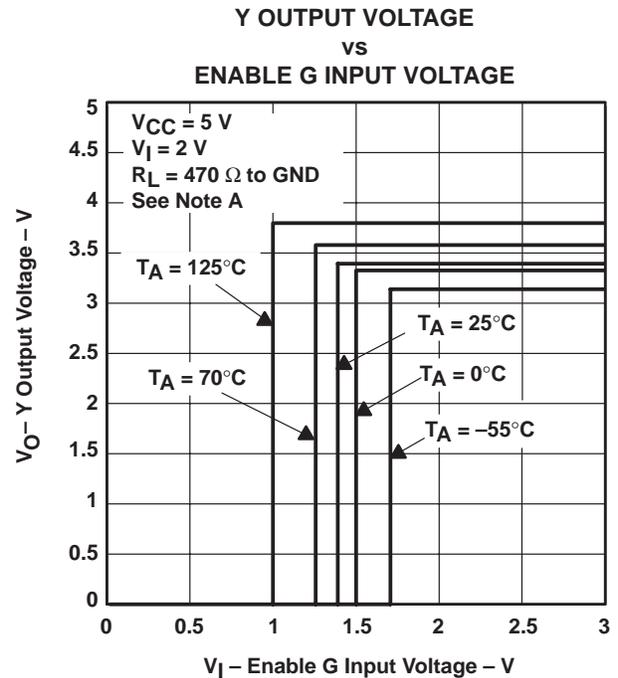


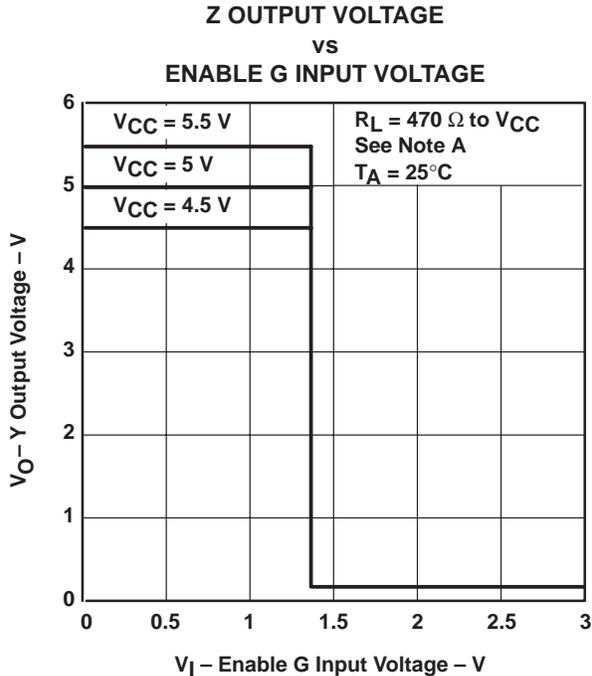
Figure 6

NOTE A: The A input is connected to  $V_{CC}$  during the testing of the Y outputs and to ground during the testing of the Z outputs.

NOTE A: The A input is connected to  $V_{CC}$  during the testing of the Y outputs and to ground during the testing of the Z outputs.

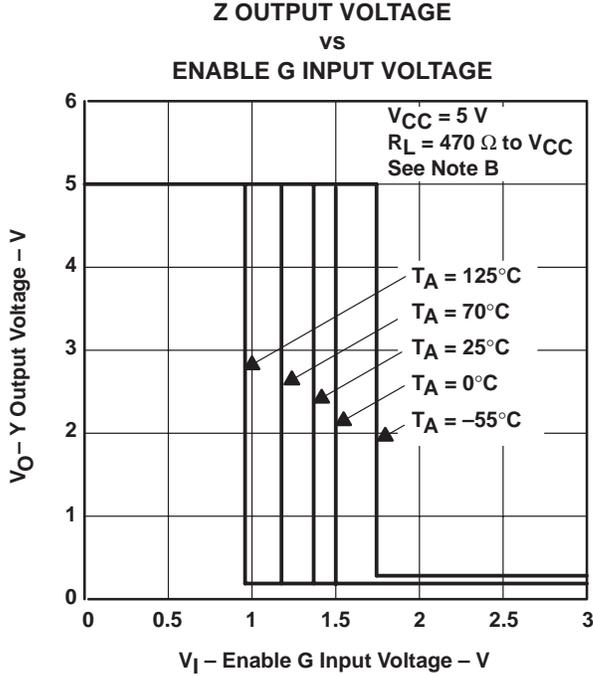
† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†



NOTE A: The A input is connected to  $V_{CC}$  during the testing of the Y outputs and to ground during the testing of the Z outputs.

Figure 7



NOTE B: The A input is connected to GND during the testing of the Y outputs and to  $V_{CC}$  during the testing of the Z outputs.

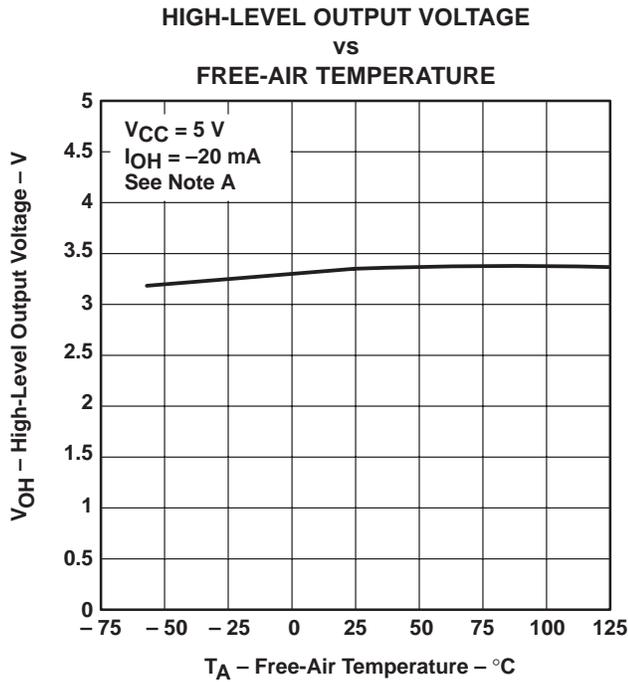
Figure 8

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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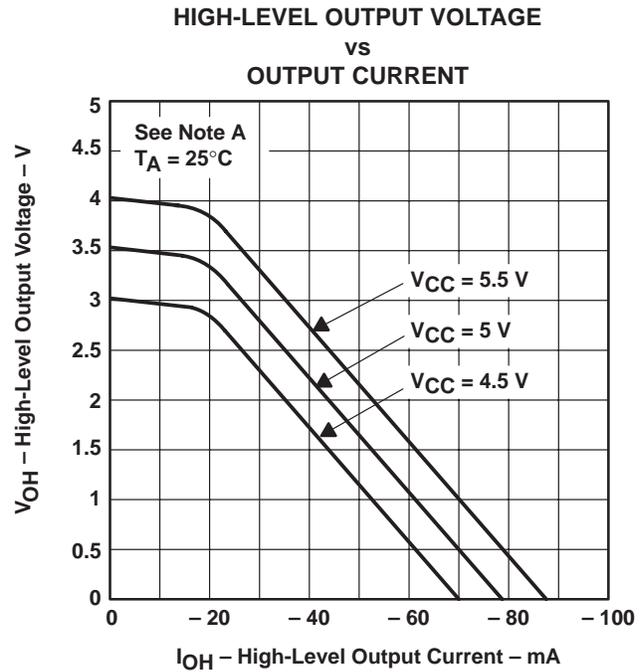
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## TYPICAL CHARACTERISTICS†



NOTE A: The A input is connected to  $V_{CC}$  during the testing of the Y outputs and to ground during the testing of the Z outputs.

**Figure 9**

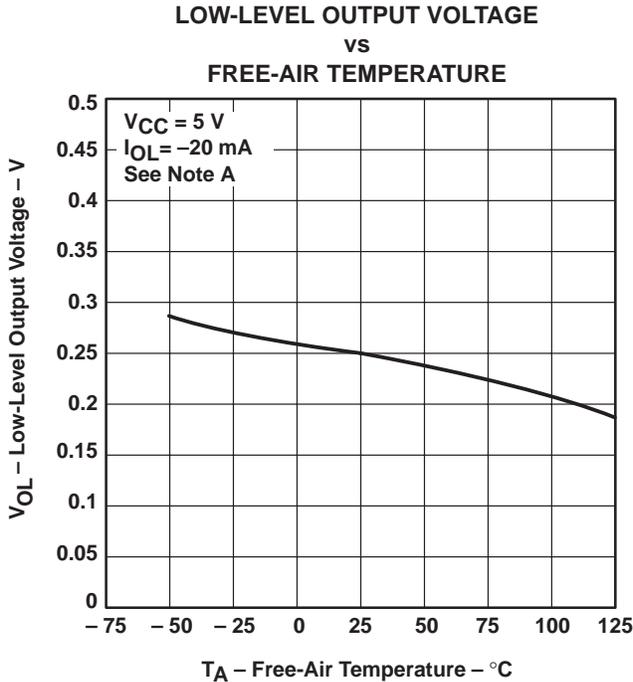


NOTE A: The A input is connected to  $V_{CC}$  during the testing of the Y outputs and to ground during the testing of the Z outputs.

**Figure 10**

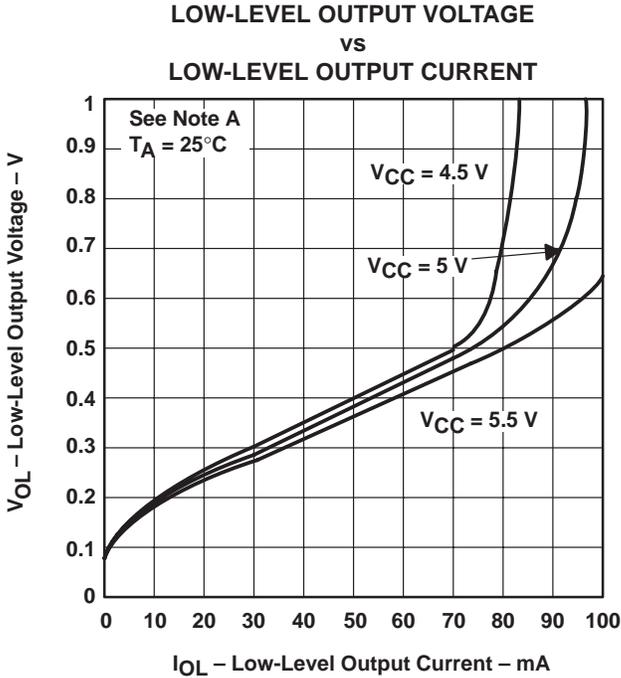
† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS†



NOTE A: The A input is connected to GND during the testing of the Y outputs and to  $V_{CC}$  during the testing of the Z outputs.

Figure 11



NOTE A: The A input is connected to GND during the testing of the Y outputs and to  $V_{CC}$  during the testing of the Z outputs.

Figure 12

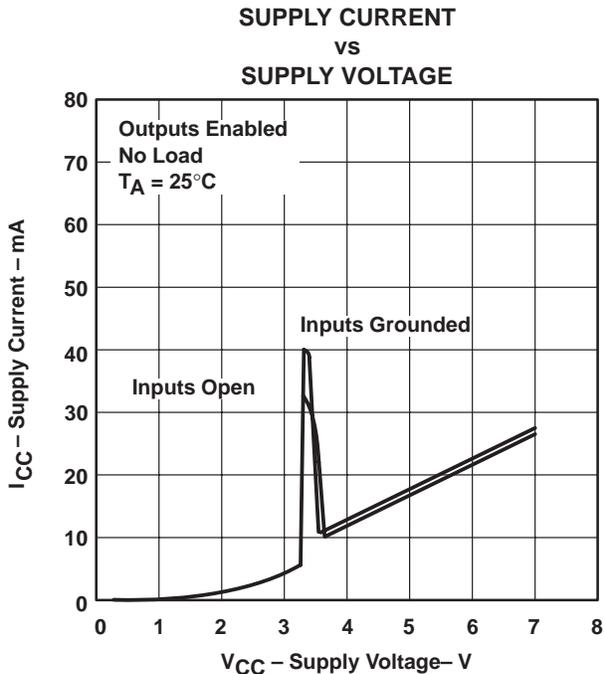


Figure 13

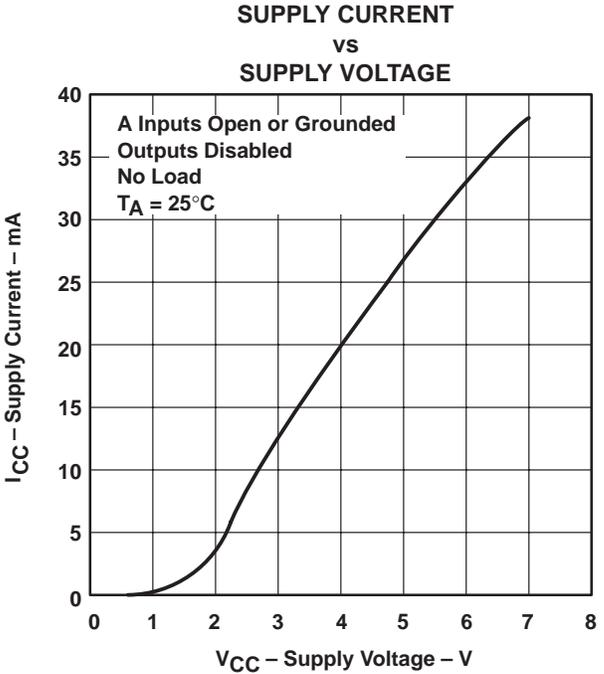


Figure 14

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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## TYPICAL CHARACTERISTICS

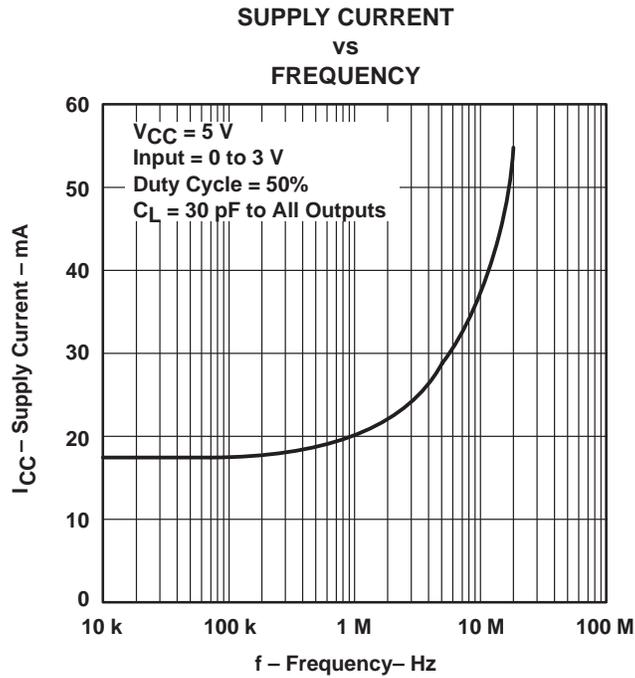


Figure 15

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|                    |  |
|--------------------|--|
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| Automotive         | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| Broadband          | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Digital Control    | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Military           | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
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| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
| Telephony          | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
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**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75ALS192D      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192DE4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192DG4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192DR     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192DRE4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192DRG4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192N      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75ALS192NE4    | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN75ALS192NSR    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192NSRE4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN75ALS192NSRG4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

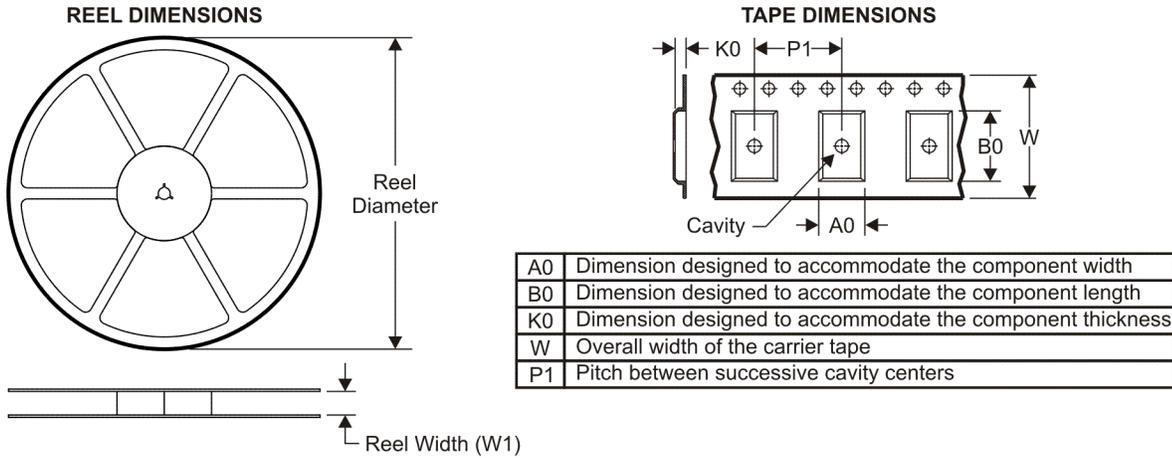
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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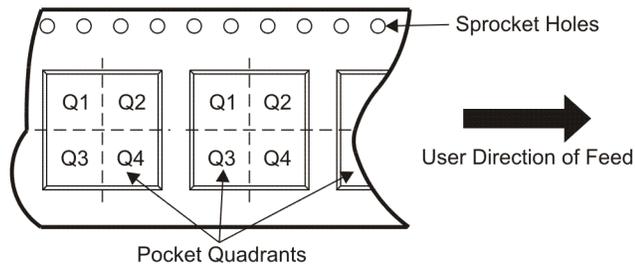
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI

to Customer on an annual basis.

**TAPE AND REEL INFORMATION**



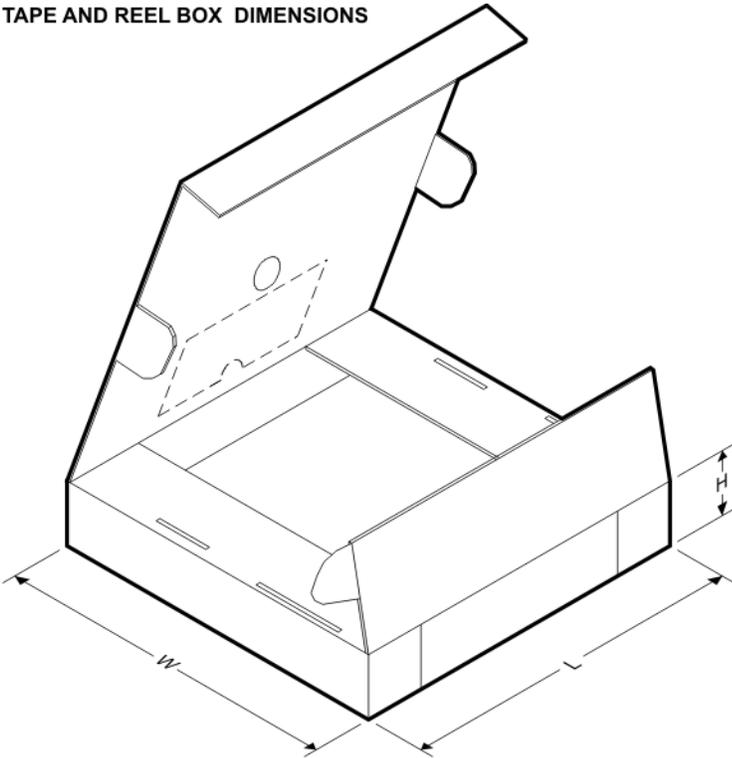
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75ALS192DR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN75ALS192NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

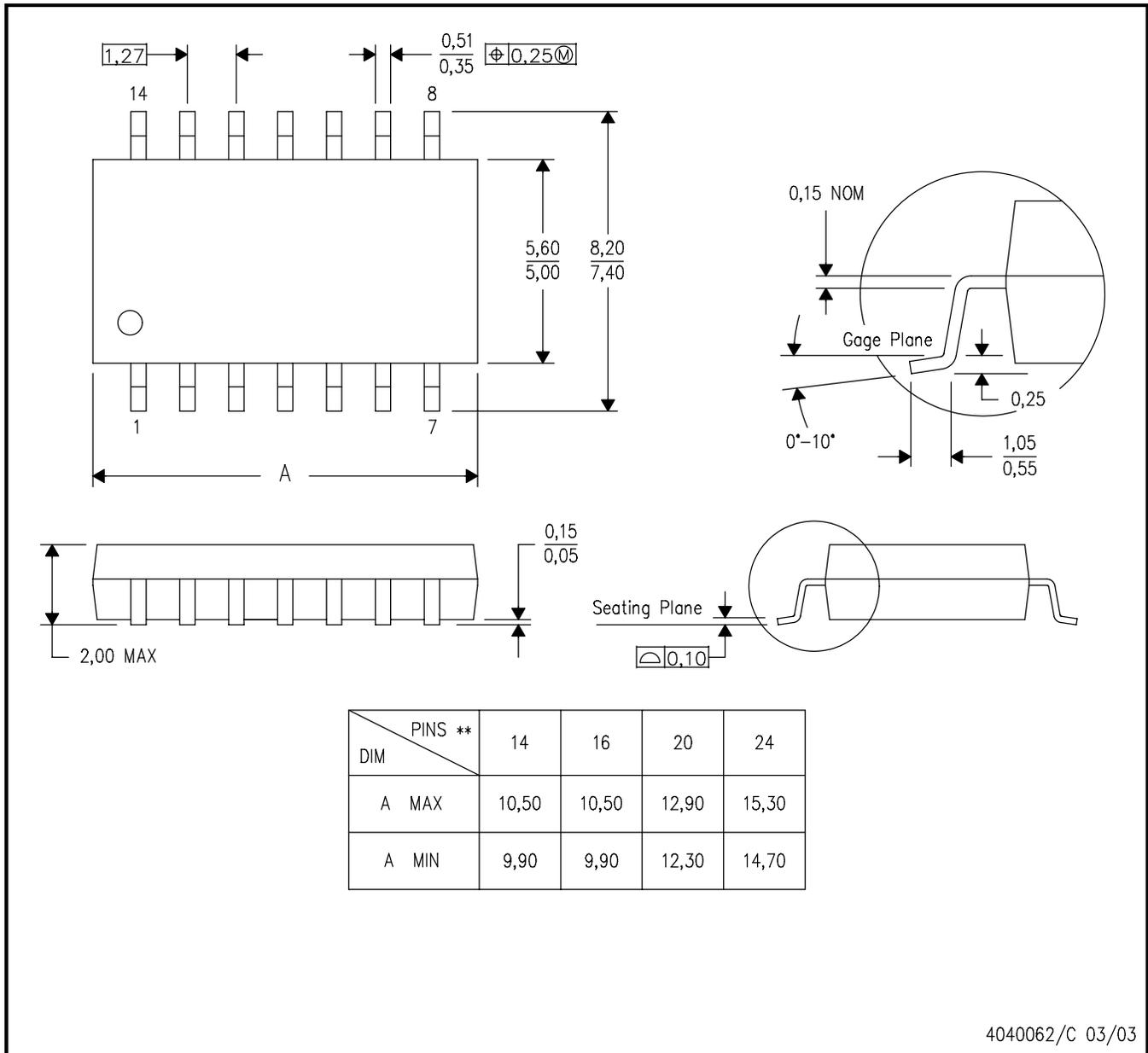
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75ALS192DR  | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| SN75ALS192NSR | SO           | NS              | 16   | 2000 | 346.0       | 346.0      | 33.0        |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

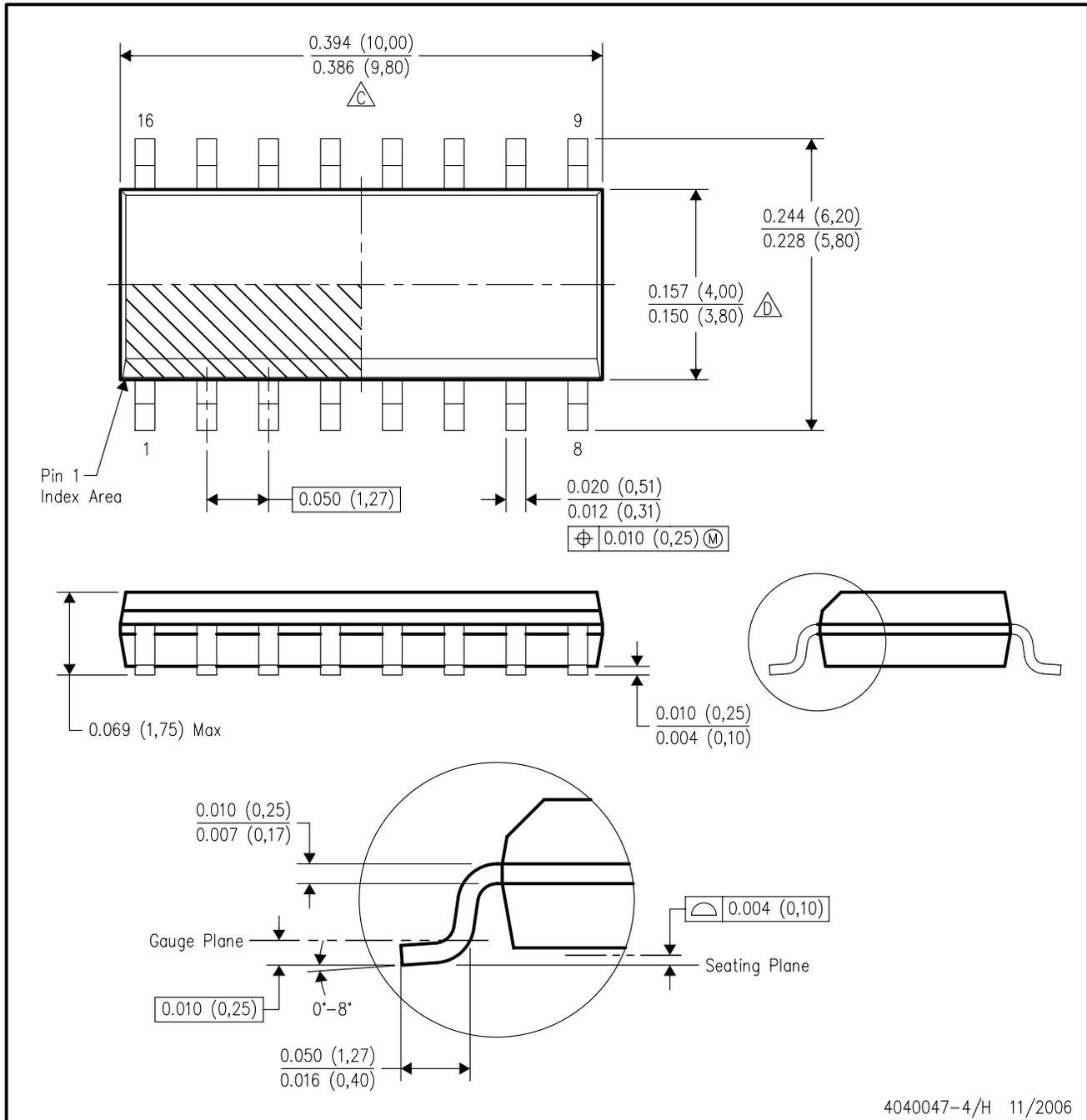
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

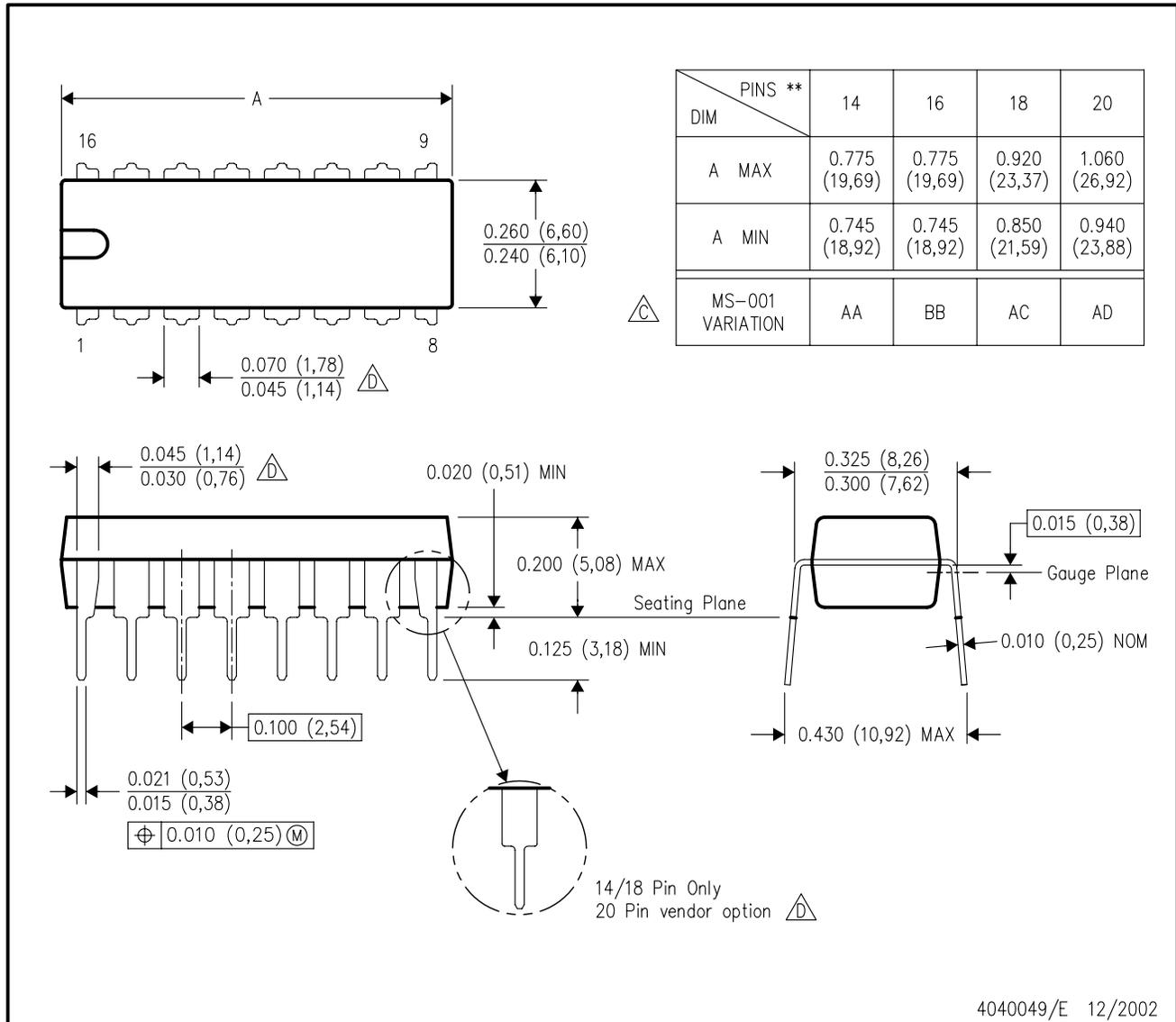


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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