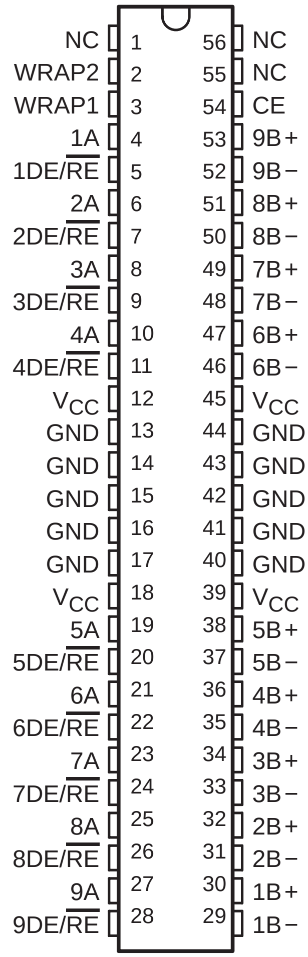
SN75LBC978
9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS134F − APRIL 1992 − REVISED APRIL 2005

- **Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI)**
- **Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typ**
- **Thermal Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output-Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

DL PACKAGE
(TOP VIEW)



Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC978 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential balanced transceivers†. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for the Small Computer Systems Interface (SCSI) standard. The WRAP function allows in-circuit testing and wired-OR channels for the BSY, RST, and SEL signals of the SCSI bus.

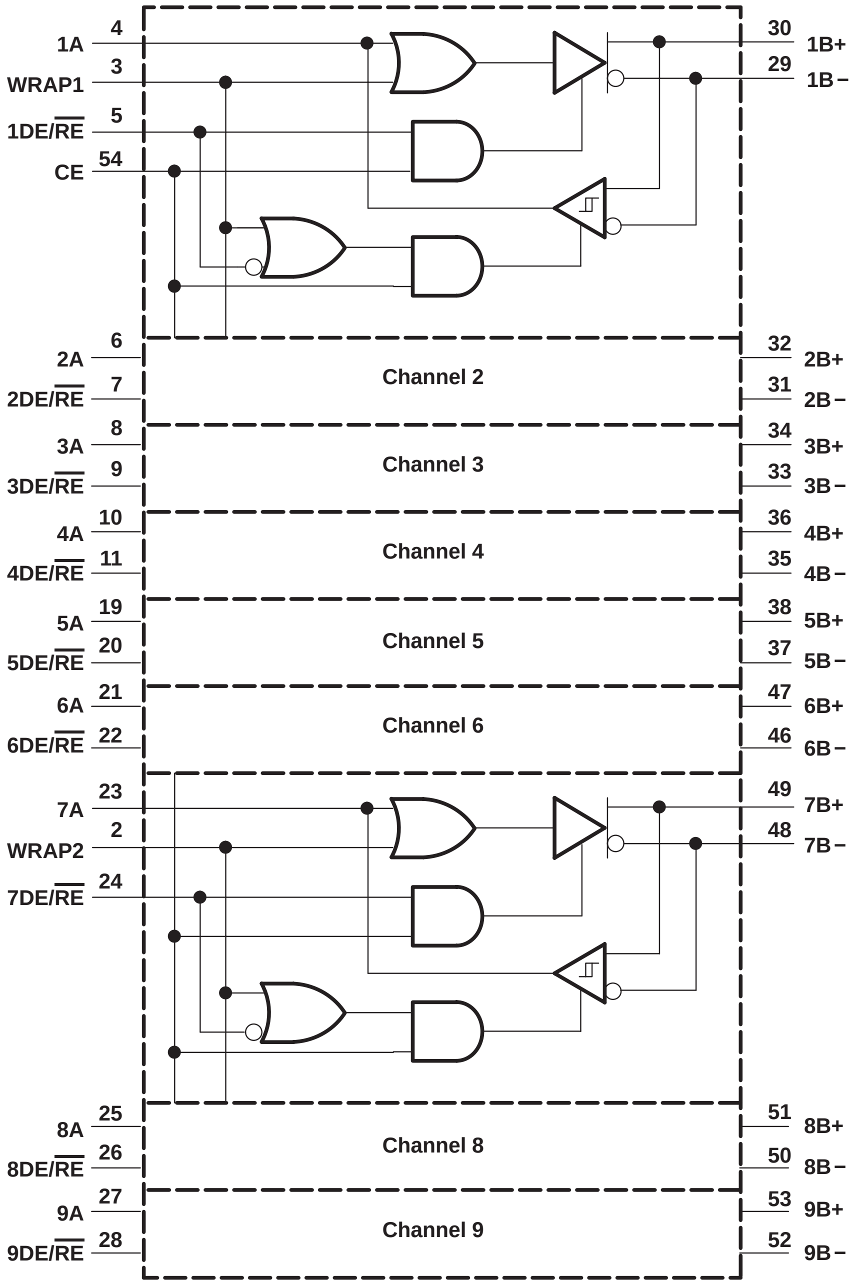
The SN75LBC978 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat-sink terminals. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed of the SN75LBC978 is sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine identical channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.131-1993 (SCSI-2) and the proposed SCSI-3 standards.

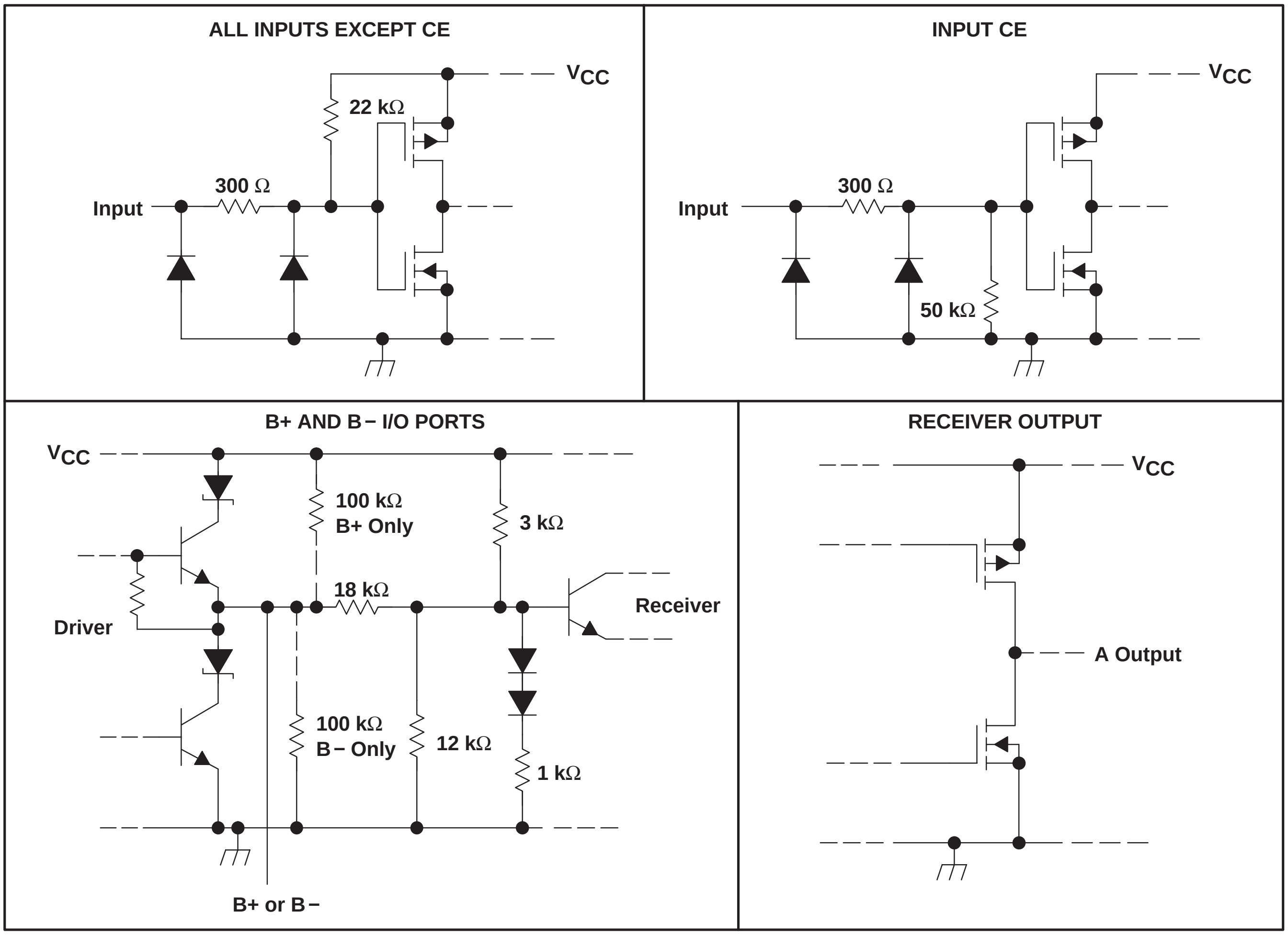
The SN75LBC978 is characterized for operation from 0°C to 70°C.

† Patent Pending
LinASIC and LinBiCMOS are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.3 V to 7 V
Bus voltage range . . . . −10 V to 15 V
Data I/O and control (A-side) voltage range . . . . −0.3 V to 7 V
Receiver output current, I_O . . . . ±24 mA
Continuous power dissipation . . . . internally limited

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are dc and with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	B+ or B−			12	V
				−7	
High-level input voltage, V_{IH}	All except B+ and B−	2			V
Low-level input voltage, V_{IL}	All except B+ and B−			0.8	V
High-level output current, I_{OH}	B+ or B−			−60	mA
	A			−8	mA
Low-level output current, I_{OL}	B+ or B−			60	mA
	A			8	mA
Operating free-air temperature, T_A		0		70	°C

device electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	A, WRAP, DE/$\overline{RE}$	See Figure 1	V_{IH} = 2 V			−200	µA
		CE					100	µA
I_{IL}	Low-level input current	A, WRAP, DE/$\overline{RE}$		V_{IL} = 0.8 V			−200	µA
		CE					100	µA
I_{CC}	Supply current	All drivers and receivers disabled	CE at 0 V			1.4	3	mA
		All receivers enabled	No load, CE at 5 V,	V_{ID} = 5 V, WRAP and DE/$\overline{RE}$ at 0 V		29	45	mA
		All drivers enabled	No load, WRAP at 0 V	CE and DE/$\overline{RE}$ at 5 V,		7	10	mA
C_O	Bus port output capacitance		B+ or B−			19		pF
C_{pd}	Power dissipation capacitance		One driver			460		pF
			One receiver			40		pF

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage	V_{test} = −7 V to 12 V, See Figure 2	1	2		V
I_{OS}	Output short-circuit current	See Figure 3			±250	mA
I_{OZ}	High-impedance-state output current	See receiver input current				

receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = −8 mA	2.5			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV, I_{OL} = 8 mA			0.8	V
V_{IT+}	Differential-input high-level threshold voltage		I_{OH} = −8 mA			0.2	V
V_{IT-}	Differential-input low-level threshold voltage		I_{OL} = 8 mA	−0.2			V
V_{hys}	Receiver input hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
I_I	Receiver input current	B+ and B−	V_I = 12 V, V_{CC} = 5 V, Other input at 0 V		0.7	1	mA
			V_I = 12 V, V_{CC} = 0 V, Other input at 0 V		0.8	1	mA
			V_I = −7 V, V_{CC} = 5 V, Other input at 0 V		−0.5	−0.8	mA
			V_I = −7 V, V_{CC} = 0 V, Other input at 0 V		−0.4	−0.8	mA
I_{OZ}	High-impedance-state output current		V_O = GND			−200	µA
			$V_O = V_{CC}$			50	

driver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential delay time, high- to low-level output ($t_{d(ODH)}$) or low-to high-level output ($t_{d(ODL)}$)	See Figure 4	11.8		26.4	ns
		V_{CC} = 5 V, T_A = 25°C, See Figure 4	14	18	22	
		V_{CC} = 5 V, T_A = 70°C, See Figure 4	18	22	26	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices				15	ns
		V_{CC} = 5 V, See Note 2			8	
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODL)} - t_{d(ODH)} \rvert$)	See Figure 4		0	6	ns
t_t	Transition time (t_r or t_f)			10		ns

receiver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, high- to low-level output (t_{PHL}) or low- to high-level output (t_{PLH})	See Figure 5	19.5		30.7	ns
		V_{CC} = 5 V, T_A = 25°C, See Figure 5	20.2	24.7	29.2	
		V_{CC} = 5 V, T_A = 70°C, See Figure 5	21.1	25.6	30.1	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices				12	ns
		V_{CC} = 5 V, See Note 2			9	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	See Figure 5		2	6	ns
t_t	Transition time (t_r or t_f)			3		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_{pd} determines the no-load dynamic current consumption; $I_S = C_{pd} \cdot V_{CC} \cdot f + I_{CC}$.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

transceiver switching characteristics over recommended ranges of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{en(TXL)}$	Enable time, transmit-to-receive to low-level output	See Figure 6		80	ns
$t_{en(TXH)}$	Enable time, transmit-to-receive to high-level output			80	ns
$t_{en(RXL)}$	Enable time, receive-to-transmit to low-level output			150	ns
$t_{en(RXH)}$	Enable time, receive-to-transmit to high-level output			150	ns
t_{su}	Setup time, WRAP1 or WRAP2 before active input(s) or output(s)		150		ns

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

PARAMETER MEASUREMENT INFORMATION

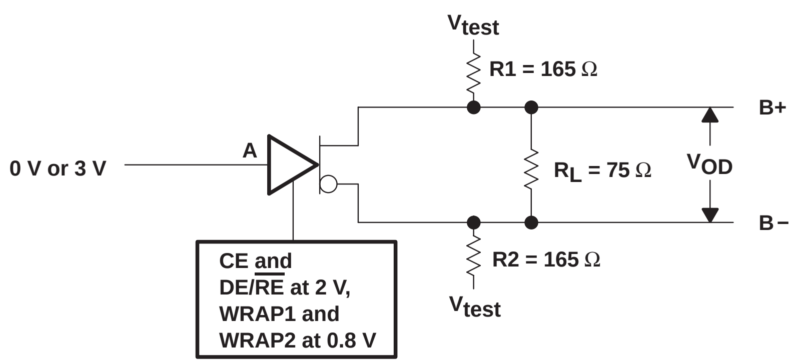
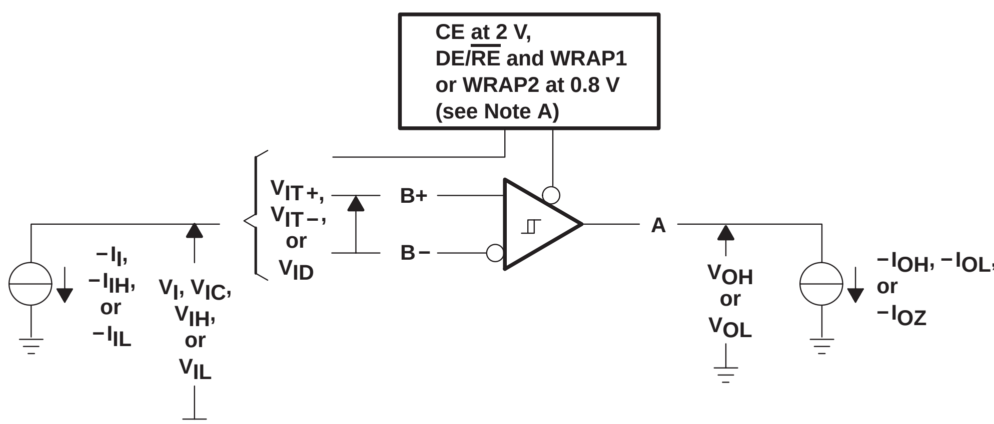


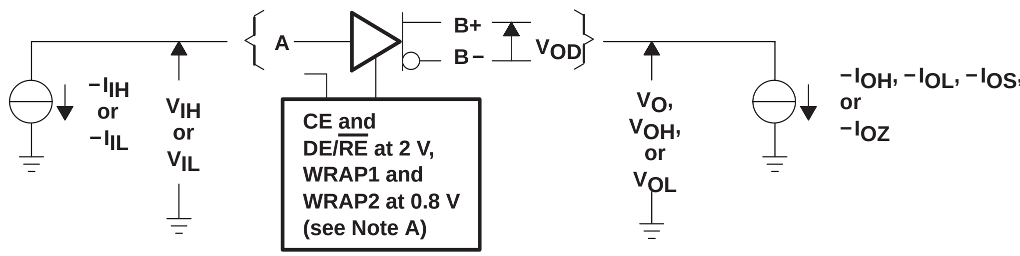
Figure 1. Driver V_{OD} Test Circuit



NOTE A: For the I_{OZ} measurement, CE is at 0.8 V.

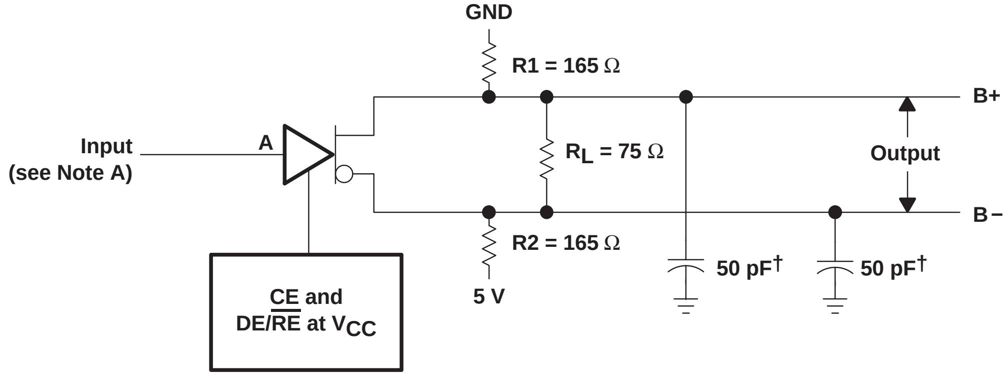
Figure 2. Receiver Test Circuit and Input Conditions

PARAMETER MEASUREMENT INFORMATION

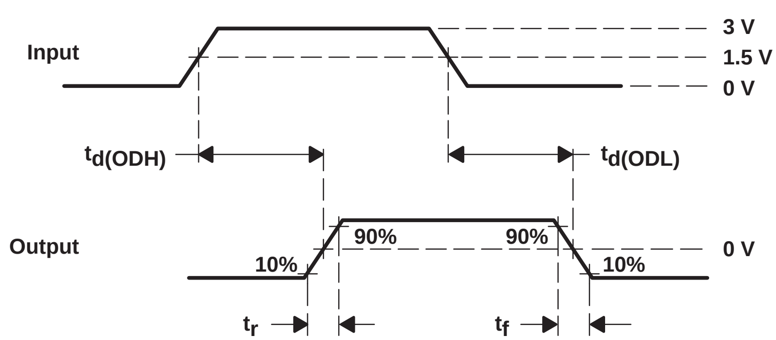


NOTE A: For the I_{OZ} test, the CE input is at 0.8 V.

Figure 3. Driver Test and Input Conditions



TEST CIRCUIT



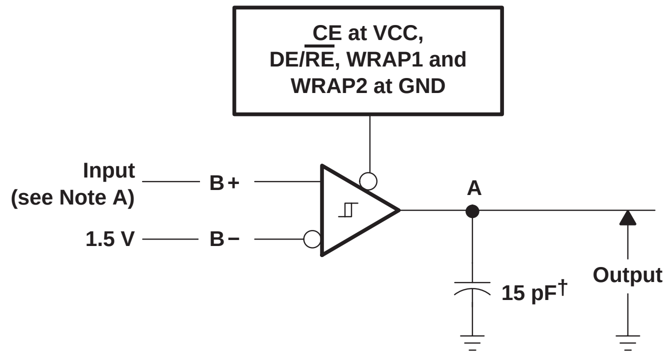
VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

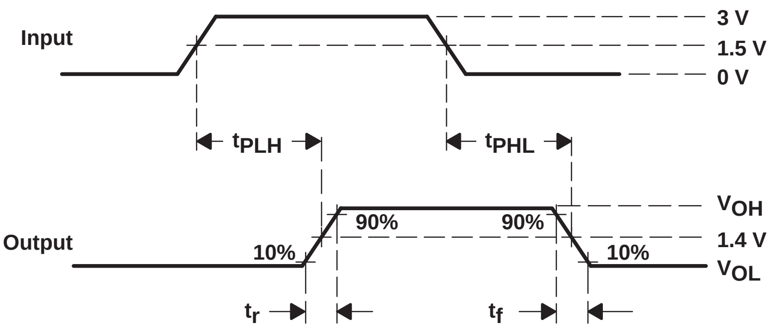
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 4. Driver Propagation Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



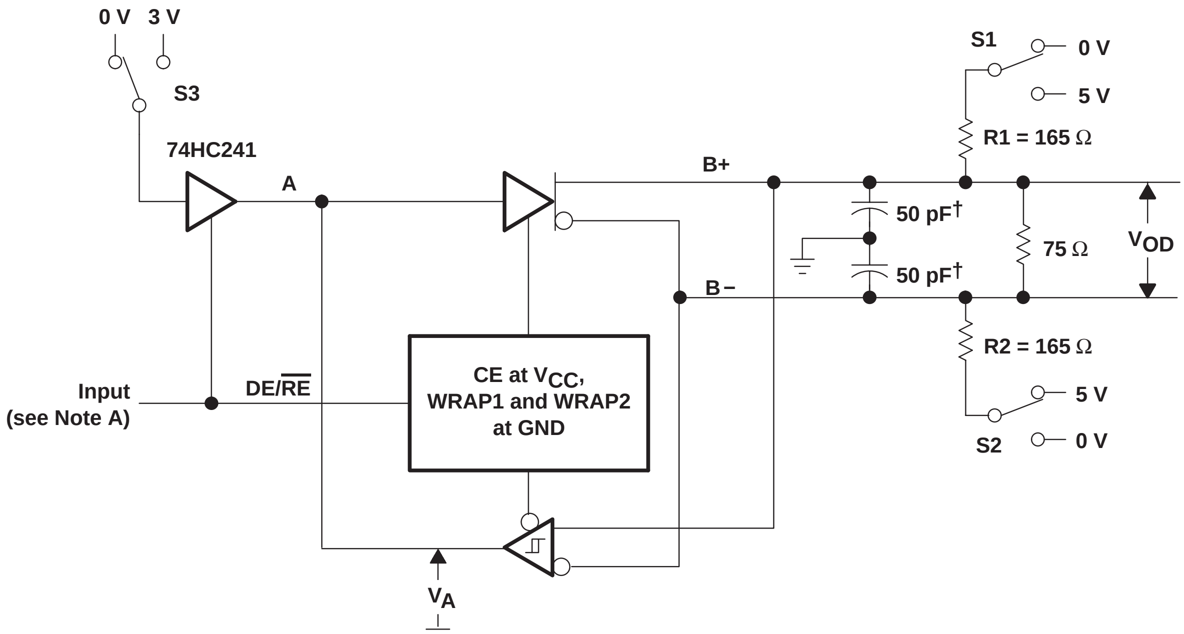
VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

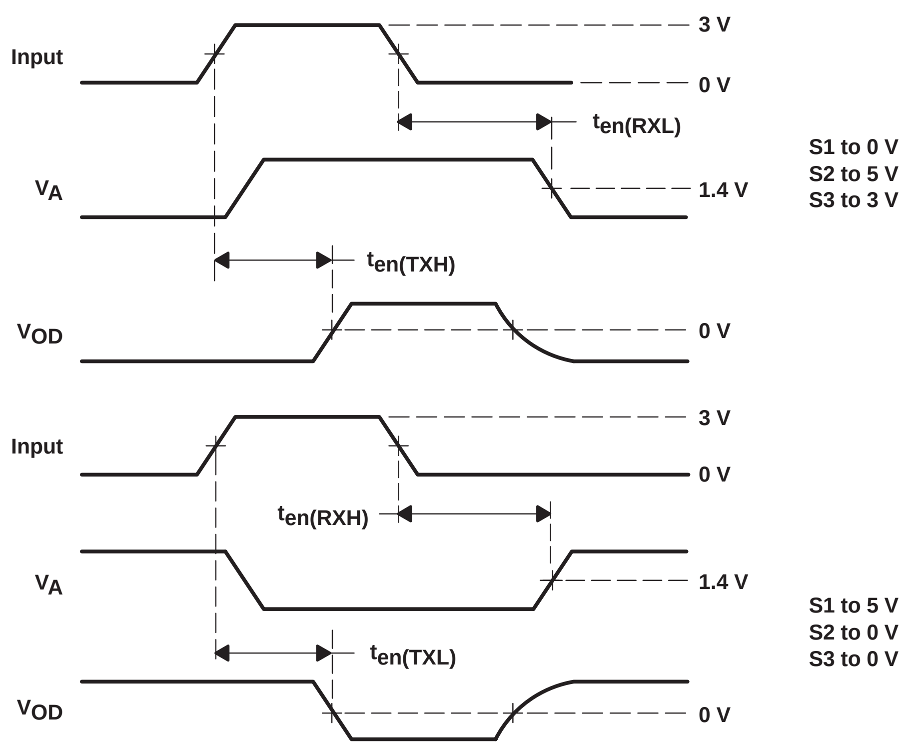
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 5. Receiver Propagation Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 6. Enable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

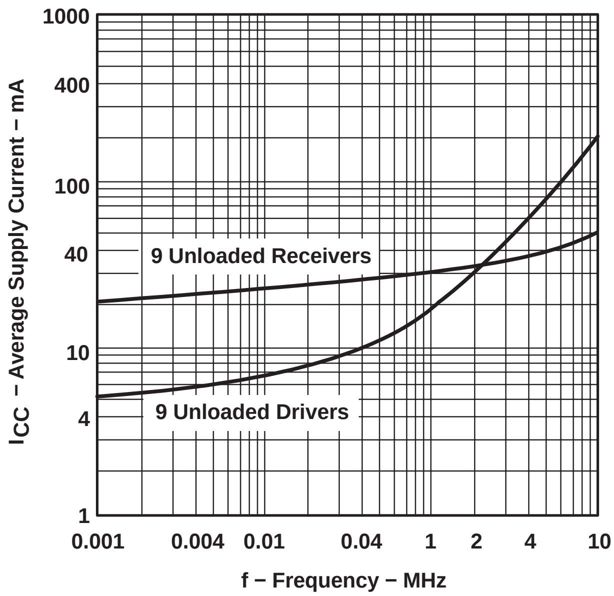


Figure 7

INPUT CURRENT
vs
INPUT VOLTAGE

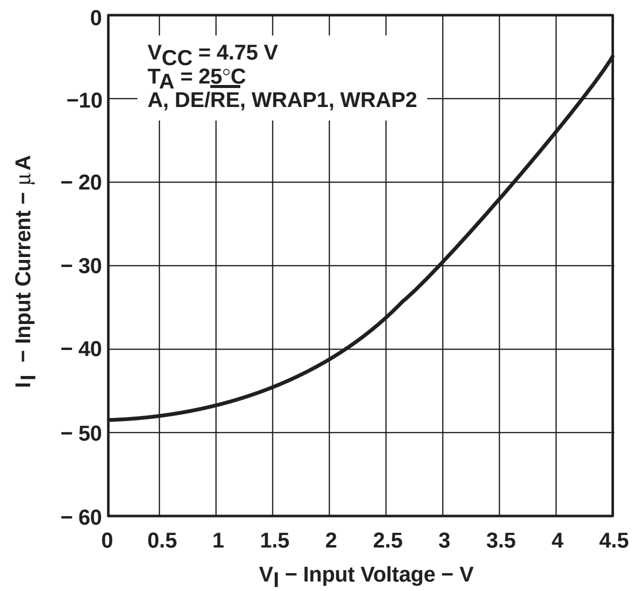


Figure 8

INPUT CURRENT
vs
INPUT VOLTAGE

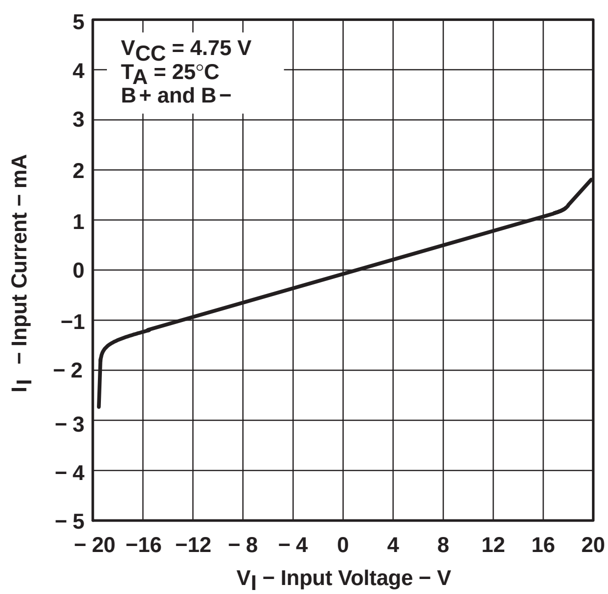


Figure 9

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

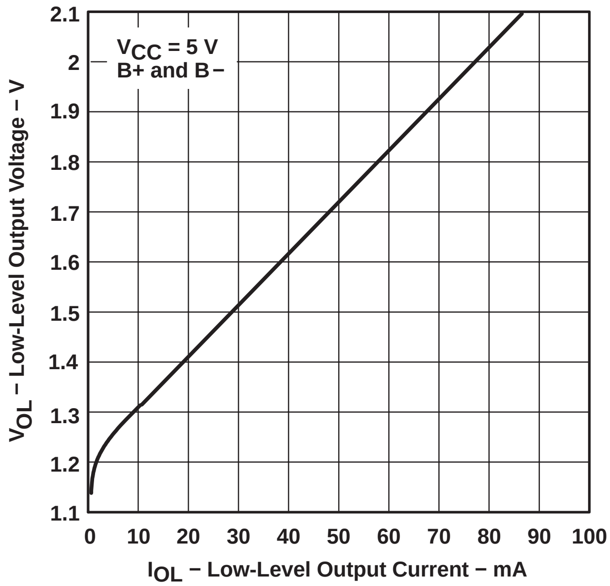


Figure 10

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

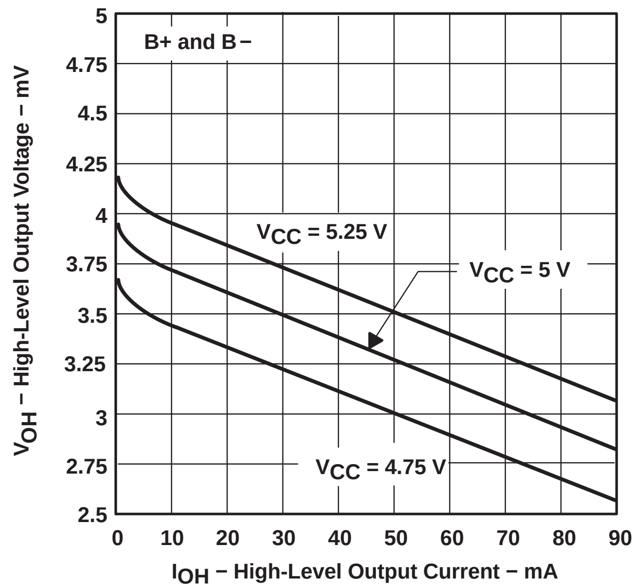


Figure 11

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

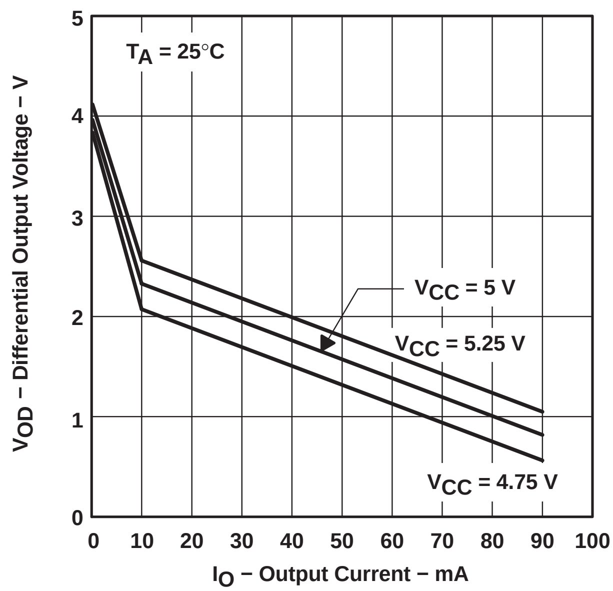


Figure 12

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

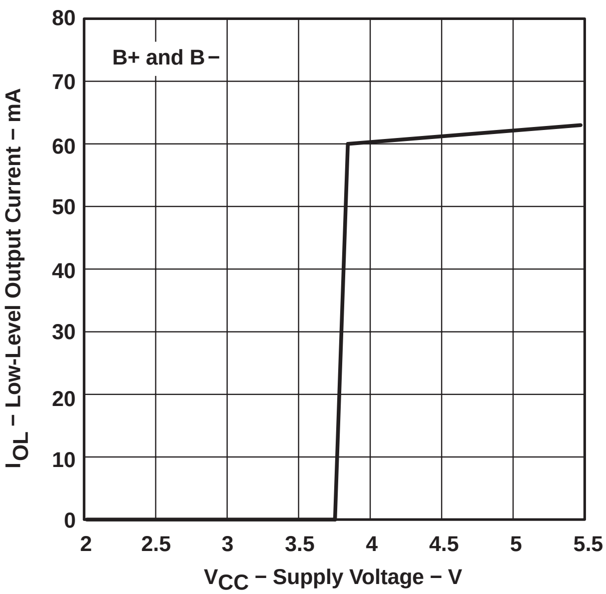


Figure 13

DRIVER
HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

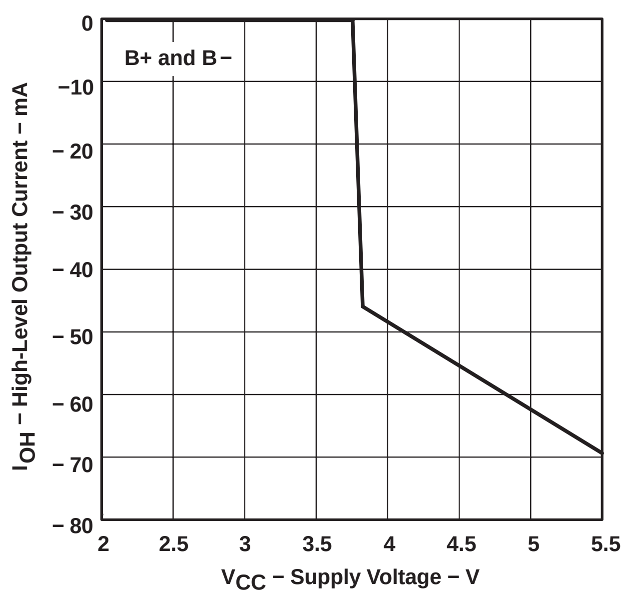


Figure 14

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

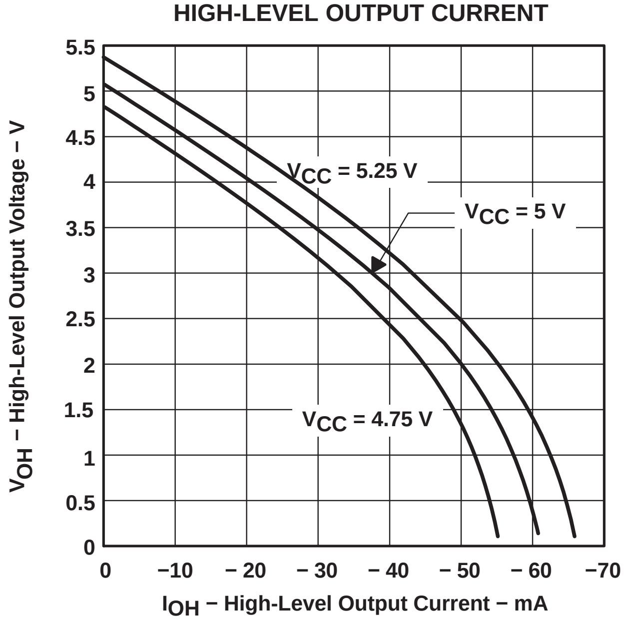


Figure 15

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

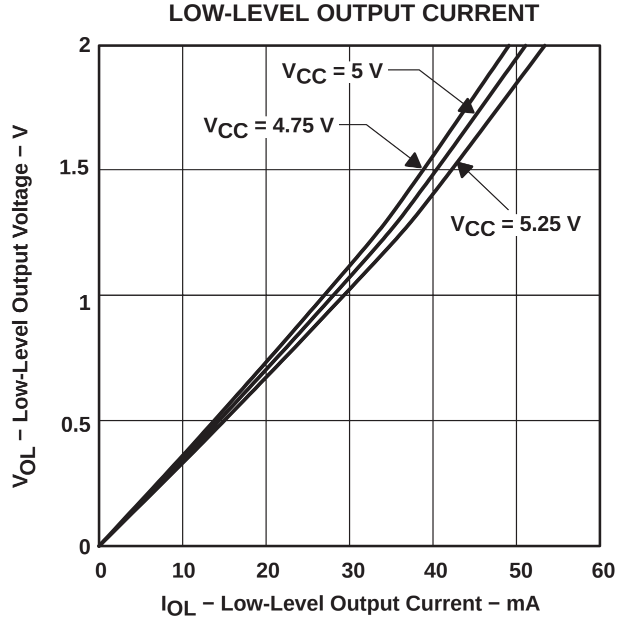


Figure 16

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

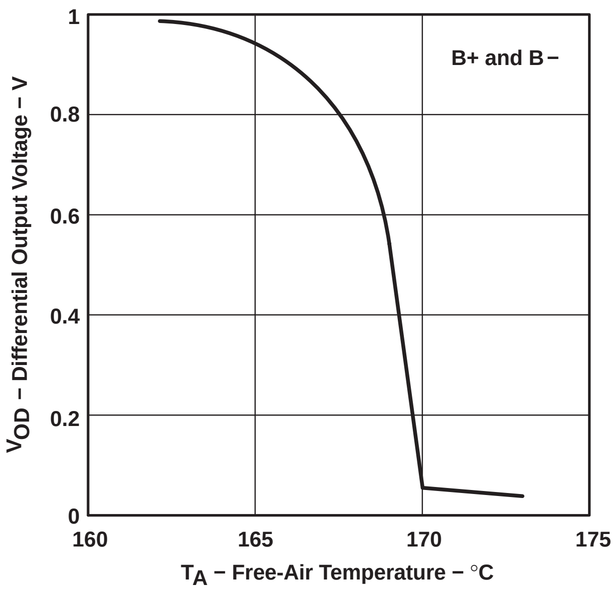


Figure 17

RECEIVER
PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

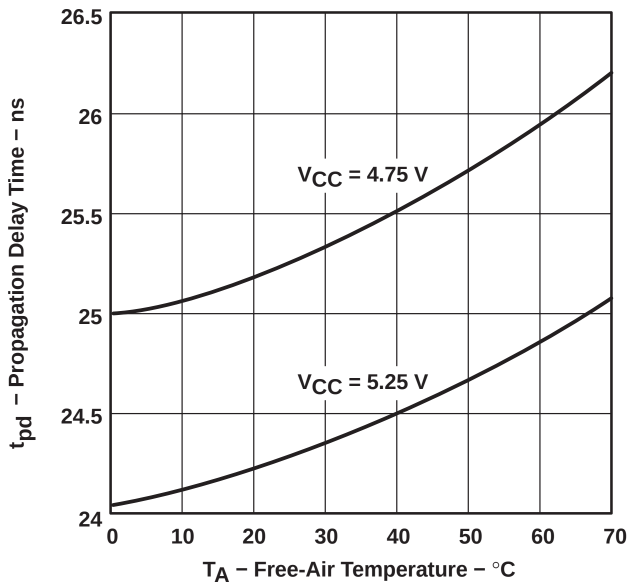


Figure 18

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

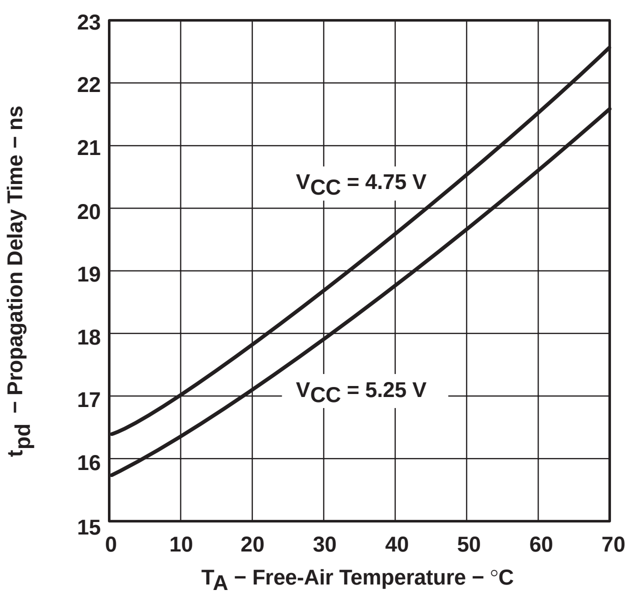


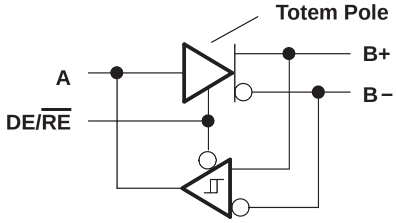
Figure 19

APPLICATION INFORMATION

function tables

Table 1. Channel Configuration for Totem Pole Circuit

**CE is high,
WRAP1 or WRAP2 is low**



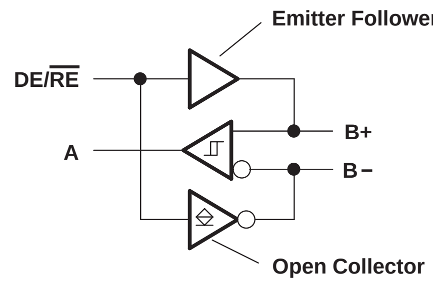
INPUTS				OUTPUTS		
DE/RE	A	B+†	B−†	A	B+	B−
L	X	L	H	L	Z	Z
L	X	H	L	H	Z	Z
H	L	X	X	Z	L	H
H	H	X	X	Z	H	L

H = high level L = low level X = irrelevant Z = high impedance

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

Table 2. Channel Configuration for Emitter Follower Circuit

**CE is high,
WRAP1 or WRAP2 is high**



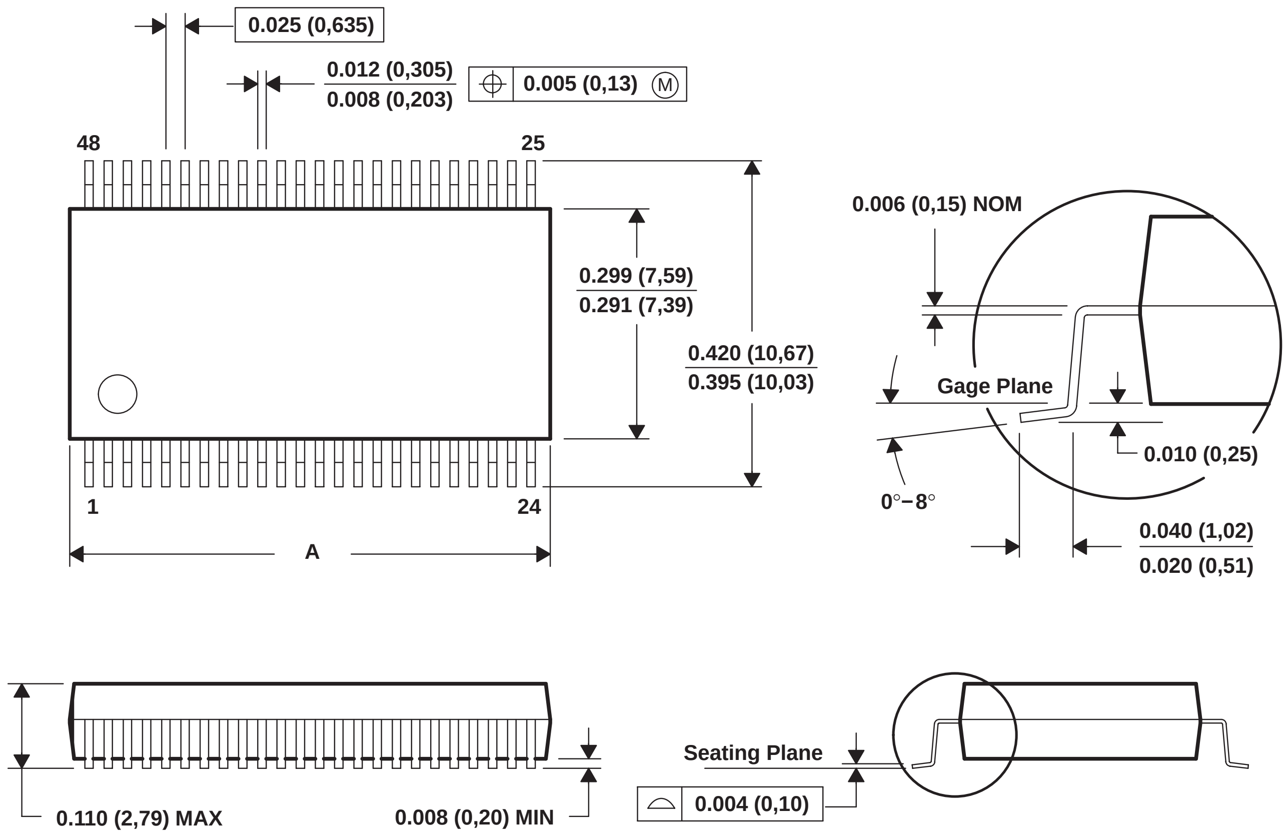
INPUTS			OUTPUTS		
DE/RE	B+	B−	A	B+	B−
L	L	H	L	Z	Z
L	H	L	H	Z	Z
H	X	X	H	H	L
H	X	X	H	H	L

H = high level L = low level X = irrelevant Z = high impedance

MECHANICAL INFORMATION

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / C 03/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75LBC978DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC978DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC978DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN75LBC978DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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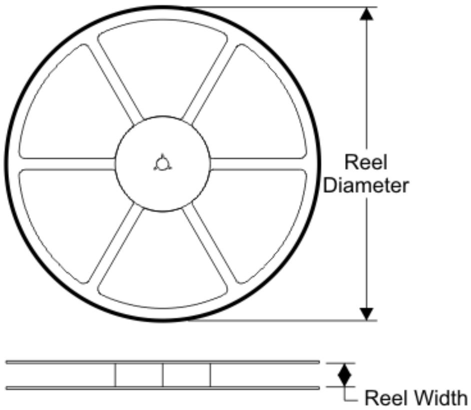
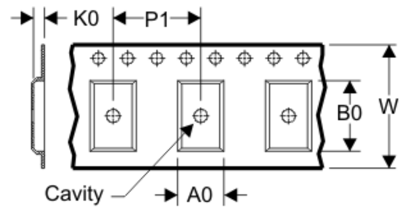
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

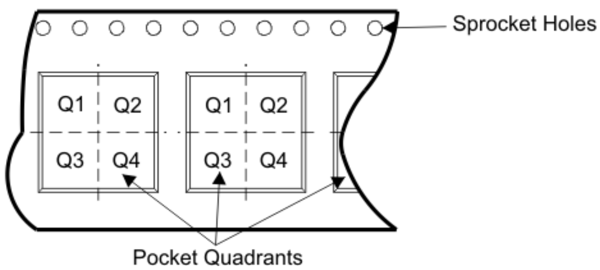


TAPE DIMENSIONS



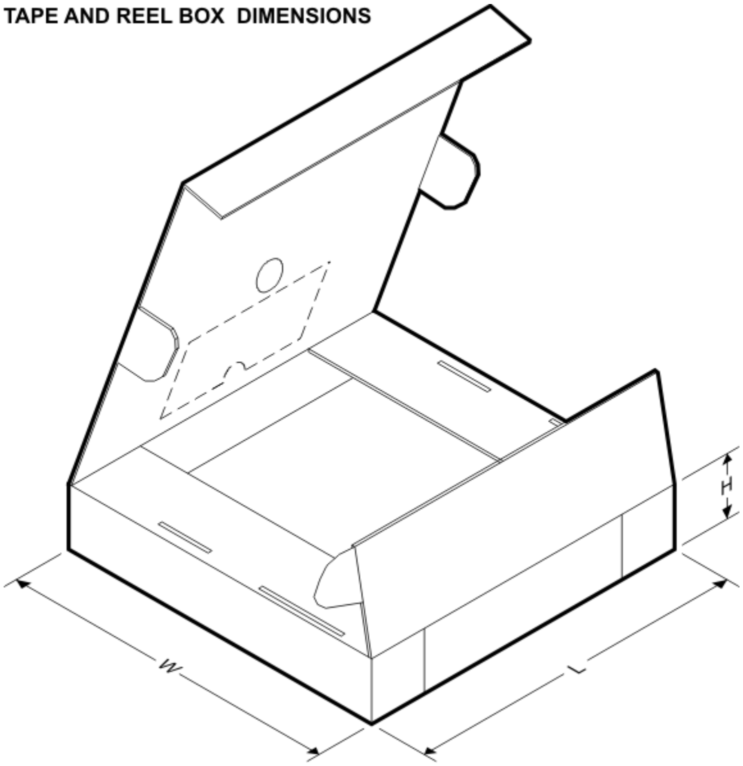
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC978DLR	DL	56	SITE 41	330	32	11.35	18.67	3.1	16	32	Q1

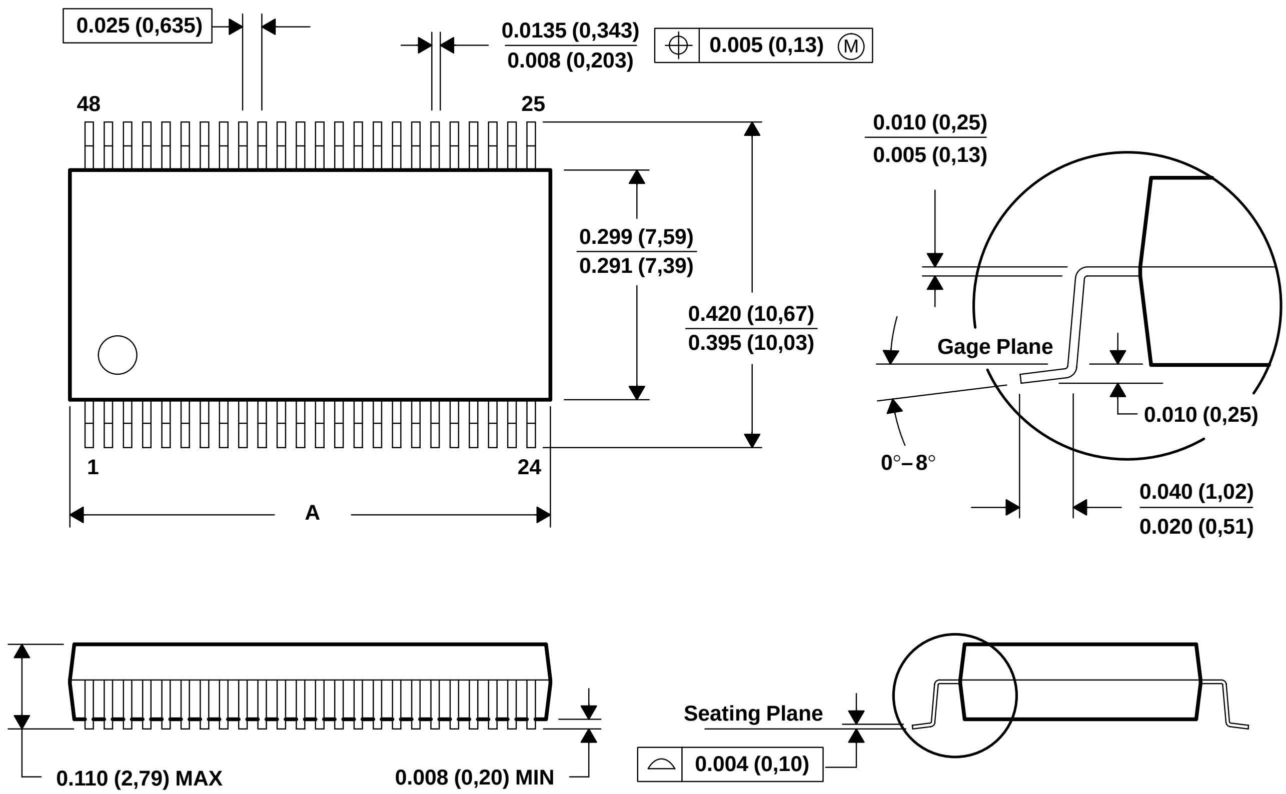
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN75LBC978DLR	DL	56	SITE 41	346.0	346.0	49.0

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

IMPORTANT NOTICE

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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