

# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

- Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A
- Meet ITU Recommendations V.10 and V.11
- Designed to Operate Up to 20 Mbaud
- -7 V to 7 V Common-Mode Input Voltage Range With 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 k $\Omega$  Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement  
35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

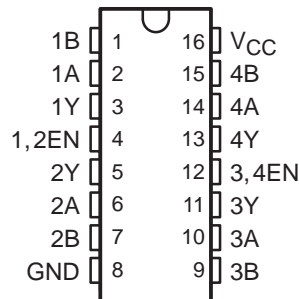
## description

The SN55ALS195 and SN75ALS195 are four differential line receivers with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

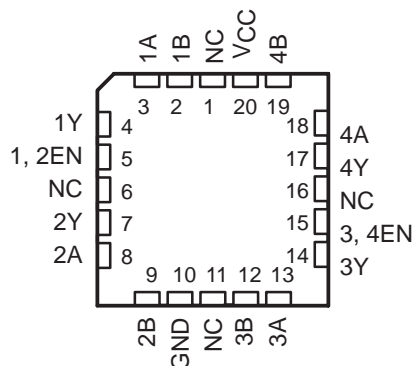
The devices are optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of  $\pm 200$  mV over a common-mode input voltage range of  $\pm 7$  V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

The SN55ALS195 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN75ALS195 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN55ALS195 . . . J OR W PACKAGE  
SN75ALS195 . . . J OR N PACKAGE†  
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection  
† For surface-mount package, see the SN75ALS199.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

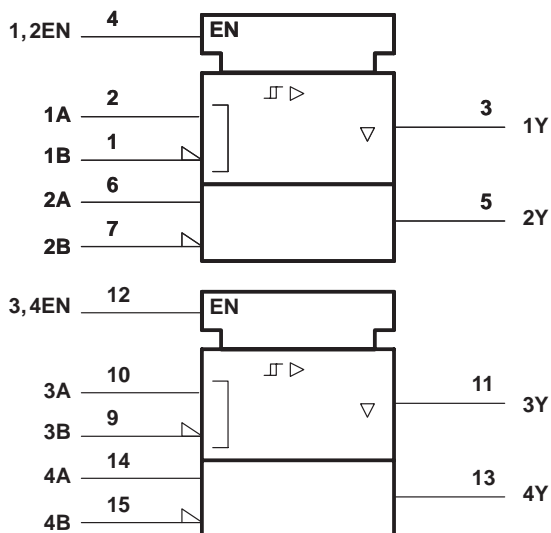
SLLS010D – JUNE 1986 – REVISED MAY 1995

**FUNCTION TABLE**  
(each receiver)

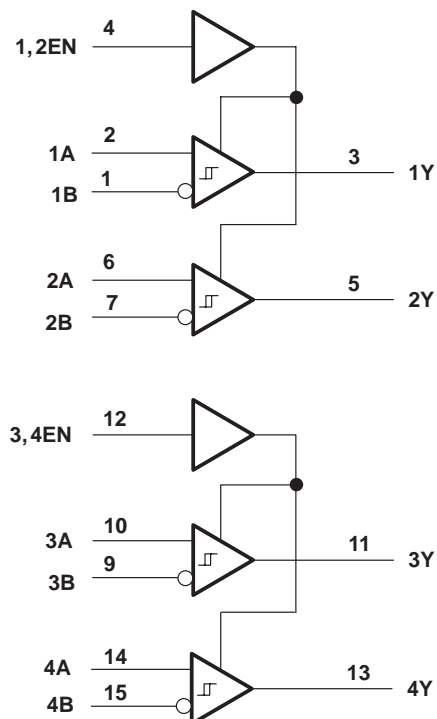
DIFFERENTIAL INPUTS A-B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2V$	H	H
$-0.2V < V_{ID} < 0.2V$	H	?
$V_{ID} \leq -0.2V$	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant, ? = indeterminate,  
Z = high impedance (off)

## logic symbol†



## logic diagram



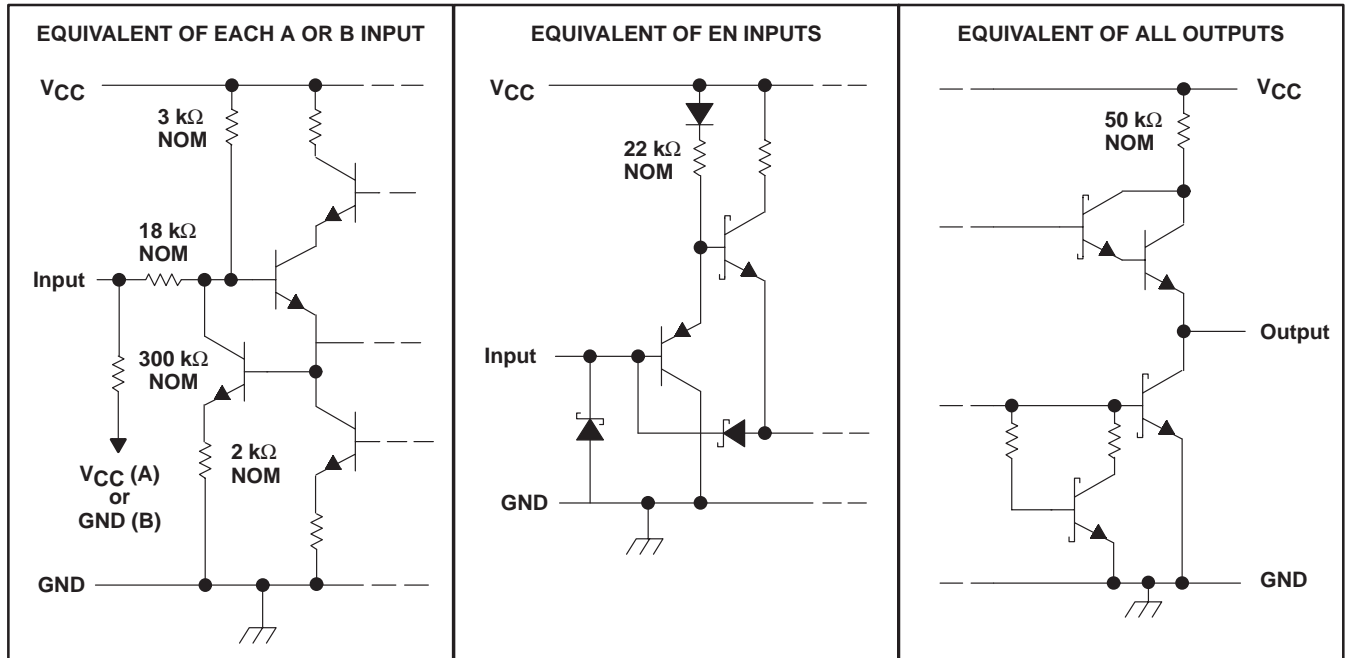
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J, N, and W packages.

# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, A or B inputs, $V_I$	$\pm 15$ V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 15$ V
Enable input voltage, $V_I$	7 V
Low-level output current, $I_{OL}$	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : SN55ALS195	$-55^\circ\text{C}$ to $125^\circ\text{C}$
SN75ALS195	$0^\circ\text{C}$ to $70^\circ\text{C}$
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Case temperature for 60 seconds, $T_C$ : FK package	$260^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, N, or W package	$300^\circ\text{C}$

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.  
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/ $^\circ\text{C}$	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/ $^\circ\text{C}$	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/ $^\circ\text{C}$	656 mW	N/A
N	1150 mW	9.2 mW/ $^\circ\text{C}$	736 mW	N/A
W	1000 mW	8.0 mW/ $^\circ\text{C}$	640 mW	200 mW

# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

## recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V		
Common-mode input voltage, $V_{IC}$	±7			±7			V		
Differential input voltage, $V_{ID}$	±12			±12			V		
High-level input voltage, $V_{IH}$	2			2			V		
Low-level input voltage, $V_{IL}$	0.8			0.8			V		
High-level output current, $I_{OH}$	-400			-400			μA		
Low-level output current, $I_{OL}$	16			16			mA		
Operating free-air temperature, $T_A$	-55			125			0	70	°C

## electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT	
$V_{IT+}$	Positive-going input threshold voltage					200	mV	
$V_{IT-}$	Negative-going input threshold voltage			-200§			mV	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			120			mV	
$V_{IK}$	Enable-input clamp voltage	$V_{CC} = \text{MIN}$ ,	$I_I = -18 \text{ mA}$			-1.5	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ , See Figure 1	$V_{ID} = 200 \text{ mV}$ , $I_{OH} = -400 \text{ μA}$	2.5	3.6		V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{ID} = -200 \text{ mV}$ , See Figure 1	$I_{OL} = 8 \text{ mA}$			0.45	V	
			$I_{OL} = 16 \text{ mA}$			0.5		
$I_{OZ}$	High-impedance-state output current	$V_{CC} = \text{MAX}$ , $V_O = 2.7 \text{ V}$	$V_{IL} = 0.8 \text{ V}$ , $V_{ID} = -3 \text{ V}$ ,			20	μA	
			$V_{IL} = 0.8 \text{ V}$ , $V_{ID} = 3 \text{ V}$ ,			-20		
$I_I$	Line input current	Other input at 0 V, See Note 3	$V_{CC} = \text{MIN}$ , $V_I = 15 \text{ V}$	0.7	1.2	mA		
			$V_{CC} = \text{MAX}$ , $V_I = -15 \text{ V}$	-1	-1.7			
$I_{IH}$	High-level enable-input current	$V_{CC} = \text{MAX}$	$V_{IH} = 2.7 \text{ V}$			20	μA	
			$V_{IH} = 5.25 \text{ V}$			100		
$I_{IL}$	Low-level enable-input current	$V_{CC} = \text{MAX}$ ,	$V_{IL} = 0.4 \text{ V}$			-100	μA	
$r_i$	Input resistance			12	18		kΩ	
$I_{OS}$	Short-circuit output current	$V_{CC} = \text{MAX}$ , See Note 4	$V_{ID} = 3 \text{ V}$ , $V_O = 0$ ,	-15	-78	-130	mA	
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ ,	Outputs disabled			22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.

4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$V_{ID} = 0\text{ to }3\text{ V}$ , See Figure 2		15	22	ns
$t_{PHL}$ Propagation delay time, high- to low-level output			15	22	ns
$t_{PZH}$ Output enable time to high level	See Figure 3		13	25	ns
$t_{PZL}$ Output enable time to low level			10	25	
$t_{PHZ}$ Output disable time from high level	See Figure 3		19	25	ns
$t_{PLZ}$ Output disable time from low level			17	22	

## PARAMETER MEASUREMENT INFORMATION

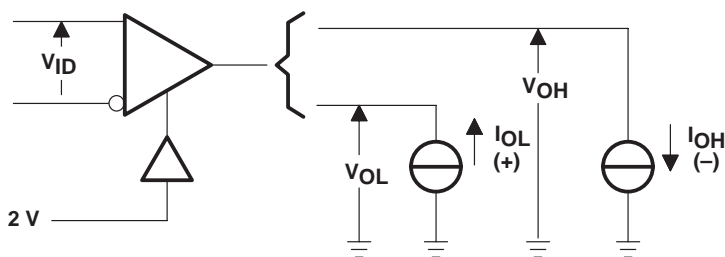
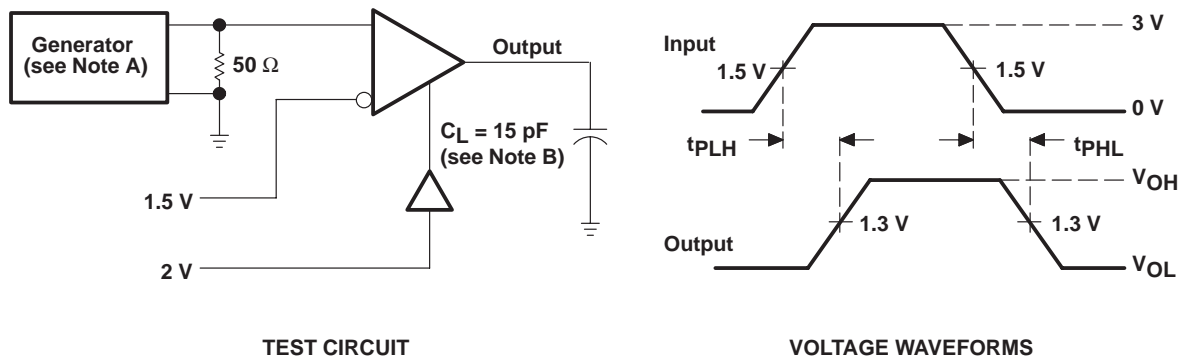


Figure 1.  $V_{OH}$ ,  $V_{OL}$



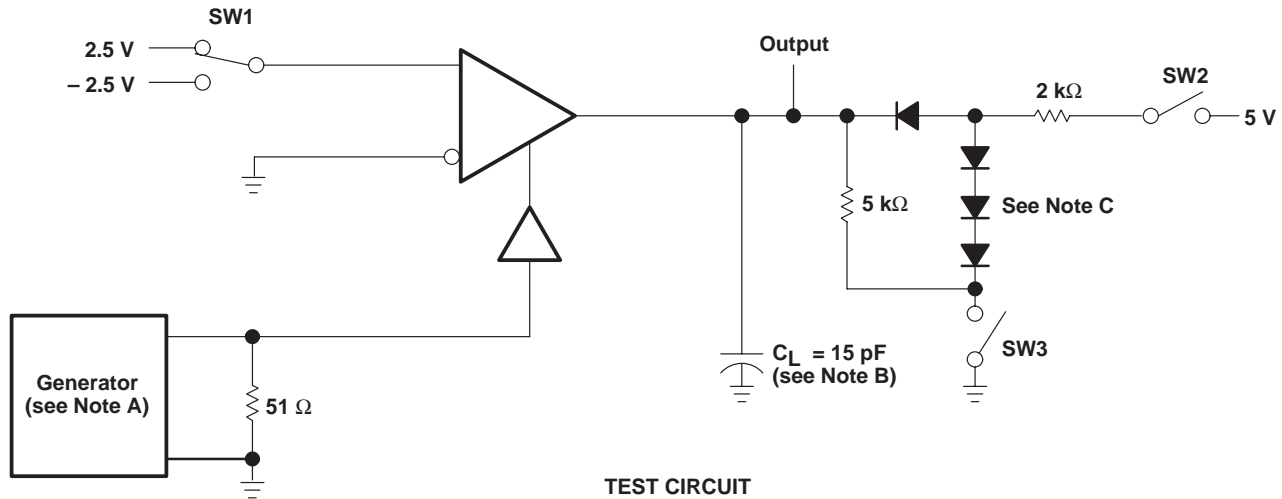
- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1\text{ MHz}$ , duty cycle  $\leq 50\%$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

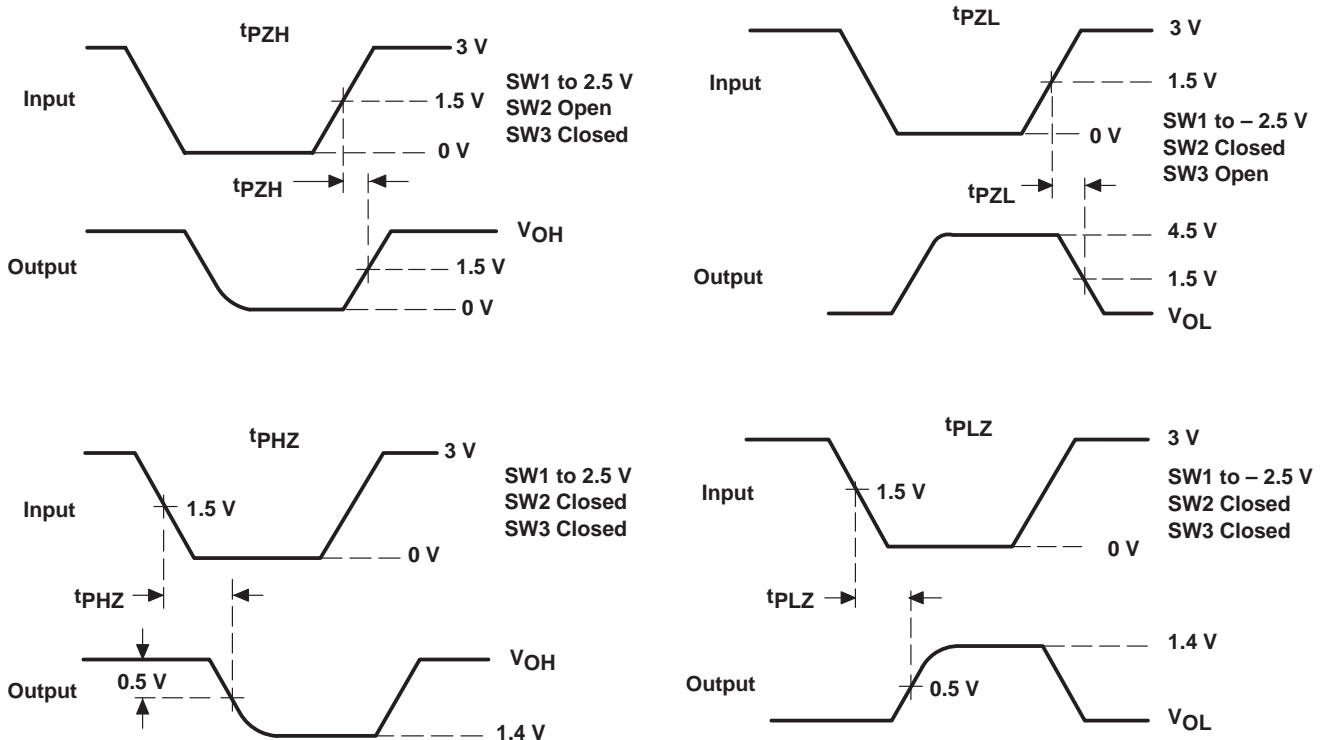
# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

## PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1 \text{ MHz}$ , duty cycle  $\leq 50\%$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

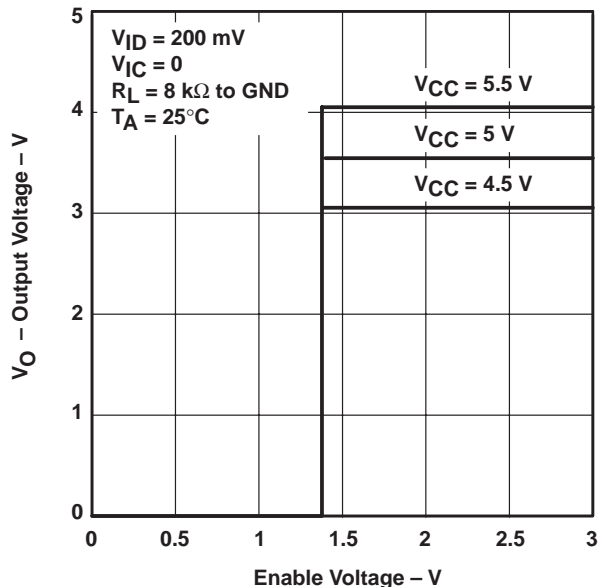


Figure 4

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

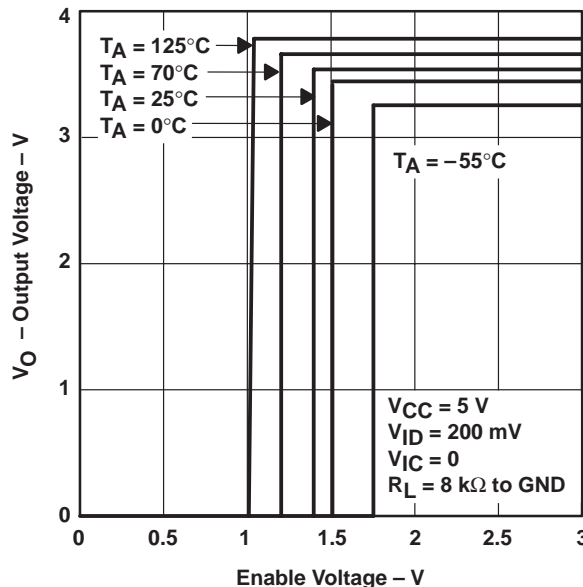


Figure 5

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

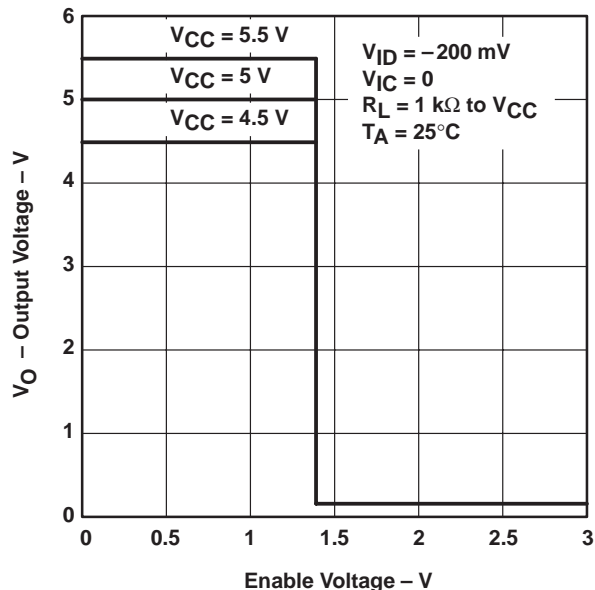


Figure 6

OUTPUT VOLTAGE  
 vs  
 ENABLE VOLTAGE

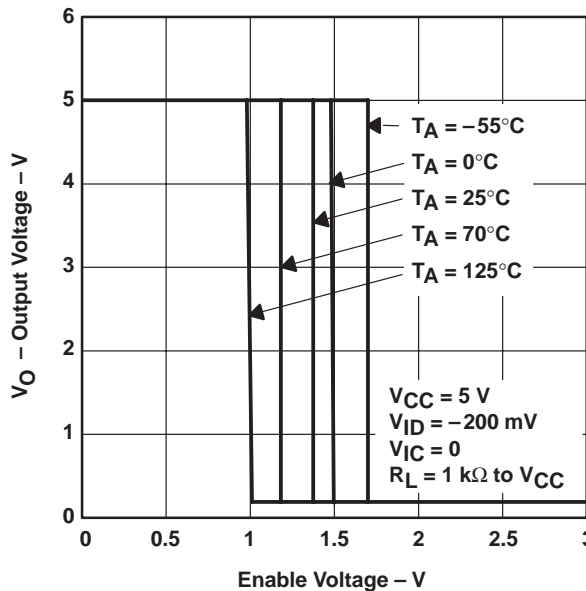


Figure 7

† Data for temperatures below  $0^\circ\text{C}$  and above  $70^\circ\text{C}$ , and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

## TYPICAL CHARACTERISTICS†

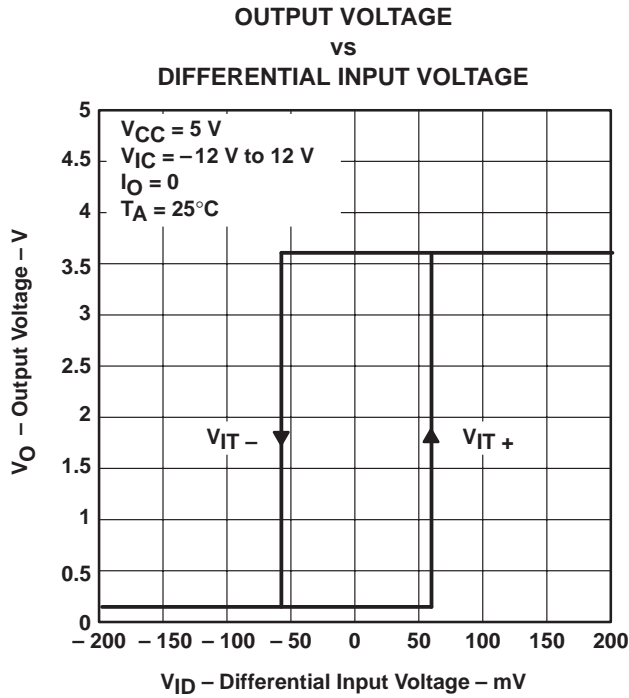


Figure 8

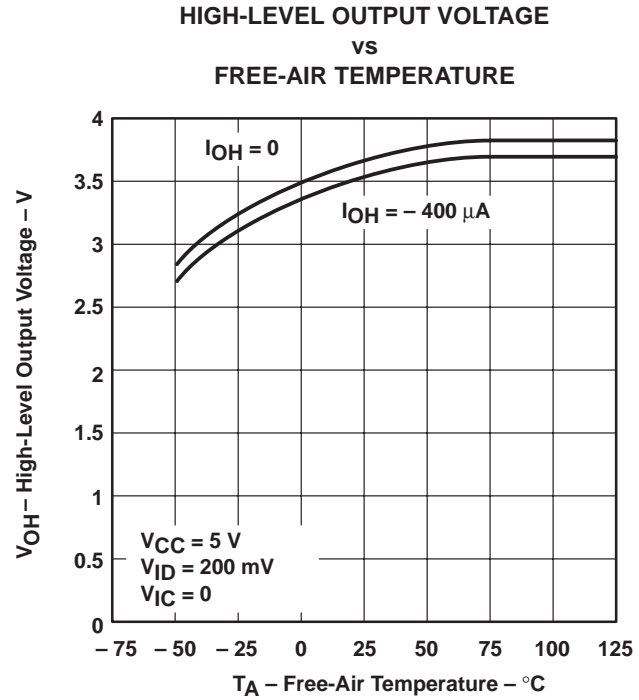


Figure 9

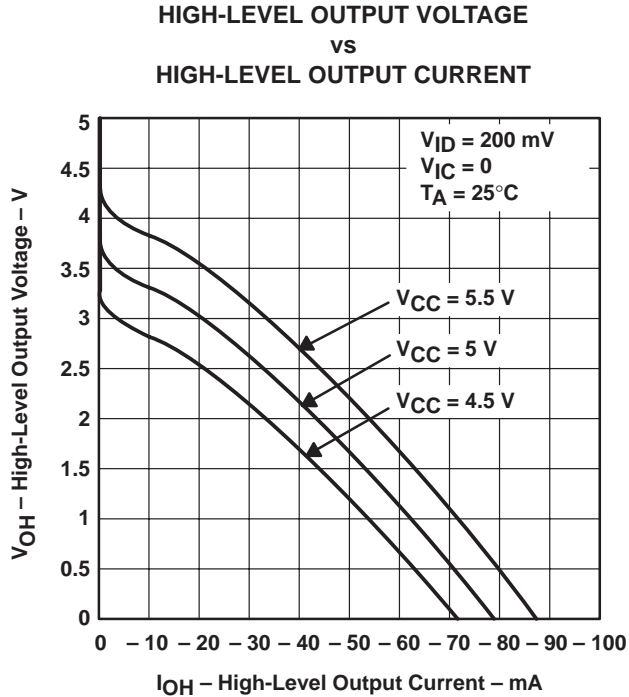


Figure 10

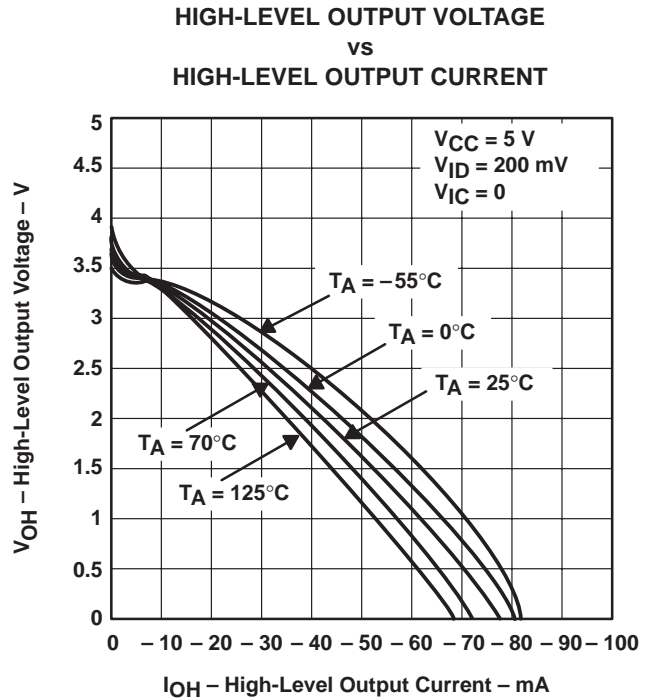


Figure 11

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.



TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 FREE-AIR TEMPERATURE

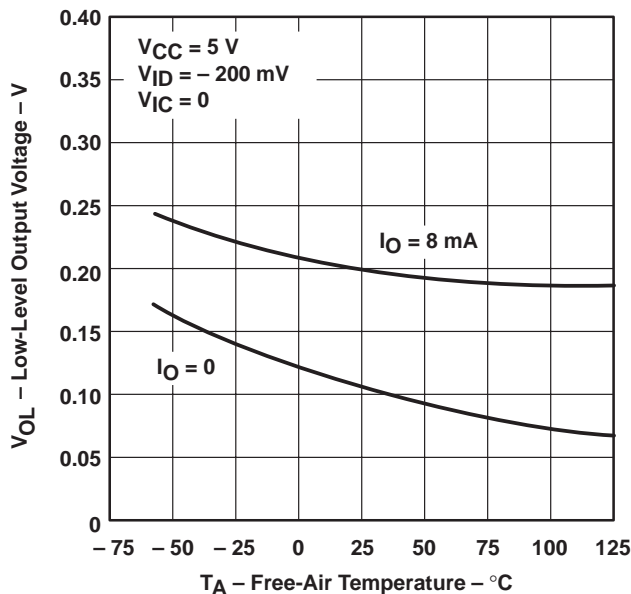


Figure 12

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

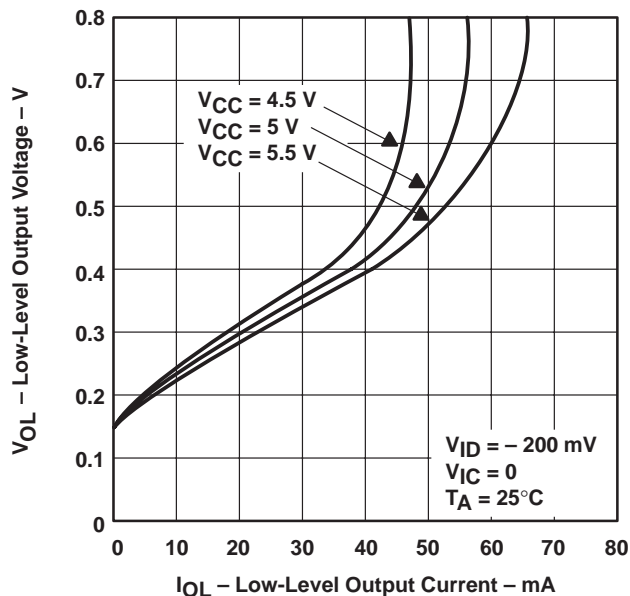


Figure 13

LOW-LEVEL OUTPUT VOLTAGE  
 vs  
 LOW-LEVEL OUTPUT CURRENT

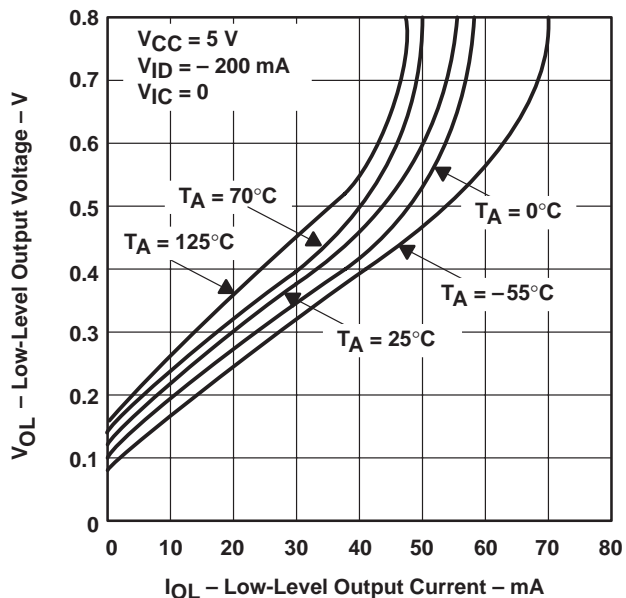


Figure 14

† Data for temperatures below  $0^\circ\text{C}$  and above  $70^\circ\text{C}$ , and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

# SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

## TYPICAL CHARACTERISTICS†

**SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

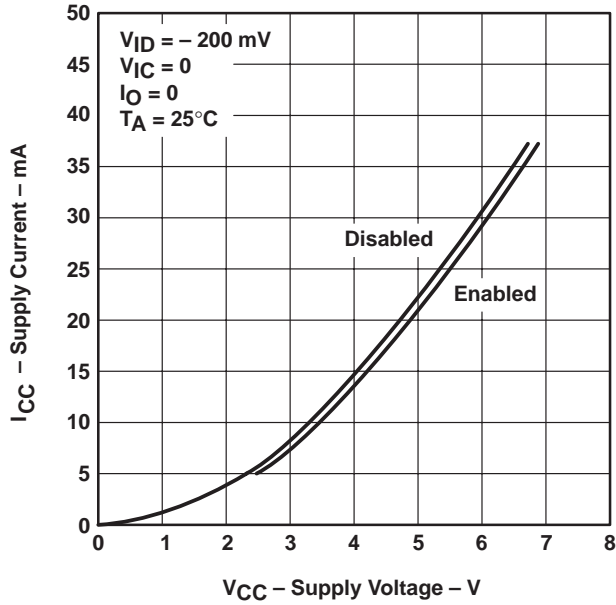


Figure 15

**SUPPLY CURRENT  
vs  
FREE-AIR TEMPERATURE**

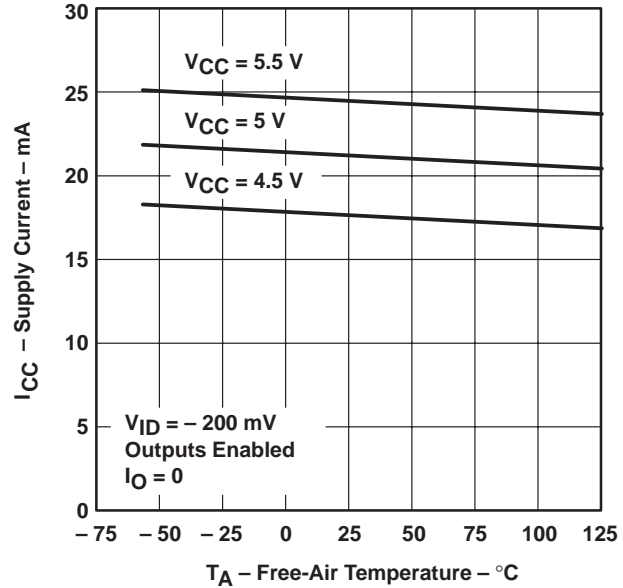


Figure 16

**SUPPLY CURRENT  
vs  
DIFFERENTIAL INPUT VOLTAGE**

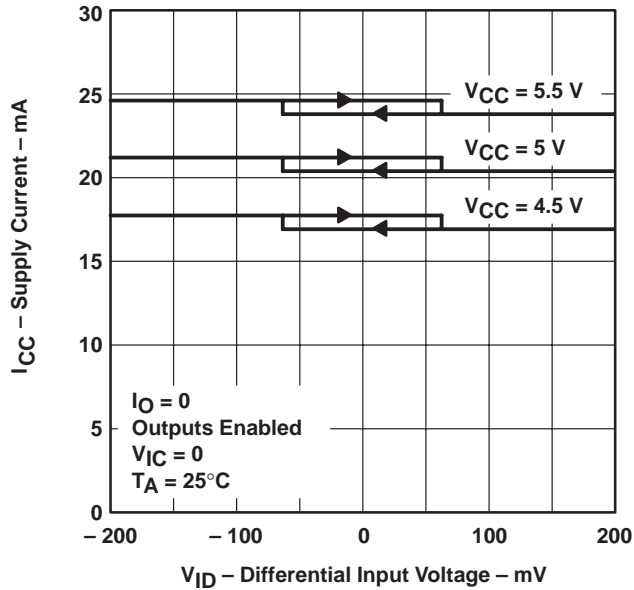


Figure 17

**SUPPLY CURRENT  
vs  
FREQUENCY**

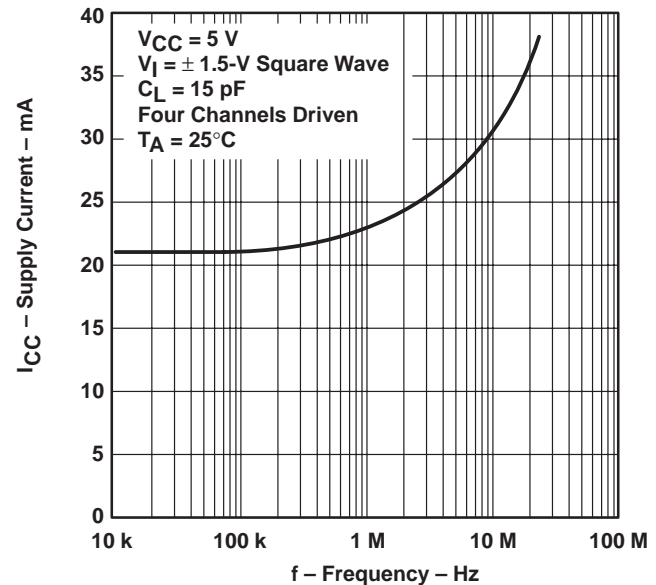


Figure 18

† Data for temperatures below  $0^\circ\text{C}$  and above  $70^\circ\text{C}$ , and below  $4.75 \text{ V}$  and above  $5.25 \text{ V}$ , are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

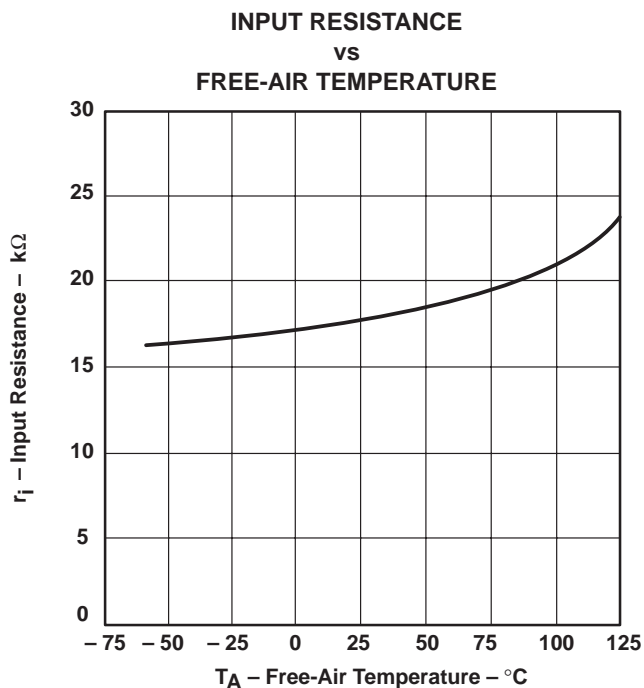


Figure 19

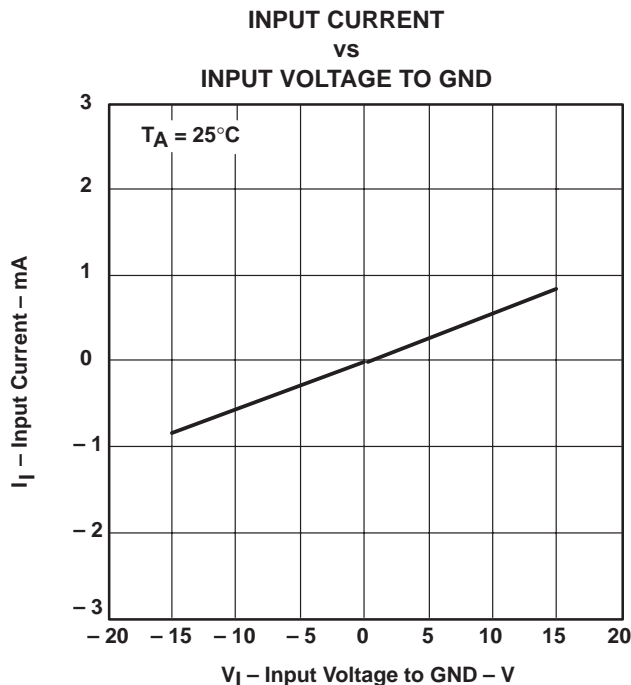


Figure 20

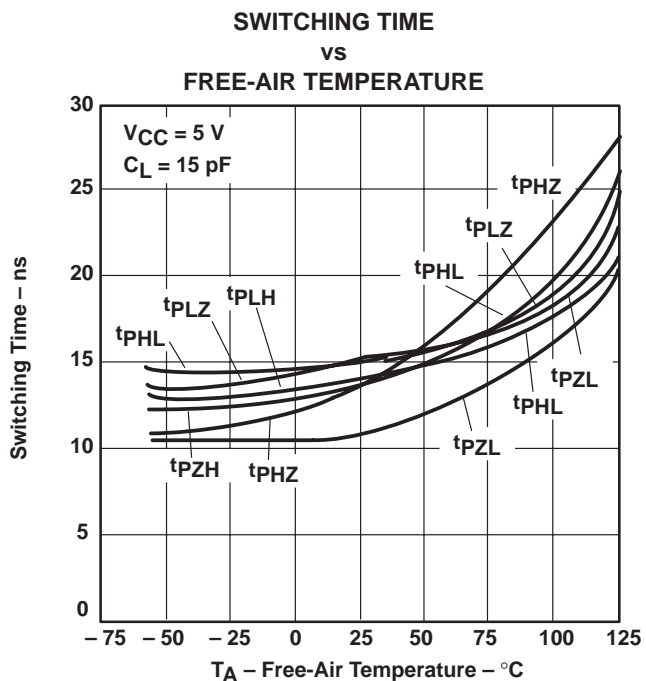


Figure 21

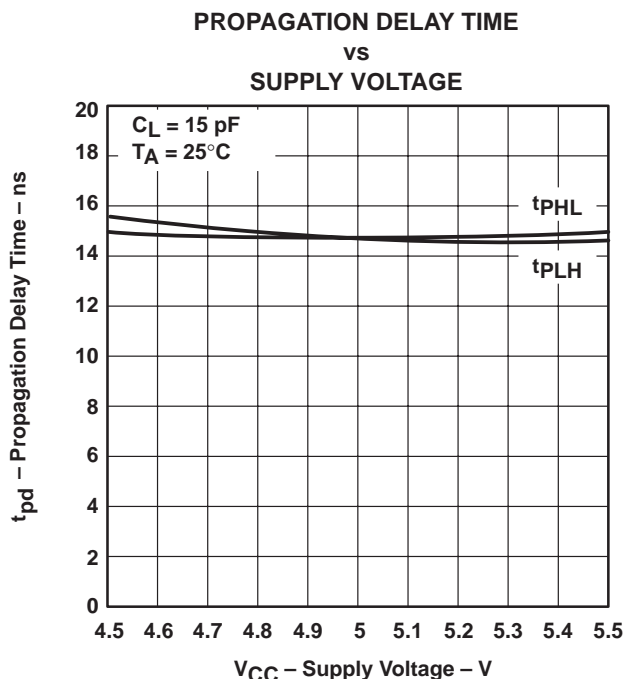


Figure 22

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.